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COMPARISON OF GDI BASED D FLIP FLOP CIRCUITS USING 90NM AND 180NM TECHNOLOGY

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ABSTRACT

Energy performance requirements are forcing designers of next-generation systems to explore approaches to lease possible power consumption. Power consumption is majorly affected by power supply voltage. Scaling of power supply voltage is major factor to reduce power consumption. The technique to achieve ultra-low power is to operate the circuit with supply voltage less than threshold voltage. The region where supply voltage is less than threshold voltage is called sub threshold region. Ultra-low power consumption can be achieved by operating digital circuits at sub threshold region. Here proposed sub threshold circuit is based on GDI (Gate Diffusion Input) technique. GDI technique allows reducing power consumption, delay, area of the digital circuit while maintaining low complexity of logic design as compared to other CMOS (Complementary Metal Oxide Semiconductor) circuits. In this article a new implementation of efficient D-Flip-Flop (DFF) using Gate-Diffusion-Input (GDI) technique, is presented. This DFF design allows reducing power-delay product and area of the circuit, while maintaining low complexity of logic design. Performance comparison with other DFF design techniques is presented, with respect to gate area, number of devices, delay and power dissipation, showing advantages and drawbacks of GDI DFF, as compared to other methods. A D-flip-flop is proposed by using different technologies for VLSI system for making high performance processing element. The performance is carried out by tanner tool.

KEYWORDS: D flip-flop, low power, Gate-Diffusion-Input (GDI) technique.

INTRODUCTION

Increasing demand for battery-operated mobile platforms like laptops, cellular phones, etc., has led to the requirement for circuit designs to be more power aware. Scaling of power supply voltage is major factor to reduce the power consumption. Sub threshold operation has gained a lot of attention due to ultralow-power consumption applications requiring low to medium performance. It has also been shown that by optimizing the device structure, power consumption of digital sub threshold logic can be further minimized while improving its performance. To accomplish this task circuit with lower frequency should be operated in the weak inversion region or sub threshold region. Sub threshold circuits are very sensitive to process variations and temperature fluctuation. These, and other factors, have to be taken into consideration when designing circuits for sub threshold operation. The architectural technique described in this paper suggests a design to minimize area and capacitance by using Gate Diffusion Input (GDI) multiplexer. As feature size of the CMOS (Complementary Metal Oxide Semiconductor) technology continues to scale down, leakage power has become an ever-increasing important part of the total power consumption of a chip. By utilizing the leakage current of devices working in sub threshold region, we propose a method to reduce the leakage power of D flip flops in this paper by using GDI technique. Implementing and simulating the D flip flop using the GDI technique and operating it in sub threshold or weak inversion region, reduces the area, and power consumption as well as power delay product w.r.t. the conventional CMOS circuits.

Binary logic has been widely used in the electronic fields. It is traditional and thus, more mature than multiple-valued logic. However, alongside the booming of the information and electronic industry, the deficiencies of binary circuits began to emerge. It has been rather difficult for binary logic to satisfy demands from chip area, switching speed, power dissipation, and other aspects all at the same time. Therefore, multiple valued circuits are becoming

increasingly important. Digital circuits in every high speed technology are typically benchmarked by the performance of static frequency dividers which is recognized as a figure of merit for a digital integrated circuit process, because a static frequency divider uses the same basic flip-flop elements found in more complex sequential circuits [1].

High speed frequency dividers are one of the key devices in measurement equipments, microwave and satellite communication systems. Therefore, many different high speed static and dynamic frequency dividers based on various kinds of device technology have been developed. The fastest frequency dividers to date are the AlInAs/GalnAs HBT static frequency divider operating at 39.5GHz [2], the AlGaAs/GaAs HEMT and the T-gate A1GaAs/InGaAs MODFET dynamic frequency dividers at 34GHz [3] and 51GHz [4], respectively. In Addition, a 30GHz static frequency divider based on the Si-bipolar technology has been reported in [5]. On the Other hand, building low power VLSI systems has emerged as highly in demand because of the fast growing technologies in mobile communication and computation. The battery technology does not advance at the same rate as the microelectronics technology. There is a limited amount of power available for the mobile systems. So designers are faced with more constraints: high speed, high throughput, small silicon area, and at the same time, low power consumption. Therefore building low power, high performance circuits are of great interest. Wide utilization of memory storage systems and sequential logic in modern electronics triggers a demand for high-performance and low-area implementations of basic memory components. One of the most important state-holding elements is the D-Flip-Flop (DFF) [1]. Various DFF circuits were researched and presented in the literature, aiming to achieve an optimal design in terms of delay, power and area. Some efficient techniques were developed and adopted by designers for a variety of technologies [1].

BASIC GDI FUNCTION

The GDI method is based on the use of a simple cell as shown in Fig. 1. At first glance, the basic cell reminds one of the standard CMOS inverter, but there are some important differences.

1) The GDI cell contains three inputs: (common gate input of nMOS and pMOS), P (input to the source/drain of pMOS), and N (input to the source/drain of nMOS).
2) Bulks of both nMOS and pMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with a CMOS inverter.

Gate-Diffusion-Input (GDI) design technique that was recently developed and presented in [6], proposes an efficient alternative for logic design in standard CMOS and SOI technologies. The GDI method is based on the simple cell shown in Fig. 1. A basic GDI cell contains four terminals - G (the common gate input of the nMOS and pMOS transistors), P (the outer diffusion node of the pMOS transistor), N (the outer diffusion node of the nMOS transistor) and the D node (the common diffusion of both transistors). P, N and D may be used as either input or output ports, depending on the circuit structure. Table 1 shows how various configuration changes of the inputs P, N and G in the basic GDI cell correspond to different Boolean functions at the output D. GDI enables simpler gates, lower transistor count, and lower power dissipation in many implementations, as compared with standard CMOS and PTL design techniques [6]. Multiple-input gates can be implemented by combining several GDI cells. The buffering constraints, due to possible VTH drop, are described in detail in [6], as well as technological compatibility with CMOS and SOI.

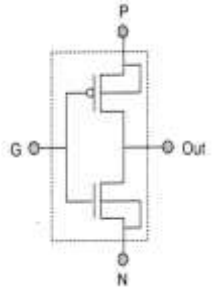

Fig:-1 GDI basic cell

It must be remarked that not all of the functions are possible in standard p-well CMOS process but can be successfully implemented in twin-well CMOS or silicon on insulator (SOI) technologies.

N	P	G	Out	Function
'0'	B	A	$\bar{A}B$	F1
B	'1'	A	$\bar{A}+B$	F2
'1'	B	A	$A+B$	OR
B	'0'	A	AB	AND
C	B	A	$\bar{A}B+AC$	MUX
'0'	'1'	A	$\bar{A}$	NOT

Table-1 Various Logic Functions of GDI Cell for different configurations

POWER CONSUMPTION IN CMOS CIRCUITS

There are three main components of power consumption in digital CMOS VLSI circuits.

*[1] **Switching Power**: consumed in charging and discharging of the circuit capacitances during transistor switching.*

*[2] **Short-Circuit Power**: consumed due to short-circuit current flowing from power supply to ground during transistor switching. This power more dominates in Deep Sub Micron (DSM) technology.*

*[3] **Static Power**: consumed due to static and leakage currents flowing while the circuit is in a stable state. The first two components are referred to as dynamic power, since power is consumed dynamically while the circuit is changing states. Dynamic power accounts for the majority of the total power consumption in digital CMOS VLSI circuits at micron technology [15], [16].*

$$P_{avg}=P_{Switching}+P_{Short\text{-}Circuit}+P_{Leakage}$$

$$=(\alpha_{0\rightarrow 1}\times C_L\times V_{dd}^2\times f_{clk})+(I_{sc}\times V_{dd})+(I_{leakage}\times V_{dd})$$

SIMULATION AND COMPARISON

Due to the topological differences among the existing latches, some of them required a modified test bench, i.e., a dual input and/or a single output. However, these modifications did not alter the principal of the analysis approach based on the simulation conditions. The role of the test bench is to provide the realistic data and clock signals, the fan out signal degradation from the previous and to the succeeding stage, and measurement of power dissipated on switching of the clock and data inputs. Buffering inverters provide the realistic data and clock signals, which themselves are fed from ideal voltage sources. Furthermore, capacitive load at the data input simulates the fan out signal degradation from previous stages. Capacitive loads at the outputs simulate the fan out signal degradation caused by the succeeding stages.As mentioned in the section on power considerations, there are three kinds of power dissipation that were measured in order to get the real insight in the amount of power consumed in and around the latch due to its presence.

- Local data power dissipation presents the portion of the gray inverter's power consumption dissipated on switching the data input capacitance.
- Local clock power dissipation presents the portion of the black inverter's power consumption dissipated on switching the clock input capacitance.
- Internal power dissipation includes the intrinsic power dissipated on switching the internal nodes of the circuit and excludes the power dissipated on switching the output load capacitances.

The Circuit is simulated using 180 nm Technology and using 90 nm Technology.

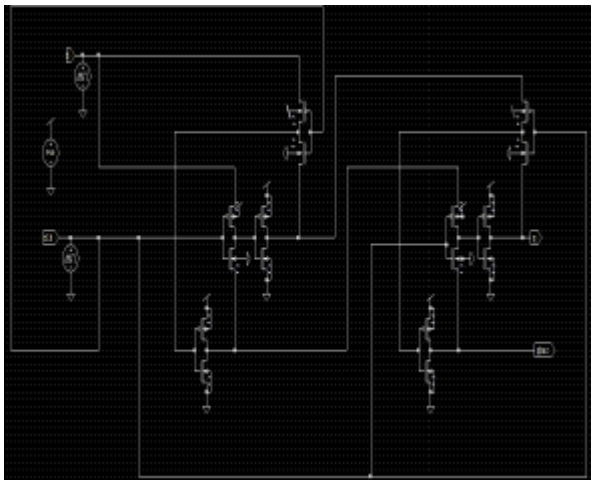

Fig:-2 16T D Flip Flop using GDI D FLIP FLOP

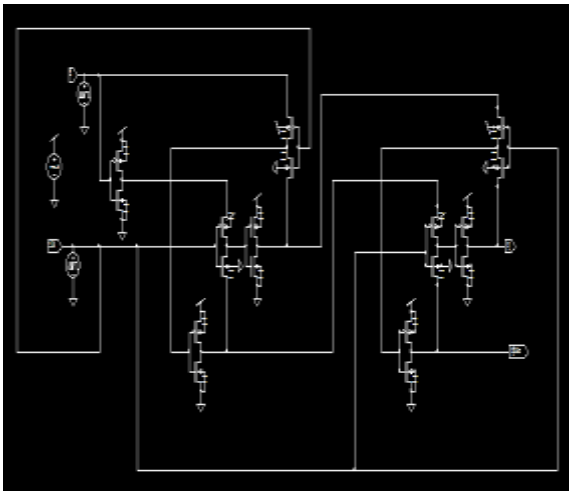

Fig:-3 18T D Flip Flop using GDI D FLIP FLOP

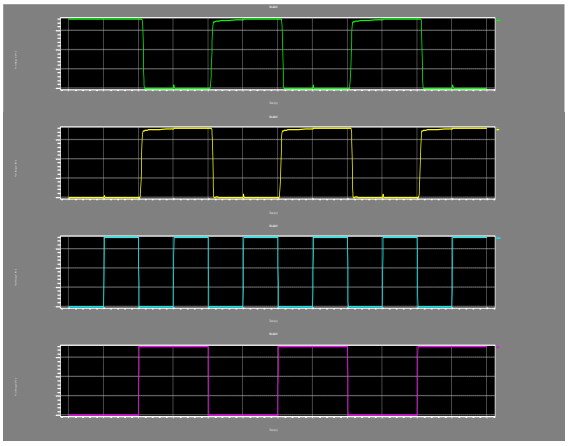

Fig:-4 WAVEFORM OF GDI D FLIP FLOP

FINAL RESULT

Design Style	No. of transistors	Width of NMOS (µm)	Width of PMOS (µm)	Avg. Power Consumed (watts)	Prop. Delay (sec)	Power Delay Product PDP
1bit GDI DFF	16	.20	.75	$2.064 x10^{-5}$	$1.152 x10^{-10}$	$2.377 x10^{-15}$
1 bit GDI DFF	18	.20	.75	$2.284 x10^{-5}$	$1.011 x10^{-11}$	$2.309 x10^{-16}$

Table:-2 Comparison between 1 Bit D Flip Flop Circuits Using 180nm Technology (v =1.6volts)

Design Style	No. of transistors	Width of NMOS (µm)	Width of PMOS (µm)	Avg. Power Consumed (watts)	Prop. Delay (sec)	Power Delay Product PDP
1 bit GDI DFF	16	.12	.38	$3.127 x10^{-5}$	$6.535 x10^{-11}$	$20.434 x10^{-16}$
1 bit GDI DFF	18	.12	.38	$3.369 x10^{-5}$	$7.568 x10^{-11}$	$25.496 x10^{-16}$

Table:-3 Comparison between 1 Bit D Flip Flop Circuits Using 90nm Technology (v =1.6volts)

Design Style	No. of transistors	Width of NMOS (µm)	Width of PMOS (µm)	Avg. Power Consumed (watts)	Prop. Delay (sec)	Power Delay Product PDP
16 bit GDI DFF	256	.20	.75	$3.299 x10^{-4}$	$1.15 x10^{-10}$	$3.793 x10^{-14}$
16 bit GDI DFF	288	.20	.75	$3.65 x10^{-4}$	$1.17 x10^{-10}$	$4.270 x10^{-14}$

Table:-4 Comparison between 16 Bit D Flip Flop Circuits Using 180nm Technology (v =1.6volts)

Design Style	No. of transistors	Width of NMOS (µm)	Width of PMOS (µm)	Avg. Power Consumed (watts)	Prop. Delay (sec)	Power Delay Product PDP
16 bit GDI	256	.12	.38	$4.985 x10^{-4}$	$6.535 x10^{-11}$	$32.57 x10^{-15}$

DFF						
16 bit GDI DFF	288	.12	.38	5.363 $x10^{-4}$	5.918 $x10^{-11}$	31.73 8 $x10^{-15}$

Table:-5 Comparison between 16 Bit D Flip Flop Circuits Using 90nm Technology (v =1.6volts)

CONCLUSIONS AND FUTURE RESEARCH

A new implementation of high-performance D-Flip- Flop using Gate-Diffusion-Input technique was presented. The proposed circuit has a simple structure, based on Master-Slave principle, and contains 18 transistors. An optimization procedure was developed for GDI DFF, based on iterative transistor sizing, while targeting a minimal power-delay product. Performance comparison with other DFF design techniques was shown, with respect to gate area, number of devices, delay and power dissipation. A variety of circuits have been implemented in 90 nm and 180 nm technologies to compare the proposed GDI structure with a set of representative flip-flops, commonly used for high performance design.

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