Wafer bonding process for zero level vacuum packaging of MEMS

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***Abstract*—It is well known that the packaging of electronic devices is of paramount importance, none more so than in MEMS were fragile mechanical elements are realized. Among the different approaches, wafer to wafer bonding guarantees the advantages of the wafer scaling and provides protection of the devices during the final phase of fabrication. Direct bonding, also known as fusion bonding, is seldom implemented in MEMS fabrication due to the high surface quality required, the high temperature involved and the compulsory wet activation process. In this paper a direct bonding process for MEMS inertial sensor without the need of any wet activation step is presented.**

Keywords— MEMS zero-level packaging, Vacuum packaging, Direct bonding, Wafer-Level bonding, inertial sensor packaging

I. Introduction

MEMS devises are, by nature, extremely fragile mechanical elements. For this reason, a package is necessary for protecting the MEMS devices. Zero-level packaging has gained importance lately because it provides protection not only during the lifetime of the device but also during the back-end processing (e.g. dicing of the wafer). Wafer level packaging rapidly became a compulsory fabrication step for commercial products. Different approaches have been implemented to be compliant with different specifications defined by the specific typology of device. Low temperature processes have been widely investigated since a thermal budget is the major constraint for multiple applications. However, such low temperature approaches do not guarantee a hermetic seal required by most resonant devices.

A stable, low-pressure environment is typically achieved with anodic bonding, thermo-compression bonding or fusion bonding. Among these bonding techniques, fusion bonding guarantees the strongest bond. The main drawbacks of this bonding approach are the high temperature needed for the annealing of the bond and the stringent bond surface requirements, e.g. flatness and cleanliness. For this reason, the surface needs to be well protected during the various fabrication processes of the device and then properly cleaned and chemically activated, which typically involves chemicals baths (e.g. ammonia). However, fully released movable MEMS structures could be adversely affected by wet processes (i.e. stiction issue) and hence must be avoided. On the other hand, single crystal silicon MEMS could sustain the high temperature needed for annealing the direct bond.

In this paper we present a cleaning procedure that facilitates vacuum zero-level packaging by direct bonding of resonant devices realized in the EU CleanSky2 project MUPIA which aims to push forwards the performance of inertial resonant sensors. The devices where realized by bulk micro machining into the device layer of a silicon-on-insulator (SOI) wafer with cavities embedded in the wafer. The device wafer was bonded to a capping wafer with cavities above the mechanical element and through silicon vias (TSVs) providing electrical connections to the resonator after bonding.

This paper is organized as follows: Section II introduces the direct bonding process. Section III presents the fabrication process used to implement the direct bonding. In Section IV the process results are described highlighting challenges that were faced in the developing of the process. The paper is then concluded in Section V.

II. Direct bonding

Direct bonding is a process used to bond two surfaces without any additional bonding material. The bonding exploits close contact interactions such electrostatic, capillary and van der Waals forces, that are formed into stronger covalent bonds upon a subsequent high temperature anneal. The exploitation of such close contact interactions imposes strong requirements on roughness and cleanliness of the bonded surfaces. For this reason, the upstream fabrication processes need to be tailored to accommodate the bonding process. While the direct bonding could be used to bond various materials, in this paper we focus on silicon to silicon and silicon to silicon oxide bonding as these are the most exploited and relevant in the fabrication of MEMS devices.

As mentioned, the surface quality of the two bonding surfaces is of major importance to guarantee successful bonding. It has been observed that a roughness of more than 5 Å could lead to a great reduction of bond strength or even prevent bonding to occur [1]. Hence, suitable protective approaches, such as utilising temporary protective layers that are removed prior to bonding should be included upstream processes. One option is to use photoresist while another approach is to deposit or grow a suitable protective layer (e.g. Silicon Oxide). The surface is so critical that even a dry process, which in most cases is a standard alternative to wet processes, could jeopardize bonding quality.

Before bonding the wafers need to be thoroughly cleaned to remove any particles or residues that could be present on the surfaces. A typical cleaning process follows the standard RCA procedure, widely implemented in clean rooms, which removes particulates, metals, and organic residues. If a more aggressive cleaning is required one can use Piranha cleaning.

Direct bonding relies on forming strong hydrogen bonds at room temperature which will be turned into covalent bonds during the annealing process. In silicon, this is possible only if the bonding surfaces have the same termination type. For bare Si surfaces it is common to treat the surface to dilute HF to create either F-terminated or H-terminated Si atoms that create the characteristic hydrophobic surface. In cases where the MEMS structures are susceptible to wet processing, a vapour HF (VHF) process can also be used. The H-F hydrogen bond results in a Si-Si covalent bond after annealing that is as

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electrically conductive as the bulk Si. When bonding surfaces with SiO_2, an H-O hydrogen bond is required. This could be done by solutions containing H^+ or OH^- or alternatively by exposing the surface to a plasma. A rinse in DI-water facilitates the bond by extending the range of the van der Waals force. After annealing the hydrophilic O-H bond results in a Si-O-Si covalent bond where the interface is electrically insulating, the extent of which is dependent on the SiO_2 thickness [2].

The two activated surfaces begin to bond once in close contact at room temperature. The environmental pressure at which the prebonding is performed defines the pressure in which the MEMS is encapsulated. For resonant devices the quality factor improves inversely with the pressure and thus high vacuum is commonly used to reduce the damping factor and improve the quality of the resonance [3]. However, by reducing the pressure the number of water molecules functionalizing the surface tends to decrease [4] which can result in a weaker bond. Typically, the tool starts the pre-bond at the centre of the wafer and then propagates the bonding to the edge. The process allows a fine alignment between the two wafers. After pre-bonding, the bonded wafers are annealed at high temperature, typically above 950 °C, to form the high strength covalent bonds. This high temperature step is typically not compatible with either MEMS or integrated circuits due to thermal constraints imposed by the specific design, e.g. diffusion of doped areas. So, a great effort has been invested in lower the temperature of this step making this bonding process compatible with more processes. The low temperature annealing typically exploits a different activation process to guarantee higher activation energy compared to the wet actuation. This activation process consists of an oxygen plasma step [1] and was be implemented in the process described in this paper as it is compatible with the mechanically released MEMS structure.

III. FABRICATION PROCESS

This work aims to manufacture inertial MEMS sensors with performance beyond the state of art for a MEMS based sensor. Among the various aspects that were optimized in both the design and the fabrication processes, one of the most critical is the wafer-level bonding. This section briefly describes the fabrication process implemented in the project to realize the sensor. The fabrication process uses bonded SOI wafer that has embedded cavities (C-SOI), (Figure 1(a)). These cavities were realized by the wafer supplier (Okmetic [5]) based on our specific design. The oxide on the back side

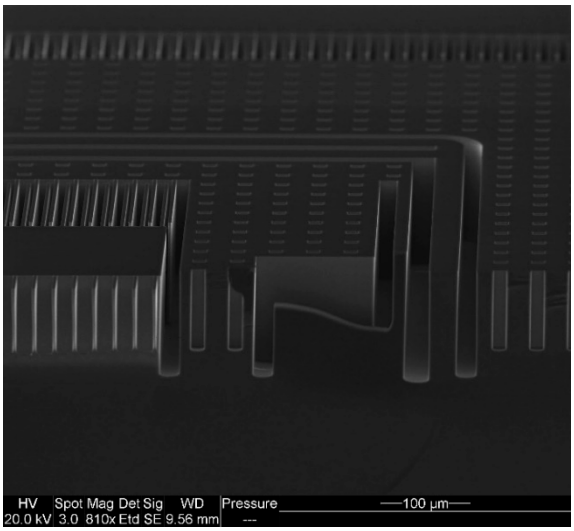

Figure 1: SEM image of the DRIE process developed for the project on a test wafer

was then patterned to open grounding contact to the handle wafer of the C-SOI, (Figure 1(b)). The device layer of the wafer was realised by deep reactive ion etching (DRIE) using a patterned oxide hard mask, (Figure 1(d)). To minimise back scattering and thus improve the lithography definition of the hard mask, a bottom anti reflective coating (BARC), made by a stack of thin layers deposited by PECVD, was integrated above the hard mask.

The resonant structure was realized into a 60 µm thick device layer of the C-SOI wafer. The DRIE process was optimized to achieve vertical walls as depicted in Figure 2. The last fabrication step before bonding was the hard mask removal. Since the DRIE process completely removed the BARC stack it was possible to remove the residues of the hard mask by a vapor HF step, (Figure 1(e)).

A 280 µm thick wafer was used to realize the capping wafer. Initially the wafer was oxidized with 1 µm of SiO_2, Figure 3 (a)). The bottom side of the wafer was patterned to realize an oxide hard mask used later to realize the cavities accommodating the MEMS (Figure 3 (b)). Before etching the

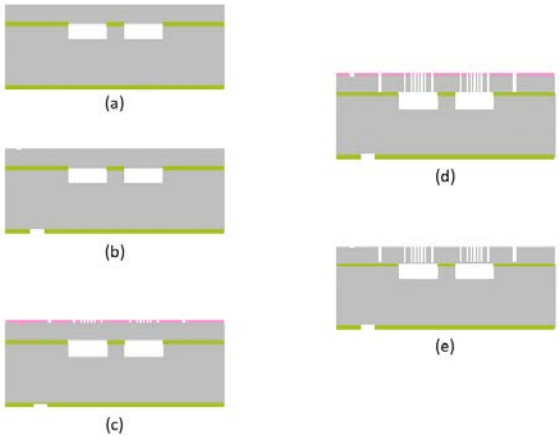

Figure 2: Main fabrication steps of the fabrication process used for the inertial device before bonding

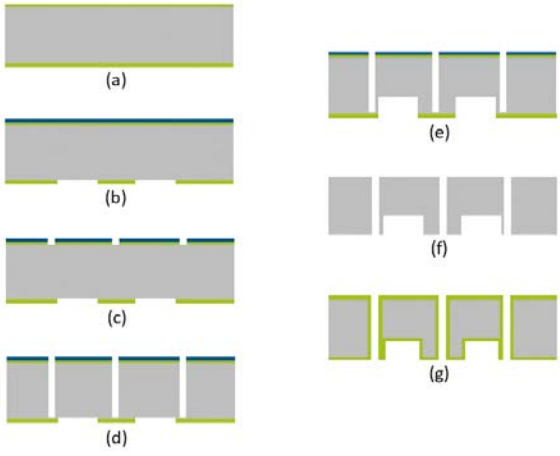

Figure 3: Fabrication process used to realize the capping wafers.

cavities, an aluminium hard mask was patterned on the top side of the wafer to realize Trough Silicon Vias (TSV) (Figure 3 (c)). The TSVs were etched with a DRIE process from the top side in Figure 3 (d) before etching of the cavities on the bottom side Figure 3.(e). The hard masks used to pattern the wafer were then removed Figure 3(f), the wafer was thoroughly cleaned followed by growth of a thick oxide were. The oxide layer was needed to passivate the TSVs and the bulk of the capping wafer.

The two wafers were then ready to be cleaned, fictionalized and pre-bonded. The cleaning process of the capping wafer was performed first in a piranha bath, which removes any organic contaminant and then in an ammonia bath. The wafer was then functionalized by the DI water rinse used after the ammonia cleaning.

Due to the delicate nature of the MEMS elements the device wafer could not be processed with wet processes at this stage. Instead the wafers were cleaned and activated with dry processes only. First the remaining oxide hard mask was removed by VHF after which the wafer which was exposed to a mild oxygen plasma used to both remove smaller organic residues and activate the surface. The alignment of wafers was performed with EVG620 tool from EVG within a short time frame. The bonding chuck used in the alignment keep the wafers aligned and separated by a 20 µm gap. Then the wafers were pre-bonded in EVG510. The wafers were first heated to 50 °C and then the bonded chamber was evacuated down to approximately 10^{-5} mbar. Once the pressure of the chamber reached the checkpoint the pre-bonding process starts by applying a pressure at the centre of the wafer and then on the whole surface. Since the pre-bonding exploits close contact forces, the force used for the pre-bonding was 1 kN.

After pre-bonding, the wafers were inspected with infrared imaging to assess the quality of the pre-bonding by highlighting any unbounded areas. The pre-bonded wafers were then stored for a day and checked in the IR imaging setup once again before the annealing process. This storing time improves the bond reducing the unbonded areas as shown in Figure 4. The pre-bonded wafers were then cleaned and annealed at high temperature, above 950 °C. The fabrication process of the inertial sensor is then concluded by the polysilicon filling of the TSVs and wire bonding pads as described in [6].

IV. Results and Discussion

The fabrication process described in the previous chapter was effectively implemented on both test wafers and C-SOI wafers. For the test wafers the bonding was successful, suggesting that the VHF process followed by oxygen plasma

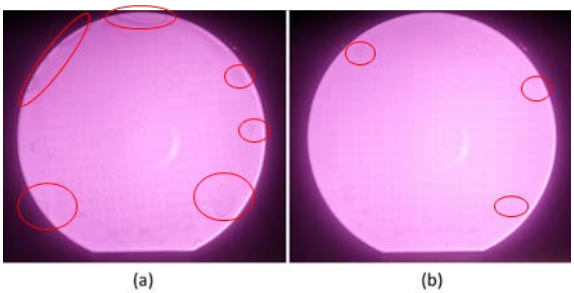

Figure 6: IR imaging of bonded wafer just after pre-bonding (a) and after 1 day (b). It is possible to see interference fields on the rim of the wafer after pre-bonding but not after 1 day,

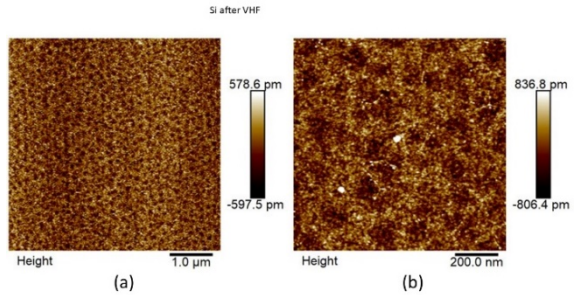

Figure 4: 5x5µm (a) and 1x1µm (b) AFM measurements of the Si surface treated with VHF.

activation could lead to a strong direct bond. Unfortunately, the C-SOI de-bonded during the cleaning procedures prior to the high temperature anneal. The C-SOI wafers were then investigated to find the cause of the failure.

The de-bonded wafers were analysed by atomic force microscopy (AFM), optical microscopy and scanning electron microscopy.

The device wafer used PECVD oxide as a protective layer from the beginning of the process. The VHF process used to remove the hard mask prior to bonding has a high selectivity towards SiO_x. However, since the PECVD chamber is also used to deposit dielectric films containing N and uses CF4 as a cleaning gas, traces of N, C and F can be found in PECVD SiO_x. These compounds are not as effectively removed by VHF as in wet etching and can thus reside on the surface after the VHF step. To remove any residues the wafers received a cleaning step in oxygen plasma.

To certify that the plasma cleaning step did not cause a roughening of the surface, AFM was used to measure the surface roughness of the device wafer (Figure 5) and the capping wafer (Figure 6). The two bonding surfaces were compared to a reference silicon wafer surface, which was only RCA cleaned. The roughness of all surfaces was measured on a 1x1 µm window. The resulting roughness was 2.3 Å for the reference silicon wafer, 2.4 Å for the device wafer with the surface treated in VHF and 2.5 Å for the thick thermal oxide layer. As expected, the roughness of the processed wafers results comparable with the reference silicon and compatible with the wafer bonding process.

Even if the bonded wafers surfaces had extremely low roughness, the microscope inspection of the device C-SOI wafers revealed agglomerates on fixed electrodes that were not found in any of the test wafers (Figure 7). These agglomerates were present on most devices in identical

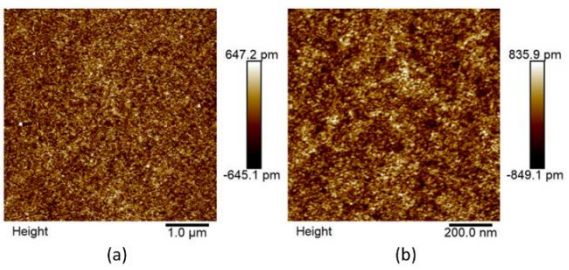

Figure 5: 5x5µm (a) and 1x1µm (b) measurements of the SiO2 surface of the capping wafer

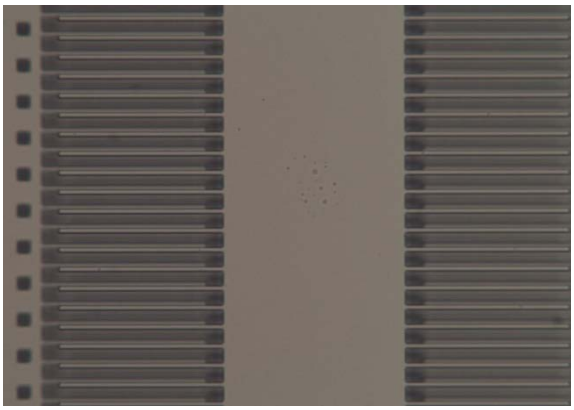

Figure 7: Optical image of a fixed electrode of a device realized in a Cavity BSOI wafer, Particles can be seen in the center of the electrode.

positions. Even with several subsequent plasma treatments, the agglomerates were not removed. The agglomeration problem occurred mostly in areas of the device that were electrically isolated from the rest of the structure.

We hypothesise, therefore, that these isolated areas become charged during oxygen plasma which in turn repels the active ions reducing the removal contaminants on the surface. However, as this problem did not occur on the BSOI test wafers, focus was put on the main difference between the these and the C-SOI wafers where the problem occurred. The main difference was cross-sectional area of the anchors attaching the device layer to the Si below the insulating oxide. In the C-SOI, this area was minimised to lower the parasitic capacitance of the anchor. Somehow, this reduction on in cross sectional area was sufficient to significantly reduce the effectiveness of the plasma cleaning. It also explains the reproducibility of the agglomeration pattern on the design.

Since plasma cleaning is the only available solution for cleaning fragile mechanical structures, alternatives to the current fabrication process have been investigated. A possible solution is to replace the PECVD hard mask with a thermally grown oxide to avoid including trace levels of contaminants. It is clear from Figure 8, that the surface of a Si surface after VHF treatment is much cleaner when the hard mask was thermally grown SiO_2 than PECVD SiO_x.

V. Conclusions

Zero-level packaging at wafer level is a compulsory process for commercial MEMS which guarantees higher yield and reliability. Direct Si-Si and Si-SiO_2 is one of the most interesting wafer-to-wafer bond approach due to its high bond strength and the high hermeticity provided. The work

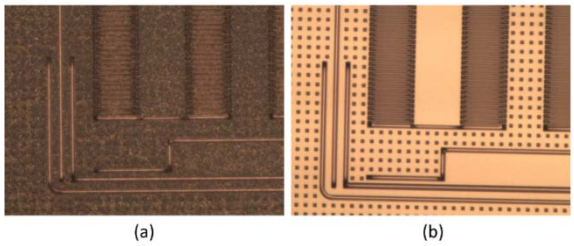

Figure 8: Optical image of residues from a PECVD SiO_2 (a) and thermal SiO_2(b) etched with VHF.

presented in this paper aims to extend the compatibility of wafer level bonding to resonating elements realized with bulk micromachining. Such typology of devices usually is not compatible with the direct bonding mainly due to the wet processes needed for cleaning and activating the surface. The process implemented exploits a SiO_2 to protect the surface while processing and dry processes to both activate and clean the surface. The process was used to bond successfully BSOI wafer but failed to bond C-SOI wafers. This issue is due to particles generated during the plasma cleaning step and needs to be further investigated.

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