Nanotechnology

PAPER • OPEN ACCESS

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To cite this article: Chiara Barri *et al* 2020 *Nanotechnology* **32** 025303

OPEN ACCESS
IOP Publishing
Nanotechnology

Nanotechnology **32** (2021) 025303 (9pp)
https://doi.org/10.1088/1361-6528/abbdda

Engineering of the spin on dopant process on silicon on insulator substrate

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Received 11 July 2020, revised 19 September 2020
Accepted for publication 2 October 2020
Published 20 October 2020

Abstract

We report on a systematic analysis of phosphorus diffusion in silicon on insulator thin film via spin-on-dopant process (SOD). This method is used to provide an impurity source for semiconductor junction fabrication. The dopant is first spread into the substrate via SOD and then diffused by a rapid thermal annealing process. The dopant concentration and electron mobility were characterized at room and low temperature by four-probe and Hall bar electrical measurements. Time-of-flight-secondary ion mass spectroscopy was performed to estimate the diffusion profile of phosphorus for different annealing treatments. We find that a high phosphorous concentration (greater than 10^{20} atoms cm^{-3}) with a limited diffusion of other chemical species and allowing to tune the electrical properties via annealing at high temperature for short time. The ease of implementation of the process, the low cost of the technique, the possibility to dope selectively and the uniform doping manufactured with statistical process control show that the methodology applied is very promising as an alternative to the conventional doping methods for the implementation of optoelectronic devices.

Keywords: spin on dopant, four-probe, SOI doping, P diffusion, ToF-SIMS

(Some figures may appear in colour only in the online journal)

1. Introduction

The functionality of semiconductors relies strongly on the impurities that can be added to the intrinsic materials to change their electrical, physical, and optical properties. Uniform doping to realize ultrashallow junctions at transistor-like device source and drain has been a key point of the effort toward device scaling [1–3]. In traditional semiconductor device fabrication, the doping is carried out using mainly three methods: ion implantation, *in situ* co-deposition, or doping furnaces. Ion implantation is an excellent process that allows high level of control on both the dose of implanted impurity atoms and the implantation depth [4–6]. However, the conventional ion implantation process, which relies on the bombardment of semiconductors with energetic ions, is incompatible with nanostructured materials, such as one-dimensional (1D) nanowires. Furthermore, it induces severe crystal damage which requires also an annealing step to reconstruct the crystal and activate the implanted impurities. Very high temperature are usually needed, limiting its applicability to platforms that can substain high thermal

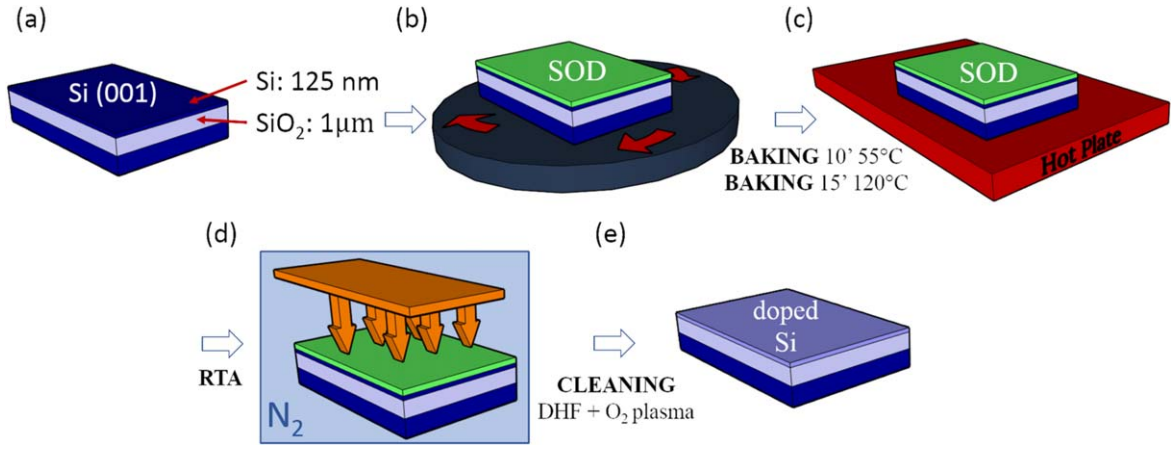

Figure 1. Representation of the doping treatment using SOD P508. (a) SOI wafer sketch; (b) SOI wafer spin coated with SOD P508; (c) annealing steps on a hot plate; (d) activation of the diffusion of P using the RTA treatment; (e) doped sample after the cleaning procedure.

budget processes. These aspects make ion implantation a delicate and costly process. In co-deposition techniques, such as chemical vapor deposition (CVD), the dopant is directly introduced in the growth chamber by a carrier gas [7–10]. This approach offers an excellent control of the dopant concentration and solubility, which can be tuned by changing the vapor pressure of the source and the temperature of the substrate during the thin films deposition. However, in CVD method the presence of toxic and explosive gases requires many safety precautions, making it an expensive and dangerous technique. Moreover, this approach lacks spatial control as it affects homogeneously the full wafer surface. In doping furnaces, doping is achieved by exposing the wafers to a flux of dopant atoms from the sublimation/evaporation of a solid/liquid source or from a gas source. Dopant diffusion into the substrate is promoted by heating the wafers for the time needed to achieve the desired doping profile. Typically, doping furnaces can be hosted only in large facilities and can accommodate a large quantity of substrates. However, due to the hazardous nature of the dopant sources, this step often requires a very long time in a controlled environment [11, 12].

To overcome the difficulties of conventional technologies and their correlated costs, tremendous research efforts have been taken in recent years to develop new strategies for introducing dopants into semiconductor materials such as monolayer doping [13–16] or spin on dopant (SOD) [17–23]. In this work we applied a SOD treatment with rapid thermal annealing process (RTA) to drive-in the dopants from the SOD polymeric film into the silicon substrate, without modifing the surface energy, requiring covalent attachment methods, such in surface-initiated polymerization [2] and grafting of functionalized polymers [24, 25]. The SOD film provides an impurity source for semiconductor junction fabrication, and due to the convenience and simplicity of use, it greatly reduces the reliance on the traditional facilities for doping diffusion. SOD based treatments have become increasingly popular due to their simple, uniform doping profile, high yields, and possibility to introduce both n- and p-type doping [26, 27]. The advantage of SOD over the aforementioned methods relies in its low cost, simple control of the process and its adaptability to different platforms, achieving a uniformity of the coated film on large substrates. Moreover, it eliminates the need for dangerous gases and their related safety precautions, it is more environmentally friendly, and reduces manufacturing costs. Additionally, unlike CVD method and furnace-based doping approaches, the SOD process allows selective doping via lithographically patterned areas, similarly to ion implantation [28]. The possibility of diffusing the SOD only in specific areas is very interesting for new nanoelectronic applications: for instance, in the fin field effect transistor the channel has not to be doped, giving the gate higher ability to control threshold voltage, which is a very important property when the transistor is scaling down, while the source and drain regions can be doped locally by SOD process. Here, we have targeted high doping levels -even though perfectly localized- to address the needs of FinFET devices for plasmonic and quantum applications [29, 30]. Clearly, such devices will not be the only perspective potentials of applications, but the necessity of having a high level of localized doping, makes them one of most challenging devices.

In this work we systematically investigate the diffusion of phosphorous from a SOD source in silicon on insulator (SOI) wafers, RTA treatments are performed using different temperatures and process times, leading to the optimization of the desired final doping concentration. By a systematic analysis of the electrical characterizations, the values of P diffusion electrically activated, the doping and mobility were extracted and compared with the chemical P diffusion obtained through time of flight secondary ion mass spectrometry (ToF-SIMS) analyses measurements, demonstrating a successful control of dopant diffusion on SOI susbtrates. At the end, a localized doped Si-based nanodevice is tested as validation of the SOD procedure.

Table 1. Parameters of the rapid thermal annealing treatments of all the samples analyzed. Series A–B–C–D–E samples used for four-probe measurements: for a fixed temperature, different annealing times have been characterized, keeping the ramp up (9 s) constant. Series G samples used in ToF-SIMS analyses. Series H samples used for mobility measurements.

Sample	Annealing treatment	
	Temperature (°C)	Time (s)
A1	860	10
A2	860	20
A3	860	30
A4	860	60
A5	860	90

Sample	Annealing treatment	
	Temperature (°C)	Time (s)
B1	880	10
B2	880	20
B3	880	30
B4	880	60
B5	880	90

Sample	Annealing treatment	
	Temperature (°C)	Time (s)
C1	900	10
C2	900	20
C3	900	30
C4	900	60

Sample	Annealing treatment	
	Temperature (°C)	Time (s)
D1	915	10
D2	915	20
D3	915	30
D4	915	60
D5	915	90

Sample	Annealing treatment	
	Temperature (°C)	Time (s)
E1	920	10
E2	920	20
E3	920	30

Sample	Annealing treatment	
	Temperature (°C)	Time (s)
G1	900	5
G2	900	10
G3	900	20
G4	915	5
G5	915	10
G6	915	20

Sample	Annealing treatment	
	Temperature (°C)	Time (s)
H1	900	30
H2	915	10
H3	930	90

2. Methods

The optimization of the SOD treatments was carried out using a (001) SOI substrate, featuring a 125 nm thick Si layer on a 1 μm buried oxide (BOX) (figure 1(a)). After a cleaning process (ultrasonic treatment with acetone, isopropanol, and N-methyl-2-pyrrolidone) the SOI wafers were spin-coated with the commercial SOD P508 (composition: 8% P and 5% SiO_2) for 30 s at speed of 3000 rpm (figure 1(b)). This process was carried out in a temperature and humidity-controlled environment to prevent cloudiness of the SOD layer. To evaporate the volatile solvent contained in P508, the samples were baked on a hot plate at 55 °C for 10 min and then at 120 °C for 15 min (figure 1(c)). The two baking steps were necessary to avoid cracking of the SOD film. The diffusion of the dopant in silicon was performed by RTA. Different annealing temperatures and times were tested to study the behavior of the diffusion profile and the resulting doping level as reported in table 1. In each process the RTA system ramped up in 9 s to the annealing temperature, which was maintained for process times in the 10–90 s range. The samples were cooled down in a controlled way by flowing the N_2 in the chamber (figure 1(d)). The remaining SOD layer was removed by rinsing in a HF solution (5% vol) for 1 min, followed by an oxygen plasma asher treatment for 30 min at 1000 W to remove any organic contamination. A final HF rinse (5% vol) for 30 s (figure 1(e)) is performed to remove any SOD residues. The reproducibility of the process was validated by processing three different samples batches. After the doping treatment by SOD and the cleaning of the samples, devices for four-probe measurements and Hall bar shaped devices were fabricated (figure 2). The four-probe devices fabrication includes just one step of optical lithography, where a positive resist is patterned before the metal deposition. The metallic contacts were obtained by electron beam evaporation of 7 nm of Ti, 50 nm of Au and 100 nm of Al followed by a lift-off process (figures 2(g), (h)). The Ti was used as a prime to increase the adhesion of Au to the Si substrate, Al allowed us to increase the final thickness of the metals to facilitate the bonding. The Hall bar shaped devices consist of a mesa, patterned by optical lithography and transferred to the substrate by dry etching (CF_4 plasma), (figure 2(b)). Specifically, the adhesion promoter TI PRIME was spin-coated at 3000 rpm for 5 s, then the positive resist AZ 5214E was spin-coated in two different steps at 750 rpm for 5 s and at 4000 rpm for 40 s. After the optical lithography, the samples were dipped for 15 s in dilute HF to remove the native oxide layer on the surface right before the contacts deposition. Finally, to obtain ohmic contacts we performed the same procedure reported for the four-probe devices. To improve the quality of the contacts, by lowering the contacts resistivity, the samples were annealed in a furnace at 300 °C for 180 s [31]. Samples were characterized electrically according to the Van der Pauw method [32], and carrier density and Hall mobility were extracted from Hall effect measurements. This electrical characterization was carried out using a permanent magnet creating a 0.204 T magnetic field at room temperature, and an electromagnet which applied a magnetic field ranging from 0 to 1 T at 3 K with an accuracy of 3 mK. The temperature has been measured with a Cernox® negative temperature coefficient RTD made of ceramic oxy-nitride. The phosphorous profile was obtained by ToF-SIMS analyses operating in negative mode and sputtering an area of 500×500 μm^2 using Cs^+ ions at 1 keV and an area of 50×50 μm^2 using Ga^+ ions at 25 keV. Phosphorous quantification was performed according to a calibration procedure that was widely discussed in a previous paper [33]. Finally, by a combination of electron beam lithography and reactive ion etching a Si-based nanodevice using the same SOI substrate before descripted is realized: a SiO_2 hard mask is

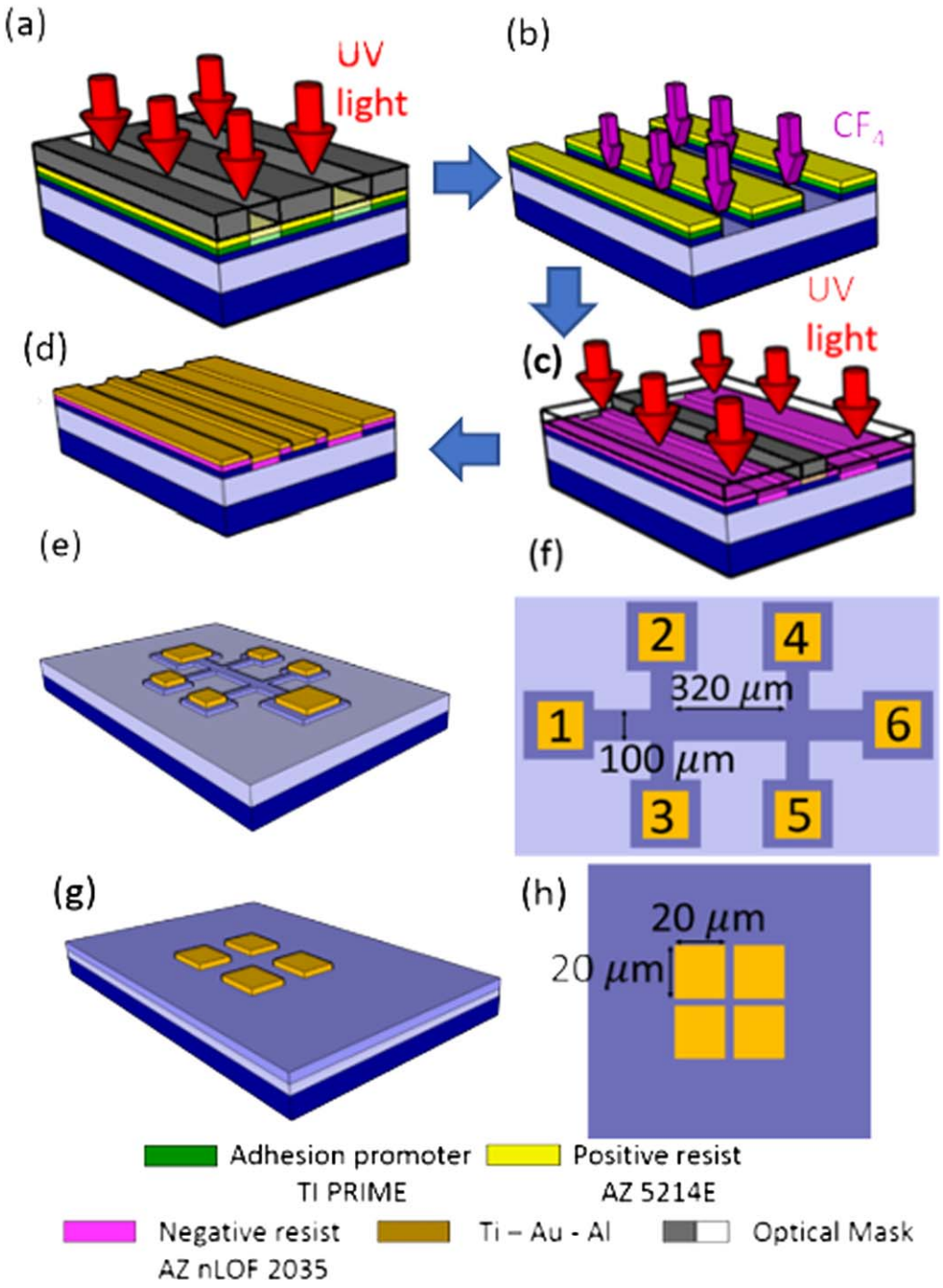

Figure 2. Representation of the fabrication steps. (a) UV exposure of the spin-coated sample; (b) after development, the Si layer is etched by CF_4 plasma; (c) second exposure using a negative resist (d) metal evaporation. (e), (f) 3D representation and plan view of the Hall bar structures: contacts 2–4 and 3–5 are used for longitudinal voltage, contacts 2–3 and 4–5 for transverse voltage measures; (g), (h) 3D representation and plan view of the contacts used for four-probe.

realized and the SOD spincoated in selective areas. The I/V characterization at room temperatures has been carried out to confirm the localized doping optimized by SOD treatment.

3. Results

The doping concentration N_D was obtained by measuring the resistivity ρ of each sample with the dual configuration four-point probe method [34]. The two resistances R_A and R_B associated with the corresponding contacts are reported in figure 3. From these characteristic resistances the sheet resistance R_S and the electrical resistivity ρ can be obtained by:

$$R_S = 2\frac{\pi}{\ln(2)}\frac{R_A + R_B}{2}, \tag{1}$$

$$\rho = R_S x_{\mathrm{Si}}, \tag{2}$$

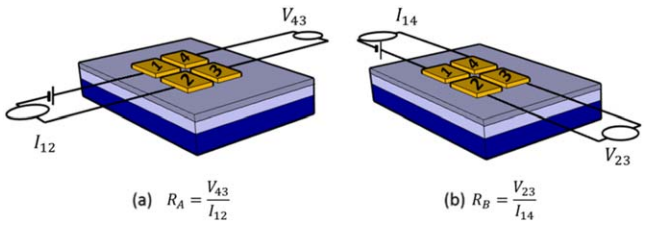

Figure 3. Schematic representation of the electrical measurement of the four-probe configuration for the characteristic resistance (a) R_A and (b) R_B.

Table 2. Parameters used in equation (5) [30].

$\mathbf{A_0}$	$\mathbf{A_1}$	$\mathbf{A_2}$	$\mathbf{A_3}$
−3.0951	−3.2303	−1.2024	−0.13679
$\mathbf{B_0}$	$\mathbf{B_1}$	$\mathbf{B_2}$	$\mathbf{B_3}$
1	1.0205	0.38382	0.041338

where x_{Si} is the thickness of the conductive layer [35]. In this analysis, the top Si layer (x_{Si} = 125 nm) is considered completely and homogeneously doped, neglecting that P atoms have a limited penetration depth as detected by the ToF-SIMS analyses reported below. Since the contacts were positioned in the middle of the sample and not in the corners of a square sample, a correction factor of 2 (in the equation (1)) is reported in the numerator in the classical Van der Pauw configuration [36]. The model described by Thurber *et al* was used to find concentration using the measured resistivity [37]. According to this model it is possible to define a parameter x as the logarithm of the ratio between the measured resistivity ρ and the normalization value $\rho_0 = 1\ \Omega$ cm

$$x = \log\left(\frac{\rho}{\rho_0}\right) \tag{3}$$

and the quantity P as the product between the electronic charge q, the measured resistivity ρ and the electrically active doping density N_D:

$$P = q\rho N_D. \tag{4}$$

Then, solving equation (5) using the parameters reported in table 2 and the normalization factor P_0 equal to 1 V s cm^{-2}:

$$\log_{10}\left(\frac{P}{P_0}\right) = \frac{A_0 + A_1x + A_2x^2 + A_3x^3}{B_0 + B_1x + B_2x^2 + B_3x^3} \tag{5}$$

the doping concentration N_D is obtained from equations (4) and (5):

$$N_D = \frac{10^{\log\left(\frac{P}{P_0}\right)}P_0}{\rho\, q}. \tag{6}$$

The N_D values should be considered as a lower bound of the doping concentration. In fact in the evaluation of the resistivity, we considered the whole thickness of the SOI, 125 nm in our case. Although the Tof- SIMS characterizations (shown below) confirm a gradient of the chemical diffusion of phosphorus, in this analysis we consider a uniform distribution of the electrically active phosphorus because it was not possible to perform four-probe measurements at the various depths levels. By increasing the annealing time and temperature it was possible to obtain a high level of doping in silicon. For an annealing time below 30 s a doping level of 10^{19} atoms cm^{-3} can be achieved at an annealing temperature of at least 880 °C, while on increasing the annealing time to 90 s, the same level can be obtained for annealing temperatures just at 860 °C. The maximum reached dopant density measured by four-probe method is about 7.8 × 10^{19} atoms cm^{-3} for 90 s annealing time at 915 °C.

Considering the samples annealed in the range between 860 °C and 915 °C and characterized by four-probes measurements, the doping concentration is a linear function of the square root of the annealing time as reported in figure 4. This same behavior is predicted by the diffusion model assuming that (1) the Si thickness is few times larger than the diffusion length of the dopant, and (2) the SOD acts as an infinite source of dopant in contact with a semi-infinite medium [38]. Following this model, the doping level is the integral of the diffusion profile of the concentration of dopant normalized with the depth of the Si layer (x_{Si}) in which the dopant diffuses. By applying this model the doping concentration has a linear dependence on the square root of the annealing time:

$$N_D = \frac{1}{x_{Si}}\int_0^{+\infty} c(x,\, t)\mathrm{d}x = \frac{1}{x_{Si}}\frac{2c_0}{\sqrt{\pi}}\sqrt{Dt} \propto \sqrt{t}, \tag{7}$$

where $c(x,\, t) = c_0\,\mathrm{erfc}\left(\frac{x}{2\sqrt{Dt}}\right)$, c_0 being the doping concentration at the SOD/silicon interface, and it is assumed to have a solubility limit of c_0 = 3.5 × 10^{20} atoms cm^{-3} for phosphorus [39]. The doping concentration as a function of the square root of the annealing time is reported in figure 4, where different temperatures have been considered. From the angular coefficient of linear fit of the data m_{fit}, the diffusivity of phosphorus in Si can be calculated:

$$D = \pi\left(\frac{m_{fit}x_{Si}}{2c_0}\right)^2. \tag{8}$$

From the experimental data, the diffusivity values for samples annealed at 860 °C, 880 °C, 900 °C, 915 °C and 920 °C are 1.73 × 10^{-14} cm^2 s^{-1}, 3.15 × 10^{-14} cm^2 s^{-1}, 7.10 × 10^{-14} cm^2 s^{-1}, 9.13 × 10^{-14} cm^2 s^{-1} and 1.34 × 10^{-13} cm^2 s^{-1} respectively. From the data of diffusivity taken from the four-probe measurements, it is possible to extrapolate the value of the activation energy (E_a) of phosphorus diffusion in Si according to the definition of the diffusivity by the Arrhenius equation ($D = D_0e^{-\frac{E_a}{k_BT}}$) where k_B is the Boltzmann constant and T the annealing temperature. From the linear fit of the natural logarithm of diffusivity $\left(\ln(D) = \ln(D_0) - \frac{E_a}{k_BT}\right)$ in function of T^{-1}), the activation energy of 3.88 eV has been obtained. This value is in agreement with the phosphorus activation energy obtained by others using a similar SOD product but other annealing treatments [40, 41]. To characterize the chemical diffusion profile of phosphorous, some ToF-SIMS analyses have been carried out (G series in table 1). The chemical profiles for different species diffused by RTA with various annealing

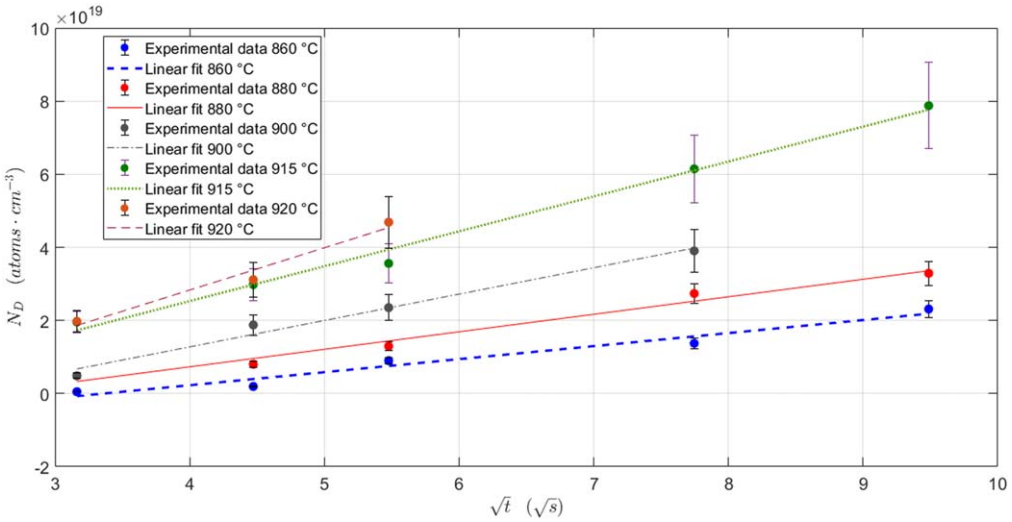

Figure 4. Linear fitting of the experimental data obtained from four-probe measurements of samples annealed at 860 °C (*R*-squared 0.96) blue line, at 880 °C (*R*-squared 0.98) red line, at 900 °C (*R* squared 0.98) gray line, at 915 °C (*R* squared 0.99) green line and at 920 °C (*R* squared 0.97) red line.

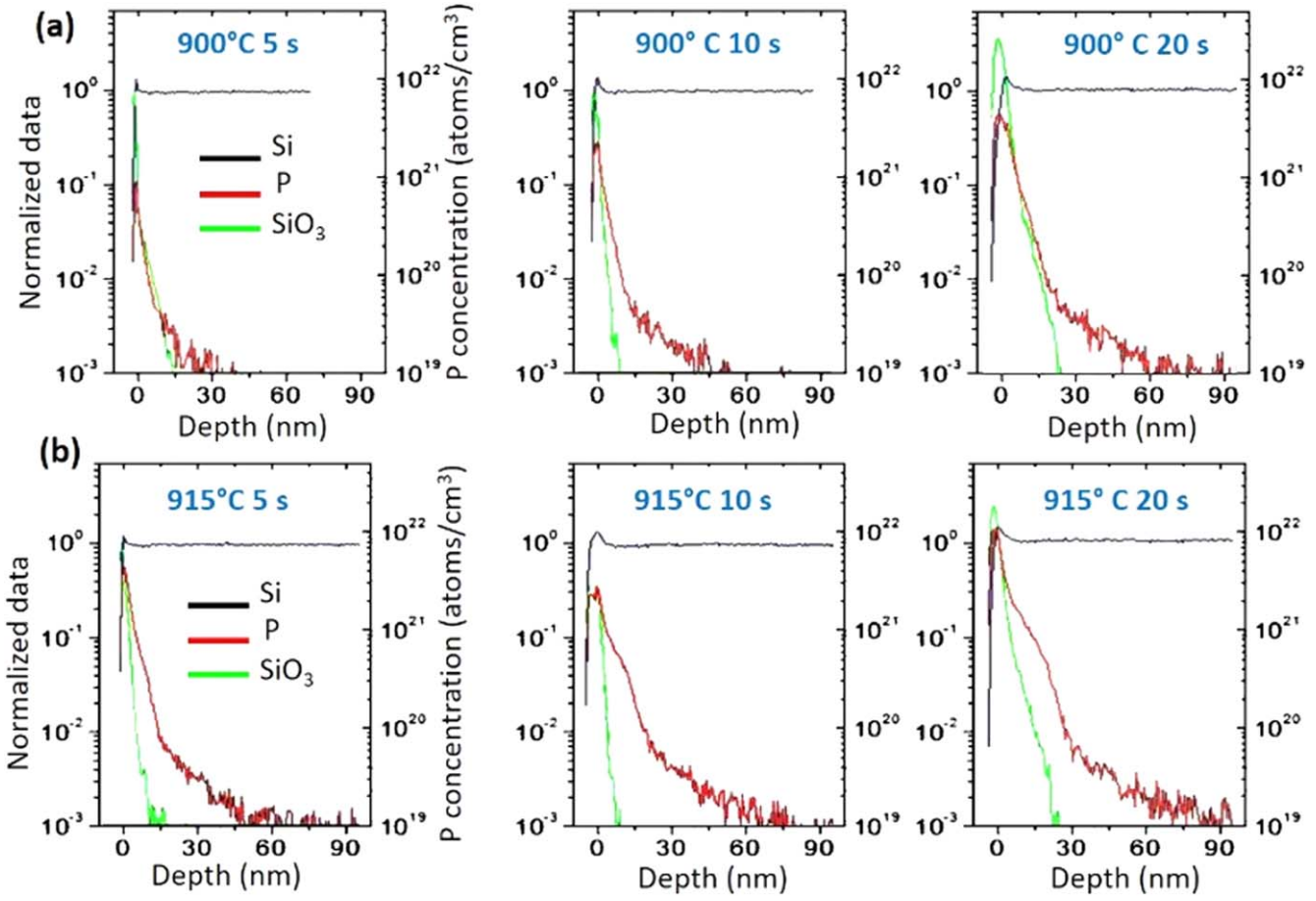

Figure 5. Doping profiles for different chemical species (Si black line—P red line—SiO_3 green line) diffused by RTA with annealing time of 5 s, 10 s and 20 s at the annealing temperature of 900 °C (a) and 915 °C (b).

time and temperatures were compared in figure 5. The longer the annealing time, the higher the concentration of P in the Si substrate was detected. However, by increasing the temperature, oxygen impurities (detected as SiO_3) diffused from the SOD films into the first nm of the silicon film, resulting in the formation of a partially oxidized SiO_x layer in each sample, with a progressively increasing thickness as the annealing time increases, without limiting the electric transport

Table 3. Experimental value of the doping density level and the electron mobility of 3 samples from Hall bar measurements carried out at 300 K and at 3 K.

Annealing Time (s)	Annealing Temperature (°C)	Doping density $\left(\frac{atoms}{cm^3}\right)$		Mobility $\left(\frac{cm^2}{V \cdot s}\right)$	
		300 K	3 K	300 K	3 K
30	900	4.35×10^{19}	5.06×10^{19}	80,2	100,6
10	915	4.9×10^{19}	5.62×10^{19}	72	94
90	930	1.16×10^{20}	1.07×10^{20}	54	89,5

properties as reported by the mobility values in table 3. A phosphorous signal is detected in first 15–30 nm with a relatively long tail extending towards the Si/BOX interface, confirming a gradient of the phosphorous chemical diffusion.

In order to continue the characterization of the samples, Hall bar measurements were performed in order to obtain the doping concentration and the electron mobility. The Hall mobility is obtained from the ratio between the Hall coefficient of the material R_H and the resistivity ρ. By exploiting the six-contact Hall bar geometry, an average value of the Hall coefficient R_H can be obtained in order to limit the negative effects caused by the non-uniformities of the sample. The resistivity ρ, instead, is obtained from:

$$\rho = \frac{V}{I}\frac{Wx_{Si}}{L}, \tag{9}$$

where V is the longitudinal voltage (figure 2(f)), W and L are respectively the width of the conductive channel of the Hall bar and the length between the voltage probes. The measured data are reported in table 3.

The doping concentrations are similar at 300 and 3 K, while the mobility values are higher at low temperature. The main factors that affect the mobility in an extrinsic semiconductor are impurity scattering, phonon scattering, and electron–electron scattering: the role of impurity scattering becomes more important as the doping density increases or when the temperature decreases [42]. According to [43], samples characterized by high doping levels are more difficult to measure and are not particularly affected by the variation of the temperature. The measured mobility values are in agreement with those of silicon samples doped with P using different techniques [44, 45], confirming the validity of doping mechanism with fast and low-cost SOD process. Finally, it is shown the capability of doping selective area through a Si-based nanodevice. From an SOI with a device layer of 145 nm are fabricated four Si pads linked through a 200 nm wide channel as reported in figure 7. To selectively doped two of the four pads (respectively contacts 1 and 3) and to leave the inner nanometric intrinsic channel, a SiO_2 mask is created figure 8. After the SOD doping treatment at 880 °C, an electrical catherization is performed between all contacts. The *I*–*V* curve reported in figure 7(a) shows an ohmic profile between the two SOD doped contacts (contacts 1 and 3), while no current is observed between the undoped ones (pad 2 and pad4), confirming the selective doping validation procedure.

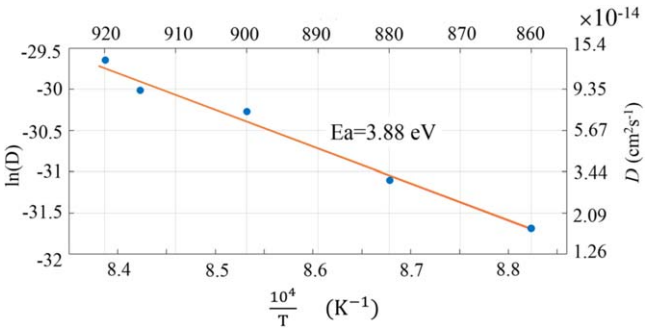

Figure 6. Linear fitting of the natural logarithm of the diffusivity values extrapolated from the experimental data to obtain the phosphorous activation energy.

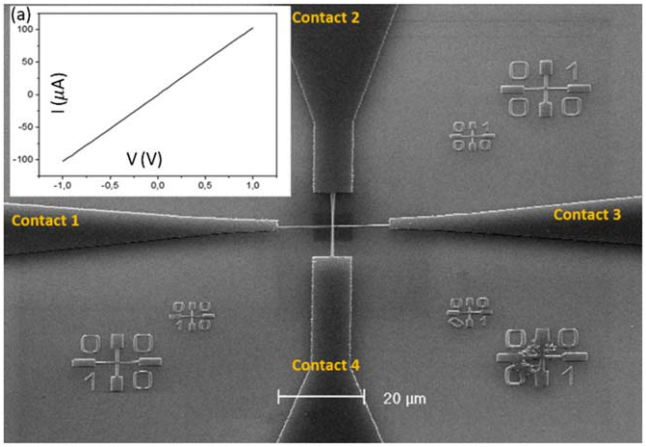

Figure 7. Sem image of the inner part of the four contacts with nanometric intrinsic channel (width 150 nm) before the SOD treatment; (a) ohmic behavior of the device measuring I in function of V between contact 1 and 3. The current reaches value of hundreds of μA.

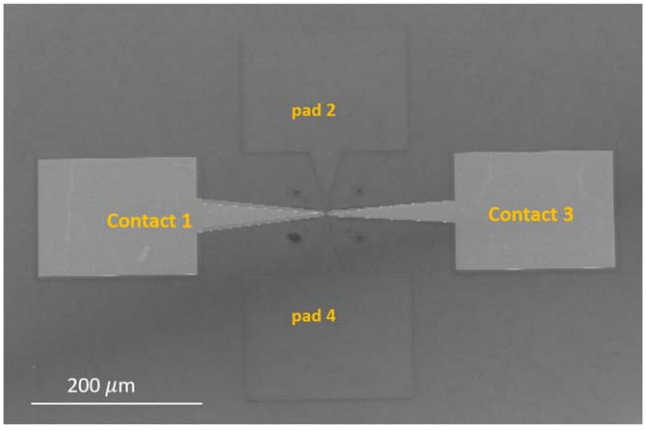

Figure 8. Sem characterization of the SiO_2 hard mask that cover the nanometric channel and all the structures except for the contact 1 and contact 3.

4. Conclusions

In this work, we exploited the spin-on dopant process on SOI wafers. By tuning the RTA treatment parameters, we are able to diffuse the phosphorous into the silicon layer with different

depth profiles. In contrast with the typical doping processes, the SOD diffusion is a low cost process and it does not damage the crystal structure. By electrical characterization at room and low temperatures, the activated phosphorous concentration, the carrier mobility, and P diffusivity have been measured. We show that by SOD treatment, a high level of n-type doping greater than 1×10^{20} atoms cm^{-3} can be reached. The Tof-SIMS analyses reveal that the phosphorous profiles depends to the RTA time. The possibility of doping with high doses, in confined areas and at a low cost is of great interest for quantum devices, Fin-FET and similar devices.

Acknowledgments

We acknowledge the EU H2020 FET-OPEN Narciso (grant no. 828890), the EU ERC Paideia (grant no. 816313), the PRIN NOMEN project (grant no. 2017MP7F8F) and the TEINVEIN project, Call Accordi per la Ricerca e l'Innovazione, co-funded by POR FESR 2014–2020 (ID: 242092).

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