International Journal of Power Electronics and Drive System (IJPEDS)
Vol. 12, No. 1, Mar 2021, pp. 241~248
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v12.i1.pp241-248

Current mode control of single phase grid tie inverter with anti-islanding

Sanjay Lakshminarayanan[1], Kiran Kumar B. M.[2], S. Nagaraja Rao[3], Pranupa S.[4]
[1]Department of Electrical and Electronics Engineering, BMS Institute of Technology, Bangalore, India
[2, 3, 4]Department of Electrical Engineering, Ramaiah University of Applied Sciences, Bangalore, India

Article Info

Article history:

Received Jun 10, 2020
Revised Jan 15, 2021
Accepted Feb 5, 2021

Keywords:

Anti-islanding
Average current mode control
Current hysteresis control
Constant frequency control
Phase locked loop
Total harmonic distortion

ABSTRACT

The aim of this paper is to explore the use of various current mode control (CMC) techniques to design a single phase grid tie inverter integrated with anti-islanding protection. Three types of CMC techniques have been discussed, namely current hysteresis control (CHC), constant frequency control (CFC) and average current mode control (ACMC). The performance of the grid tie inverter in the event of grid voltage failure is also studied to help install an anti-islanding mechanism. The proposed control techniques shall eliminate the use of Phase locked loop (PLL) control as the current reference is generated from the grid voltage itself. All three current mode control techniques of an inverter have been simulated in MATLAB/Simulink to evaluate the performance of the designed inverter. The simulated results show a current THD of less than 5% in all three methods and a good anti-islanding response.

This is an open access article under the CC BY-SA license.

Corresponding Author:

Sanjay Lakshminarayanan
Professor, Departement of Electrical and Electronics Engineering
BMS Institute of Technology, Bangalore, India
Email: sanjay.laks@gmail.com

1. INTRODUCTION

With the advent of renewable energy sources such as solar and wind energy, there was a need to find new ways of dealing with and utilizing the generated power [1]. One elegant method was to supply this power to the utility power supply grid. This eliminated to a large extent the need for energy saving devices like batteries or pumped storage or SMES etc. Power Electronics plays an important part in this idea, as it provides with the means to transform and efficiently control the power flow from the solar panels or wind generators to the power supply grid [2]-[3].

In the case of large solar plants, three phase inverters are used to convert the DC output of the photovoltaic cells to three phase voltages which are synchronized with the three phase power supply grid and feed power to them [4]-[6]. In the case of wind turbines, energy is generated as AC due to the rotating generators which may be converted into an intermediate DC which is once again fed to the grid by inverters [7]-[10].

Three phase grid tie inverters are controlled using control concepts similar to vector control used to control induction motors. Here "α-β" to "d-q" or "abc" transformations are used to deal with the dynamics of the system [11]. Single phase grid tie inverters are used in smaller solar plants such as roof top installations on domestic sites. This calls for low cost solutions without compromising on the power quality [12].

There is one problem associated with grid tie operation which is "islanding". Normally at the point at which the inverter is connected to the grid, there may be some parallel loads or even other inverters, in which case if the grid fails and is disconnected by breakers, the grid tie inverter continues to supply the loads and

islands albeit at improper magnitudes and phase or frequency. This could result in damage to installations and maintenance personnel. Hence there is a need for an "anti-islanding" mechanism [13]-[16].

Traditionally, single phase grid tie inverters are voltage source inverters which have SPWM and a PLL for synchronization with the grid. This approach satisfies the steady state performance, but when the grid supply fails, the anti-islanding schemes behave erratically. What is desired is the steady state power to be supplied to the grid at a required power factor and when the grid fails, the inverter to be shut down and not feed the parallel loads and form islands [17]-[18].

In this paper CMC is suggested instead of the voltage mode of operation of the traditional single phase grid inverter [19]-[20]. CMC may be used to operate the inverter at unity power factor with the current reference drawn from the grid voltage itself thus requiring no PLL [21]. This also suggests that the anti-islanding may be almost automatic. First it must be confirmed if the current THD supplied to the grid is within limits during normal operation. In this paper the parallel load consists of a 1 KW resistive UPF load.

The first method employed is current hysteresis control, also known as tolerance band current control. This is easily done with a MOSFET H-bridge connected through an inductor to the grid supply [22]. Current through the inductor may be sensed using a hall-effect current sensor. It was seen that with a proper hysteresis or tolerance band, a sinusoidal current waveform with a frequency of 50 Hz is generated which is injected to the grid through the inductor. The hysteresis component is seen as a saw tooth like waveform riding on the fundamental, which has to be adjusted so that the THD is less than 5%. The switching frequency varies and depends on the tolerance band. Another non-linearity is the dead time between the upper and lower switches of the H-bridge which could be 1-2 microseconds [23]-[25].

When the grid supply fails in the case of the current hysteresis control the current reference also drops to zero, but the inverter maintains a tolerance band around the zero current level and pumps this to the parallel loads resulting in a low voltage high frequency voltage at the inverter AC side [26]-[28]. This can be detected by an under-voltage relay and can be used for anti-islanding detection and protection.

Another method tried was constant frequency CMC or also known as Peak current control. Here also the grid voltage is used to derive the current reference signal. However, the control method adopted is different from the case of the current hysteresis method. The switches of the H-bridge are turned on at constant frequency, they are maintained on till the current peak rises to the reference value at which point they are switched off and the current drops.

The third method tried was ACMC, here a control voltage is used to vary the duty ratio (PWM) of the switches by comparing with a triangular waveform at switching frequency higher than the fundamental at 50 Hz. The control voltage is derived from a PI control fed with the difference of the average output inductor current and the current reference generated from the grid voltage.

The overall conFigureuration of the system under study is as in Figure.1, the H-bridge consists of IGBTs or MOSFETs, which are unidirectional switches with anti-parallel diodes integrated into them. The grid voltage is also sensed and used in the CMC circuit. No PLL is shown as, unity power factor operation is used with the current reference being derived from the grid voltage waveform, scaled to the required peak current.

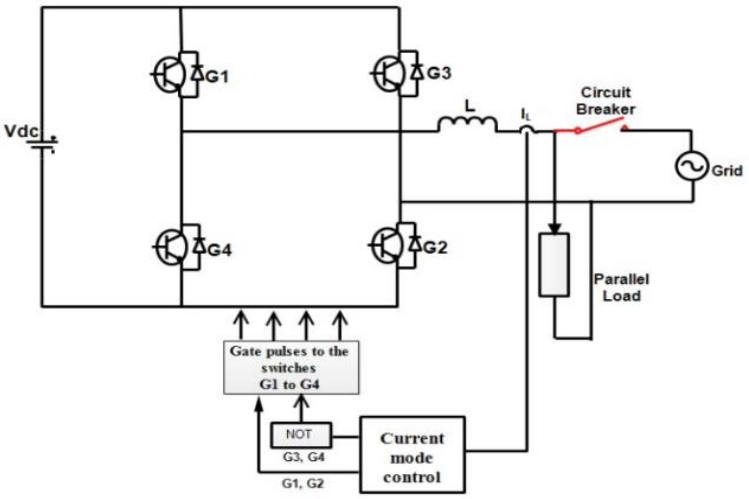

Figure 1. Overall configaration of the single phase grid tie inverter with CMC to be studied

2. ANTI-ISLANDING

Anti-islanding methods can be classified into two categories, active and passive methods. There is what is known as a non-detection zone or NDZ, where the anti-islanding method fails to operate. On the other hand the inverter may be tripped by fluctuations in the grid or parallel loads, even when there is no need for anti-islanding. In passive methods measurements of voltage, current, phase, impedance, frequency and THD are used to detect islanding and circumvent it. In active methods disturbances are added to the inverter output which are detected at the time of islanding. Total elimination of the NDZ is possible using active methods, however they may cause instability in the system. Using current mode in the grid tie inverter seems to suggest that passive techniques can be used in conjunction with them to achieve robust anti-islanding methods.

2.1. Current hysteresis control

CHC is simulated using MATLAB/Simulink. The control circuit is shown in Figure 2. G1, G2 and G3, G4 are the gate signals to the diagonally opposite pairs of the IGBTs or MOSFETS of the single phase bridge inverter in the power circuit. The Input DC voltage is 400 V, the grid voltage is 230 V, 50 Hz. The grid voltage is by itself used to shape the current reference waveform. This ensures unity power factor operation, with no PLL. Currents of 5 A to 10 A, were used to simulate the system. Inductor values from 10mH to 200 mH were used to experiment with. When hysteresis current of +/-200 mA was used with a 50mH inductor, a current output of THD less than 5% was obtained. Figure 3 shows the inductor current using CHC for the reference current of 5 A.

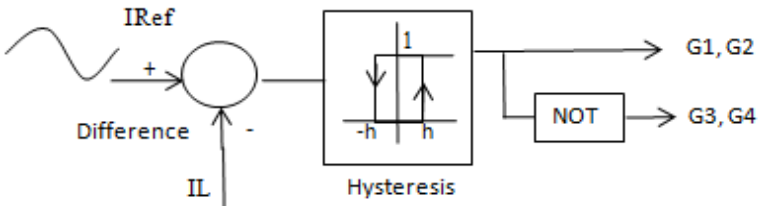

Figure 1. Control circuit for CHC

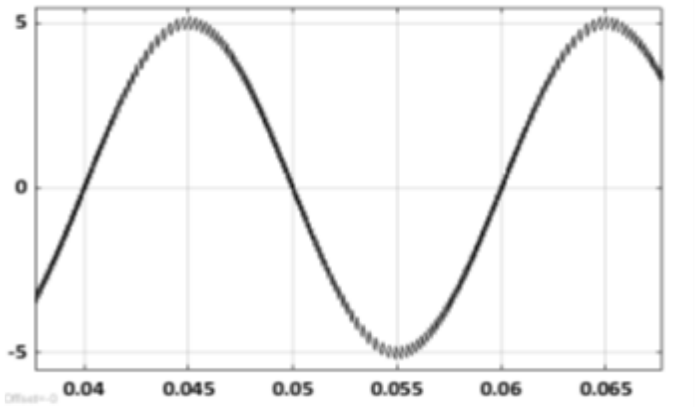

Figure 3. 5A inductor current generated using CHC

The switching frequency varies which is the main disadvantage of CHC. The switching frequency at the peak of the current reference can be calculated theoretically using the Figure 4. During the upward slope of the inductor current, the following approximation can be made knowing that the switching frequency is much larger than 50 Hz, the fundamental frequency of the current reference.

$$L\frac{di}{dt} = 400\,V - 325\text{ V} \quad (1)$$

During the downward slope the equation is as (2):

$$L\frac{di}{dt} = -400\,V - 325\text{ V} \quad (2)$$

Solving this for an inductance of 100 mH, and a hysteresis of ±200 mA, gives t1 and t2, the total period being t1+t2, the reciprocal being the switching frequency during the peak of the current reference. $t1 = 533.3\ \mu s, t2 = 55.2\ \mu s$ which gives a switching frequency of 1.7 KHz. If similar equations were written for the half way point when the grid voltage is 162.5 V, a frequency of 4.1 KHz is obtained. (Though more approximate).

When the circuit breaker is opened, simulating loss of grid voltage, the current reference becomes zero. However, the hysteresis current controller continues to pump a ±200 mA as there is a path for the flow of current from the DC voltage of 400 V, through the switches, inductor and into the parallel load. So, there is a voltage across the parallel load due to the hysteresis band of current of ±200 mA, albeit at a high frequency say 10 KHz, compared to the normal 50 Hz. This behaviour may be used to shut down the inverter by halting the gate signals to the switches in the single phase bridge. A very reliable anti-islanding method may be developedusing this phenomenon. A simple under-voltage relay may be calibrated to establish anti-islanding protection. Figure 5 shows the voltage across the parallel load using CHC during grid failure.

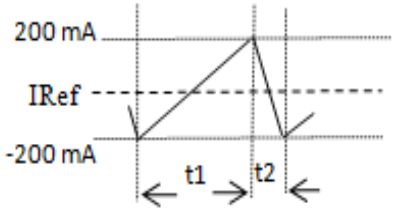

Figure 4. Current ripple in CHC

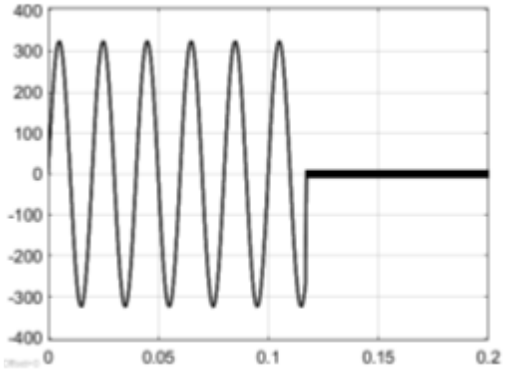

Figure 5. CHC, grid failure at 117 ms, voltage across parallel load

2.2. Constant Frequency Current Mode Control

The control circuit of CFC mode control, also known as peak CMC is shown below in Figure. 6. The following details are used in the simulation. The current reference is derived from the grid voltage scaled to the peak current required. So, this results in unity power factor operation and needs no PLL. The inductor current "I_L" may be sensed by a hall-effect current sensor. The input DC voltage Vdc is 400 V. The grid voltage is 230 V, 50 Hz. A constant switching frequency of 10 KHz is used to produce pulses. A switch pair is turned on when the high frequency clock pulse goes to the "set" (S) input of the SR flip-flop. When the current rises and its peak equal and just exceeds the current reference, the comparator produces a "reset" (R) pulse to the flip-flop which turns of the switches. The current decays till the next "set" pulse from the clock upon which the whole cycle repeats. G1 and G2 are controlled during the positive cycle of the grid voltage and G3, G4 are controlled during the negative cycle of the grid voltage. Slope compensation is added to the current reference to prevent sub-harmonic oscillations. A resettable integrator is used to generate slope compensation.

Figure 2 shows the inductor current in CFC mode control. A current THD lesser than 5 % is achieved when the inductor is chosen to be 50 mH. So, the method may be used legitimately. When the circuit breaker is opened, the grid voltage is removed and the current reference becomes zero. However, there is a path for inductor current to flow through the parallel load. Some low current high frequency oscillations are observed during this period which is shown in Figure 8, possibly due to the slope compensation circuitry. The voltage across the parallel load is shown in Figure 9 by considering an impedance of 50 ohm in CFC mode control, when the grid is disconnected at 117 ms.

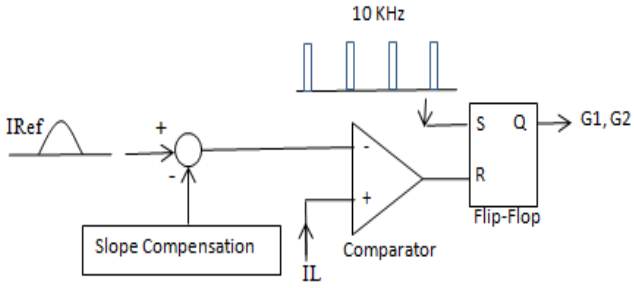

Figure 6. Control circuit for CFC mode control

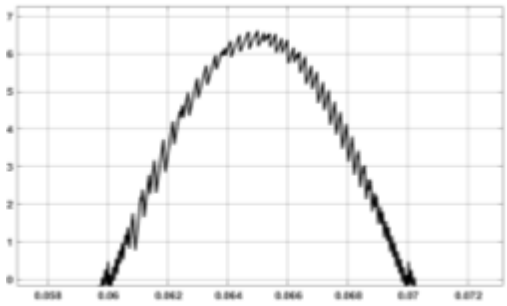

Figure 7. Detailed view of inductor current in CFC mode control

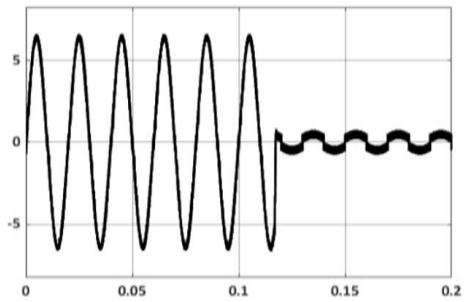

Figure 8. Inductor current, 7 A peak falls when grid fails at 117ms in peak CMC

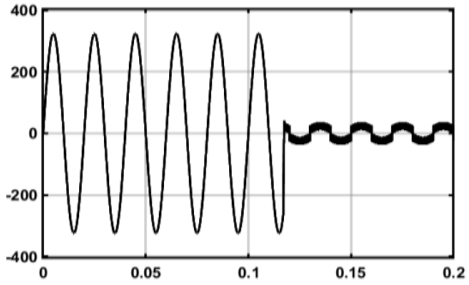

Figure 9. Voltage across parallel load when grid is disconnected at 117 ms in CFC mode control

2.3. Average Current mode Control

The circuit diagram for the control circuit of the ACMC is shown in the Figure 10. It is the most intuitive of the three methods discussed. It is based on the fact that the duty ratio of the switches, determines the rise of the inductor current. This is controlled by a simple feedback control with a PI or proportional-integral control. The only draw back is the tuning of the PI controller. The value of the inductor determines the performance.

Figure 11 shows the inductor current using ACMC A switching frequency of 10 KHz was used. In the simulation a proportional gain of 10 and an integral gain of 2 seemed to work well. The low pass filter used to sense the inductor current was a first order filter with a cut-off of frequency of 1 KHz. A 50 mH inductor gives a current waveform with THD lesser than 5%. Figure 12 shows an inductor current in average current control mode with 10 A reference before and after the grid is shut down at 117ms.

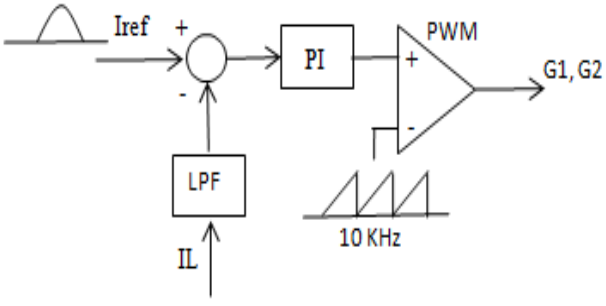

Figure 10. Control circuit of the ACMC

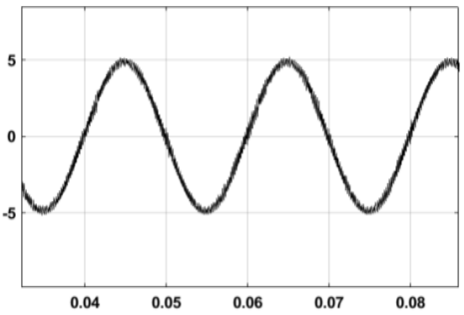

Figure 11. Detailed view of 5A peak inductor current using ACMC

As in the other methods, when the grid voltage fails, low voltage, high frequency oscillations are induced across the parallel load which are quite distinct from the normal grid voltage. This is like an under-voltage situation and can be discriminated as a fault situation quite rapidly.

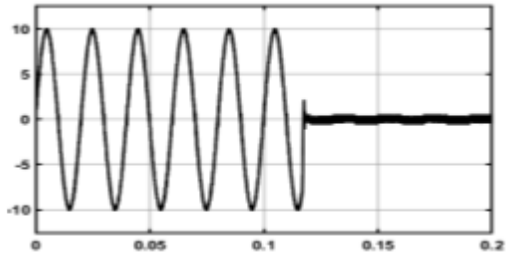

Figure 12. Inductor current in average current control mode control falls at 117ms when grid is shut down

3 IMPLEMENTATION

The power circuit can be implemented with four MOSFETs or IGBTs, and their gate drive circuits. The inductor may be an iron cored type. Currents and voltage sensing can be done using hall-effect sensors which provide excellent isolation of the control circuit from the power circuit which is live. Gate drives should preferably have opto-isolation. The control circuits are built from analog devices such as opamps, comparator, transistors and diodes. Some digital circuits such as SR flip-flops, and other logic gates are also required. In current hysteresis control, the hysteresis may be provided by a Schmitt trigger using an Opamp. Slope compensation in constant frequency current mode or peak current mode can be implemented using Opamps. In ACMC, the PI controller is built using Opamps with resistive-capacitive elements for compensation. ACMC in particular is conducive to an embedded solution using a DSP or microcontroller.

4. CONCLUSION

CMC techniques can be used effectively in grid tie inverters and provide effective anti-islanding features. CMC of grid tie inverter operates at unity power factor without PLL, grid voltage is used to shape current reference waveforms. This paper presents results of three control techniques used in current mode grid tie inverter. The Input DC voltage is 400 V, the grid voltage is 230 V, 50 Hz for all the three current control techniques used. All the three methods can be operated so as to result in current THD less than 5%. CMC results show low current high frequency oscillations when the grid voltage is turned off. ACMC is the most intuitive of the three methods discussed. When the grid voltage fails, low voltage, high frequency oscillations are induced across the parallel load which are quite distinct from the normal grid voltage. This is like an under-voltage situation and can be discriminated as a fault situation quite rapidly. Paper also explains the passive techniques of anti-islanding method during grid failure. This can be used to build low cost single phase grid tie inverters for solar, PV applications at homes and commercial sites.

REFERENCES

[1] Panwar, N. L., S. C. Kaushik, and Surendra Kothari, "Role of renewable energy sources in environmental protection: A review," *Renewable and sustainable energy reviews*, vol. 15, no. 3, pp. 1513-1524, 2011.
[2] Jana, Joydip, Hiranmay Saha, and Konika Das Bhattacharya, "A review of inverter topologies for single-phase grid-connected photovoltaic systems," *Renewable and Sustainable Energy Reviews*, vol. 72, pp. 1256-1270, 2017.
[3] John, Vinod, Zhihong Ye, and Amol Kolwalkar, "Investigation of antiislanding protection of power converter based distributed generators using frequency domain analysis," *IEEE Transactions on Power Electronics*, vol. 19, no. 5, pp. 1177-1183, 2004.
[4] Zhang, Dehua, et al., "High efficiency current mode control for three-phase micro-inverters," *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Orlando, FL, 2012, pp. 892-897.
[5] Kjaer, Soeren Baekhoej, John K. Pedersen, and Frede Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Transactions on Industry Applications*, vol. 41, no. 5, pp. 1292-1306, 2005.
[6] Velasco, David, et al., "Review of anti-islanding techniques in distributed generators," *Renewable and sustainable energy reviews*, vol. 14, no. 6, pp. 1608-1614, 2010.
[7] Wu, Hongying, et al., "A current-mode control technique with instantaneous inductor-current feedback for UPS inverters," *APEC '99. Fourteenth Annual Applied Power Electronics Conference and Exposition. 1999 Conference Proceedings (Cat. No.99CH36285)*, Dallas, TX, USA, 1999, pp. 951-957, vol. 2.

[8] Zare, Firuz, and Gerard Ledwich, "A hysteresis current control for single-phase multilevel voltage source inverters: PLD implementation," *IEEE transactions on power electronic*s, vol. 17, no. 5, pp. 731-738, 2002.
[9] Jianhua, Wang, et al., "Modeling and analysis of hysteretic current mode control inverter," *2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition*, Washington, DC, 2009, pp. 1338-1343.
[10] S. Nagaraja Rao. Kiran Kumar B. M, and Pranupa S., "Three Phase Diode Clamped Multilevel DC Link Inverter with Multi Reference Modulation Techniques." *Journal of Advanced Research in Dynamical and Control Systems*, vol. 10, no. 9, pp.1793-1805, 2018.
[11] Yao, Zhilei, and Lan Xiao, "Control of single-phase grid-connected inverters with nonlinear loads," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 4, pp. 1384-1389, 2011.
[12] Cherati, S. M., et al., "Design of a current mode PI controller for a single-phase PWM inverter," *2011 IEEE Applied Power Electronics Colloquium (IAPEC)*, Johor Bahru, 2011, pp. 180-184.
[13] Manoharan, MohanaSundar, Ashraf Ahmed, and Joung-Hu Park, "Digital implementation of peak current mode control for single-phase H-Bridge inverter with slope compensation," *2013 International Conference on Electrical Machines and Systems (ICEMS)*, Busan, 2013, pp. 1502-1506.
[14] Lamchich, M. R. T., "Average Current Mode Control of a Voltage Source Inverter Connected to the Grid, Application to Different Filter Cells," *Journal of Electrical Engineering*, vol. 55, no. 3-4, pp. 77-82, 2004.
[15] Manoharan, Mohana Sundar, Ashraf Ahmed, and Joung-Hu Park, "Peak-valley current mode controlled H-bridge inverter with digital slope compensation for cycle-by-cycle current regulation," *Journal of Electrical Engineering & Technology*, vol. 10, no. 5, pp. 1989-2000, 2015.
[16] Rajeev, Mini, and Vivek Agarwal, "Single phase current source inverter with multiloop control for transformerless grid-PV interface," *IEEE Transactions on Industry Applications*, vol. 54, no. 3, pp. 2416-2424, 2018.
[17] Rao, S. Nagaraja, D. V. Ashok Kumar, and ChBabu, "Grid Connected Distributed Generation System with High Voltage Gain Cascaded DC-DC Converter Fed Asymmetric Multilevel Inverter Topology," *International Journal of Electrical & Computer Engineering (IJECE)*, vol. 8, no. 6, pp. 4047-4059, 2018.
[18] Rao, S. Nagaraja, D. V. Ashok Kumar, and Ch Sai Babu, "Implementation of Cascaded based Reversing Voltage Multilevel Inverter using Multi Carrier Modulation Strategie," *International Journal of Power Electronics and Drive Systems (IJPEDS)*, vol. 9, no. 1, pp. 220-230, 2018.
[19] Khanfara, M., R. El Bachtiri, M. Boussetta, and K. El Hammoumi. "A multicarrier PWM technique for five level inverter connected to the grid." *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 9, no. 4, pp. 1774-1783, 2018.
[20] Rao, S. Nagaraja, DV Ashok Kumar, and Ch Sai Babu, "Integration of Reversing Voltage Multilevel Inverter Topology with High Voltage Gain boost Converter for Distributed Generation," *International Journal of Power Electronics and Drive Systems (IJPEDS)*, vol. 9, no. 1, pp. 210-219, 2018.
[21] Vadde, Anusha, S. Sachin, and V. V. S. N. Sitaram Gupta, "Real implementation of synchronous boost converter with controller for power factor correction," *2017 IEEE Region 10 Symposium (TENSYMP)*, Cochin, 2017, pp. 1-4.
[22] Kamil, Haval Sardar, et al., "Low-voltage Ride-through Methods for Grid-connected Photovoltaic Systems in Microgrids: A Review and Future Prospect," *International Journal of Power Electronics and Drive Systems (IJPEDS)*, vol. 9, no. 4, pp. 1834-1841, 2018.
[23] Della Krachai, M., K. Melouk, and M. Keddar, "Investigating sine-band hysteresis control of photovoltaic-grid connected inverter," *International Journal of Power Electronics and Drive Systems (IJPEDS)*, vol. 11, no. 2, pp. 969-976, 2020
[24] Hassaine, Linda, and Mohamed Rida Bengourina, "Design and digital implementation of power control strategy for grid connected photovoltaic inverter," *International Journal of Power Electronics and Drive Systems (IJPEDS)*, vol. 10, no. 3, pp. 1564-1574, 2019.
[25] Manjunatha, B. M., et al., "An Optimized Multilevel Inverter Topology with Symmetrical and Asymmetrical DC Sources for Sustainable Energy Applications," *Engineering, Technology & Applied Science Research*, vol. 10, no. 3, pp. 5719-5723, 2020.
[26] Abokhalil, Ahmed G., Ahmed Bilal Awan, and Abdel-Rahman Al-Qawasmi, "Comparative study of passive and active islanding detection methods for PV grid-connected systems," *Sustainability*, vol. 10, no. 6, p. 1798, 2018.
[27] Baghaee, Hamid Reza, et al., "Anti-Islanding Protection of PV-based Microgrids Consisting of PHEVs using SVMs," *IEEE Transactions on Smart Grid*, vol. 11, no. 1, pp. 483-500, 2020.
[28] Yu, Byunggyu, "Anti-islanding performance analysis of multiple PV micro-inverter operations," *IETE Journal of Research*, vol. 64, no. 6, pp. 785-795, 2018.

BIOGRAPHIES OF AUTHORS

Dr. Sanjay Lakshminarayanan is a B.Tech (Hons) from IIT, Kharagpur 1990. He has done his Masters and PhD from the Indian Institute of Science Bangalore. He has 7.5 years of experience in industry and 13 years of experience in academics. He is currently a professor in the Electrical and Electronics Engineering department of BMSIT&M, Bangalore. His area of interest is power electronics and drives.

Kiran Kumar B M is currently working as an Assistant Professor in department of Electrical Engineering at M S Ramaiah University of Applied Sciences, Bengaluru. He is also pursuing Ph.D in the same university. He has three international conferences and three international journal papers to his credit. His research interests in power electronics, renewable energy systems and robotics, he is a student chair of IEEE SB RUAS and graduate student member of IEEE.

Dr. S.Nagaraja Rao is currently working as an Assistant Professor of the Dept. of Electrical and Electronic Engineering, M.S. Ramaiah University of Applied Sciences, Bangalore. He obtained his Ph.D. degree in Electrical and Electronics Engineering, Jawaharlal Nehru Technological University Kakinada, Kakinada, A.P., INDIA. He has published several National and International Journals and Conferences. His area of interest power electronics and Electric Drives.

Ms. Pranupa. S is currently working as Assistant Professor in department of Electrical Engineering at Ramaiah University of Applied Sciences (RUAS), Bangalore. She has been active in IEEE Bangalore Section and also a member of IEEE Power and Energy Society (PES). Her research interest is on renewable energy, robotics, optimization and control.