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A High-Performance Low-Cost Communications System for Small LEO Satellites

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ABSTRACT

In the framework of two nanosatellite projects with European Space Agency a versatile platform consisting of a powerful processor based on a system-on-chip-module with a large field-programmable array (FPGA) and a software-defined radio (SDR) front-end was developed by TU Graz and the SME UniTel. The SDR module covers a frequency range from 300 to 6000 MHz. These two units constitute a flexible transceiver for small LEO satellites, suitable both for LEO-to-ground links, but also for inter-satellite links for LEO constellations. Without extra converters S- and C-band can be accommodated directly. The design was made flexible such that X-, Ku- and Ka-band can be utilised as well by using adapter boards containing the LNAs, SSPAs and frequency converters for these bands. Special care was taken in the PCB layouting to guarantee a very high performance and to minimise EMC effects. UniTel recently developed an add-on module with special hardware encryption. Due to the optimised PCB layouting, the hardware is immune against side attacks. In the framework of the H2020 project EO-ALERT a direct space-ground link in S-band has been defined to transmit alerts generated on board of a novel generation of Earth observation satellites with minimum latency to hand-held terminals used by rescue teams. The size of the modules was chosen to comply with the CubeSat form factor. Industrial COTS electronic components are used in the transceiver. With the support of ESA the systems were extensively tested for total dose radiation at the Co60 test facility at ESTEC and for single-event upsets at the Paul-Scherrer Institute. It was verified that it is safe to operate this transceiver system in a LEO environment for at least two years.

The paper describes the system design of the processor and radio front-end and gives insight in the hardware design criteria for optimised EMC performance. The concept for alert delivery in the EO-ALERT project is presented.

Keywords: software-defined radio, nanosatellites, OPS-SAT, PRETTY, EO-ALERT

1. INTRODUCTION

In the framework of ESA's OPS-SAT project [1], [2] two subsystems were developed: a powerful processing platform based on an ALTERA Cyclone V system-on chip module with a large FPGA and a software-defined radio (SDR) front-end which is closely interconnected with the processor.

In the OPS-SAT project the processor is used for on-board software experiments, in particular to demonstrate novel operational concepts and new protocols, especially the MO (Mission Operations) services as defined by CCSDS. The FPGA of the processor is also used together with the radio front-end as a versatile programmable receiver for communications experiments.

Due to its flexibility it was decided to use the central processor module and an updated SDR front-end for a payload on a CubeSat to demonstrate altimetry utilising passive GNSS reflectometry.

In the framework of the H2020 project EO-ALERT which elaborates the next generation of Earth observation satellites with on-board SAR and optical image processing TU Graz has the task to design the communications subsystem.

In the course of the study the idea emerged to deliver alerts generated on board not only via the high-speed Ka-band telemetry or a relay constellation, but also directly to small hand-held terminals in S-band. For this communications subsystem the SDR/processing platform offers a flexible solution. UniTel IT Solutions, a SME which has been cooperating with TU Graz in the development of the processor and SDR platforms is currently preparing a unique hardware encryption board which provides extremely high data security. The processor, SDR and the encryption platforms constitute a versatile system for a variety of satellite communications applications.

2. PROCESSOR PLATFORM

The Satellite Experimental Processing Platform (SEPP) is a powerful subsystem for advanced space applications.

The SEPP is realized as a very compact printed circuit board (PCB) design with optimum form factor for CubeSat and Nanosatellite missions. Outstanding computational power is achieved by the use of an Altera Cyclone V SX System-on-Chip (SoC) digital logic device with a built-in dual core ARM-9 CPU with 800 MHz clock rate and a Cyclone V Field Programmable Gate Array (FPGA).

A fast DDR3L random access memory (RAM) enables the execution of several high-end software applications and provides sufficient memory for nearly all variants of on-board software (OBSW). By default the SEPP platform is equipped with a Yocto Linux Operating System and several Linux drivers and additional user space software stored on the embedded Multi-Media Controller (eMMC) flash memory.

The SEPP is equipped with high-efficiency DC/DC converters. Power supply monitor and control components protect the system from failures and guarantee a save and reliable system operation.

Special power supply bus switches are used to connect an external supply voltage with the SEPP on-board voltage converters which generate the SoC supply voltage. Data bus switches allow the user to connect one or more SEPP interfaces to the satellite bus or disconnect interfaces if necessary. The concept of power supply and data bus switches provides the possibility to connect several SEPP units to the same external power supply and data bus and allows the establishment of a redundant system in cold redundancy. This means that the SEPP boards can be combined to a stack where one SEPP is activated by enabling the power and data bus switches while the others are disabled and available as spare parts in case of a system failure.

A customized aluminum housing gives additional protection against radiation and provides sufficient area and volume for thermal management. The housing is designed for CubeSat and Nano-Satellite missions and allows a mechanically stable combination of several SEPP boards to a redundant module. Fig.1 depicts the processor board which was implemented as a 22-layer PCB for excellent EMC performance.

Fig.1: Processor Platform

3. SDR FRONT-END

The OPS-SAT SDR platform developed by MEW Aerospace in collaboration with TU Graz was presented at IAC in [2]. This unit used a COTS board (Myriad) augmented by external components such as LNAs and clock generators (Fig.2).

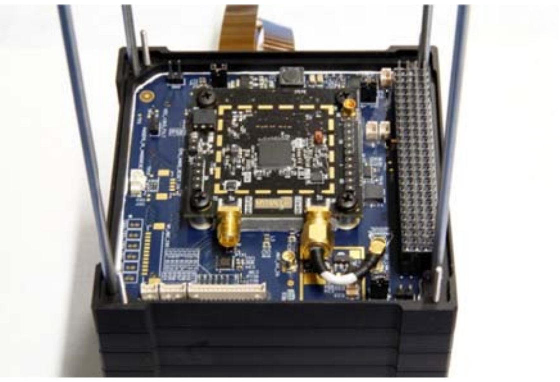

Fig.2: SDR Front-end integrated with processor payload

For a new ESA mission, PRETTY- Passive Reflectometry and Dosimetry [3], which is currently under preparation by RUAG Space Austria, TU Graz and Seibersdorf Laboratories a new front-end is under preparation.

The baseline SDR front-end for the passive reflectometer payload is a design based on the Analog Devices AD9361 transceiver IC. The AD9361 has two broadband RF receivers as well as two broadband RF transmitters The chip provides data connection by parallel LVDS pairs. The chip is a transceiver with continuous coverage of the 70 MHz to 6 GHz frequency range, with a programmable RF bandwidth up to 56 MHz. This is sufficient to fulfil the required (IQ baseband) bandwidth of 14 MHz maximum for operating the passive reflectometry experiment.

For the PRETTY mission only one receiver part of the AD9361 will be used. The receiver is equipped internally with independent and selectable amplifiers, which provide a maximum gain of 71 dB. In addition, an external Low Noise Amplifier (LNA) will be used to further increase the gain of the overall frontend including the antenna to ~105dB.

The SDR RF-front-end module comprises

- an LNA with an optional low-pass filter
- the RF transceiver IC (AD9361)
- a stable reference clock source (TCXO) with an accuracy of <0.5ppm
- the data connection module to the SEPP

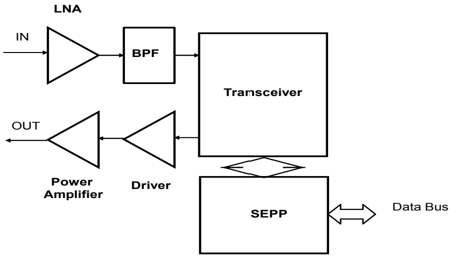

Fig.3: RF Front-end Block Diagram

4. ENCRYPTION

To provide data security a special encryption module has been developed by the company Unitel. Encryption takes place in FPGA hardware on packet level whereby for each packet a different key is used. Encryption is based on a stream cipher and is bit-wise providing very high speed. It is therefore suitable for the delivery of very large files with low latency or real-time HD video.

The depth of encryption is high as 2^{123} bit keys are used.

Special emphasis was put on the PCB design such that side-channel attacks, e.g. by monitoring the electromagnetic emissions of the electronics board, are practically impossible.

A major advantage of the hardware and the algorithms is the very low power consumption in contrast to conventional software solutions.

5. ALERT LINK SYSTEM

In the framework of the H2020 project EO-ALERT [4] a data transmission chain for the delivery of alert messages to small hand-held terminals has been defined.

EO-ALERT is coordinated by DEIMOS in Spain and has partners in Germany (DLR), Italy (OHB Italia, Politecnico di Torino) and Austria (TU Graz). EO ALERT aims at definition an development of the next generation of Earth Observation satellites. Essential data processing functions will be implemented on board of the spacecraft with the aim to deliver EO products within 5 minutes. This avoids the high latency in the convention data acquisition, data processing and dissemination chain.

The architecture features innovative technological solutions, including

- on-board image generation and processing for the generation of EO products and alerts for optical and SAR (synthetic aperture radar) payload missions
- on-board data compression and encryption
- on-board reconfigurable data handling
- high-speed on-board avionics
- reconfigurable high data rate communication links to ground.

Typical applications of the EO-ALERT system are

- ship detection (maritime surveillance)
- severe weather event detection (nowcasting).

The overall communications architecture is shown in Fig.4.

The Ka-band chain operates at data rates up to 2.6 Gbit/s (direct Space-to ground links) and is used for bulk data as well as alert. A typical SAR image has a size of 400 MB, an optical image 200 MB. Alerts are small, only 10 kB per alert. A maximum of 900 alerts are envisaged during an orbit.

The S-band alert chain to hand-held receivers is considered advantageous for rescue teams not having other means to get the data via Internet. It consists of a transmitter with modulator and FEC encoder and an 80 W SSPA feeding a 20 dBi antenna to close the link. The DVB-S2 standard was chosen for modulation and coding. With QPSK and a low-density parity check code (LDPC) only 1.5 dB of signal/noise ratio are needed at the hand-held terminal to provide a virtually error-free channel. The link budget is presented in Table 1.

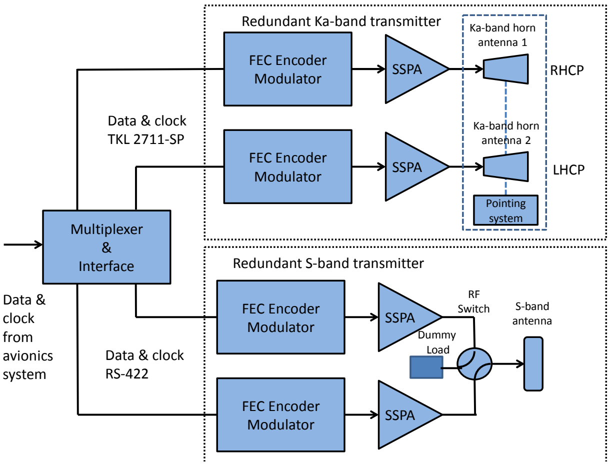

Fig.4: Communications Chain for EO-ALERT Satellites

LINK BUDGET S-BAND		
Input Parameters		
Transmit frequency	2200,00	MHz
Receive Frequency	2200,00	MHz
Distance	2200,00	km
Bandwidth	1000,00	kbit/s
DOWNLINK		
Satellite transmit power	80,00	W
Satellite transmit power	19,03	dBW
Satellite antenna gain	12,00	dBi
Back-off	1,80	dB
Satellite EIRP	29,23	dBW
Free-space loss	166,13	dB
Polarization loss	3,00	dB
Atmospheric loss	0,60	dB
Ionospheric loss	0,70	dB
Pointing loss	0,50	dB
Receive antenna temperature	70,00	K
Input losses	0,10	dB
LNA noise temperature	50,00	K
LNA noise temperature	0,69	dB
Hand-held antenna gain	0,00	dBi
Ground station system temperature	172,63	K
Ground station G/T	-22,37	dB/K
Eb/No at ground station	**4,53**	**dB**
Eb/No required (QPSK/LDPC coding)	1,50	dB
Margin	**3,03**	**dB**

Table 1: S-Band Link Budget

The ground terminal contains an S-band receiver based on the software-defined radio front-end described before which is fed by a double-helix antenna providing hemispherical coverage. Therefore no stringent pointing towards the spacecraft is required. The processor described in section 2 has the following tasks

- Demodulation, FEC decoding and decryption of data
- Display of alerts (text and thumbnail images)

The FPGA has sufficient resources for the demodulation and decoding functions.

Fig.5 shows the coverage and footprint of a nadir pointing S-band antenna with 12 dBi gain.The flight track is in red; limits of the side–looking SAR access range (swath - from 190 km to 460 km) is presented in blue; the 12 km swath of the multispectral optical payload is in green.

Fig.5. Footprint of the S-band Link

It shall be mentioned that in addition to the Ka- and S-band communications chains, the emerging LEO satellite communications systems such as LEOSAT are under consideration for global alert and potentially bulk data transmission. As a short-term solution an INMARSAT L-band solution by ADVALUE is a candidate.

6. INTER-SATELLITE LINKS

In addition to the applications mentioned before, the combination of SDR front-end and powerful processor can be utilised for inter-satellite radio links between small satellites operating in a constellation. Fig.6 depicts the system which can be used as a regenerative or transparent transponder, e.g. in Ka-Band with up- and downconverters from Ka-Band to an "IF" of up to 6 GHz which the transceiver chip can handle. In the case of a transparent transponder the output of the internal A/D converter is simply fed back to the D/A converter.
In case of a regenerative transponder the FPGA of the SoC will implement a demodulator/decoder as well as encoder/modulator.

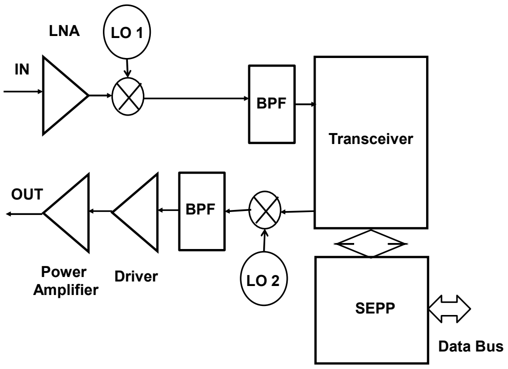

Fig.6: Transponder

7. SUMMARY

A versatile transmission system for small satellites consisting of an SDR front-end and a powerful processor has been presented. A special stream-cipher, low-power encryption system implemented in an FPGAto provides data security. The front-end with processor will be used in ESA's PRETTY altimeter mission and can be used in the context of the H2020 project EO-ALERT for the next generation of advanced Earth Observation satellites.
Another application is for inter-satellite links in small satellite constellations, where the system can be used as transparent or regenerative transponder.

8. ACKNOWLEDGEMENTS

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