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Research Article

Coupling effect in field Hall elements based on thin-film SOI MOS transistors

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Abstract

The influence of the coupling effect on the parameters of field Hall elements based on thin-film MOS transistors has been studied. Analysis of the development of today's microelectronics shows the necessity of developing the element base for high performance sensors based on silicon technologies. One way to significantly improve the performance of sensing elements including magnetic field sensors is the use of thin-film transistors on the basis of silicon on insulator (SOI) structures. It has been shown that field Hall sensors (FHS) may become the basis of high-performance magnetic field sensors employing the coupling effect occurring in the double gate vertical topology of these sensing elements. Electrophysical studies of FHS have been conducted for different gate bias and power supply modes. The results show that the coupling effect between the gates occurs in FHS if the thickness of the working layer between the gates is 200 nm. This effect leads to an increase in the effective carrier mobility and hence an increase in the magnetic sensitivity of the material. Thus field Hall elements based on thin-film transistors fabricated using silicon technologies provide for a substantial increase in the magnetic sensitivity of the elements and allow their application in highly reliable magnetic field sensors.

Keywords

transistor, silicon on insulator, field Hall sensor, charge coupling, magnetic field.

1. Introduction

Over the last decades microelectronics industry has been developing at a fast pace since it is directly related to the development of information technologies, industrial automation and Internet of things which provide for effective control of human life space. Doubtlessly further achievements of microelectronics will only be possible provided the necessary element base is available, with the emphasis of development being on sensors and microsystems for environmental monitoring [1]. Magnetic field sensors are among the most demanded devices in various general-purpose civil and special applications. It is therefore not surprising that the world's fabrication figures of these sensors amount to billions of devices and grow by about 10% annually [2, 3].

Analysis of publications on sensor technologies shows that silicon is the key material in this segment used for the fabrication of the sensing elements of sensors and the infrastructure electronics for the processing of the signals generated by the sensing elements, as well as for overall sensor operation [4, 5].

A tangible improvement in the performance of silicon microelectronic sensors can be achieved, without abandoning silicon technologies, by fabricating the sensing

elements from thin-film silicon field effect transistors with two vertical control gates based on silicon on insulator (SOI) structures [6, 7].

Silicon on insulator (SOI) is an important material of silicon macro- and microelectronics. Currently SOI transistors are widely used for the fabrication of various physical, chemical and biological sensors [8–10]. The advantages of SOI structures for sensors fabrication in comparison with conventional bulk substrate technologies mainly include higher element operation temperatures due to lower leakage currents and new functionalities.

SOI MOS field effect transistors typically have two gates. One is for controlling the carrier concentration in the channel and the other at the substrate side is earthed. A distinctive feature of fully depleted SOI MOS transistors is the coupling effect, i.e., a correlation between the interface potentials of the Si thin film in which the device is fabricated and the surrounding dielectric [11–14]. This coupling effect may lead to a dependence of the SOI layer conductivity on the transistor control gate bias and the substrate metallization voltage.

The aim of this work is to study the effect of gate voltage on the Hall voltage in field Hall sensors (FHS) in the form of magnetically sensitive thin-film double gate SOI MOS transistor with probes at two opposite sides of the *n*-Si channel. The SOI FHS operation principle is electron accumulation at the Si–SiO_2 interface boundaries separated by the partial depletion zone.

2. Experimental

FHS were described in detail earlier [15, 16]. The SOI structures used for FHS fabrication were synthesized by oxygen ion implantation into silicon wafers using the SIMOX technology (Separation by Implantation of Oxygen). The FHS crystal cut from a SOI structure was 500 × 500 × 400 μm in size. The FHS topology in the *n*-conductivity SOI structure silicon layer with an electron concentration of $5 \cdot 10^{14}$ cm^{-3} and 0.2 μm in thickness separated from the substrate by a 0.35 μm SiO_2 buried layer. The 50 × 50 μm current and Hall contact pads were produced by phosphorus ion implantation and annealing to a 10^{20} cm^{-3} concentration in the entire silicon layer depth. Then a 0.35 μm thermal oxide layer was grown on the silicon working layer surface and capped with an Al film. Thus the FHS has a system of two vertical gates for controlling the electrophysical parameters of the device. The FHS design is schematically shown in Fig. 1.

The FHS working principle is electron accumulation at Si–SiO_2 interface boundaries and partial Si channel depletion between the electron accumulating zones of the Si film. For further details see Fig. 2 [17].

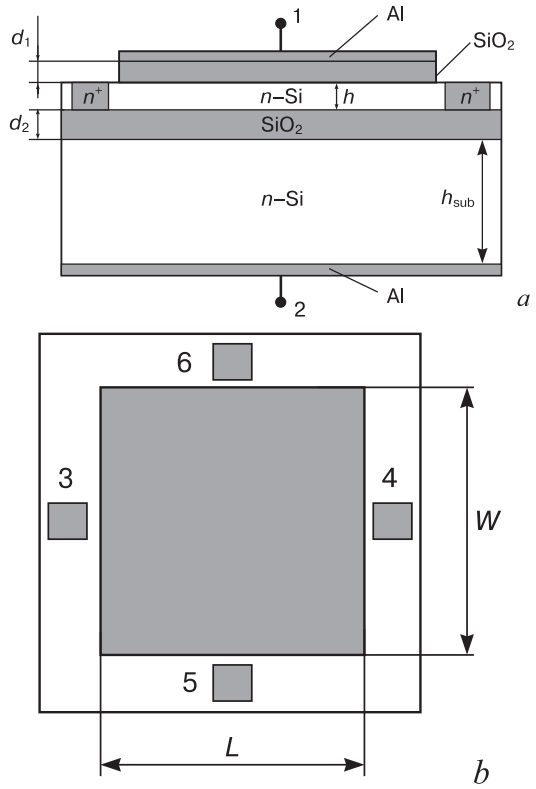

Figure 1. Dimensions and arrangement of SOI FHS elements: (*a*) cross-section and (*b*) top view; (*1* and *2*) top and bottom gate contacts; (*3* and *4*) current (Ohmic) contacts and (5 and 6) side Hall probes.

Parameters: h = 0.2 μm is the working silicon layer thickness, d_1 = 0.35 μm is the top gate dielectric thickness, d_2 = 0.35 μm is the SOI structure buried dielectric layer thickness, h_{sub} = 400 μm is the substrate thickness, L = 500 μm is the silicon channel length and W = 500 μm is the silicon channel width

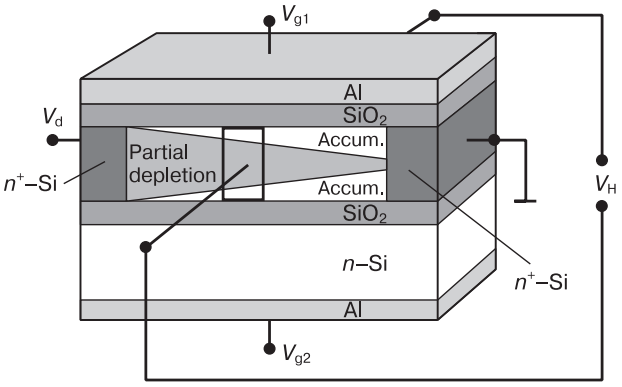

Figure 2. FHS schematic and working principle explanation: V_d is the FHS power voltage, V_{g1} and V_{g2} are the top and bottom FHS gate bias, respectively, and V_H is the Hall voltage read at the Hall probes.

3. Results and discussion

In this work we studied the current and Hall characteristics of the FHS for different gate bias modes: 1) variable bias is applied to each of the gates separately while the other gate has a zero bias and 2) equal bias is applied to both the gates simultaneously. Room temperature experimental curves taken at a 50 mT induction are shown in Fig. 3.

It can be seen from Fig. 3 that applying equal bias V_g to both the gates increases the Hall voltage V_H almost twofold in comparison with single gate bias mode in the

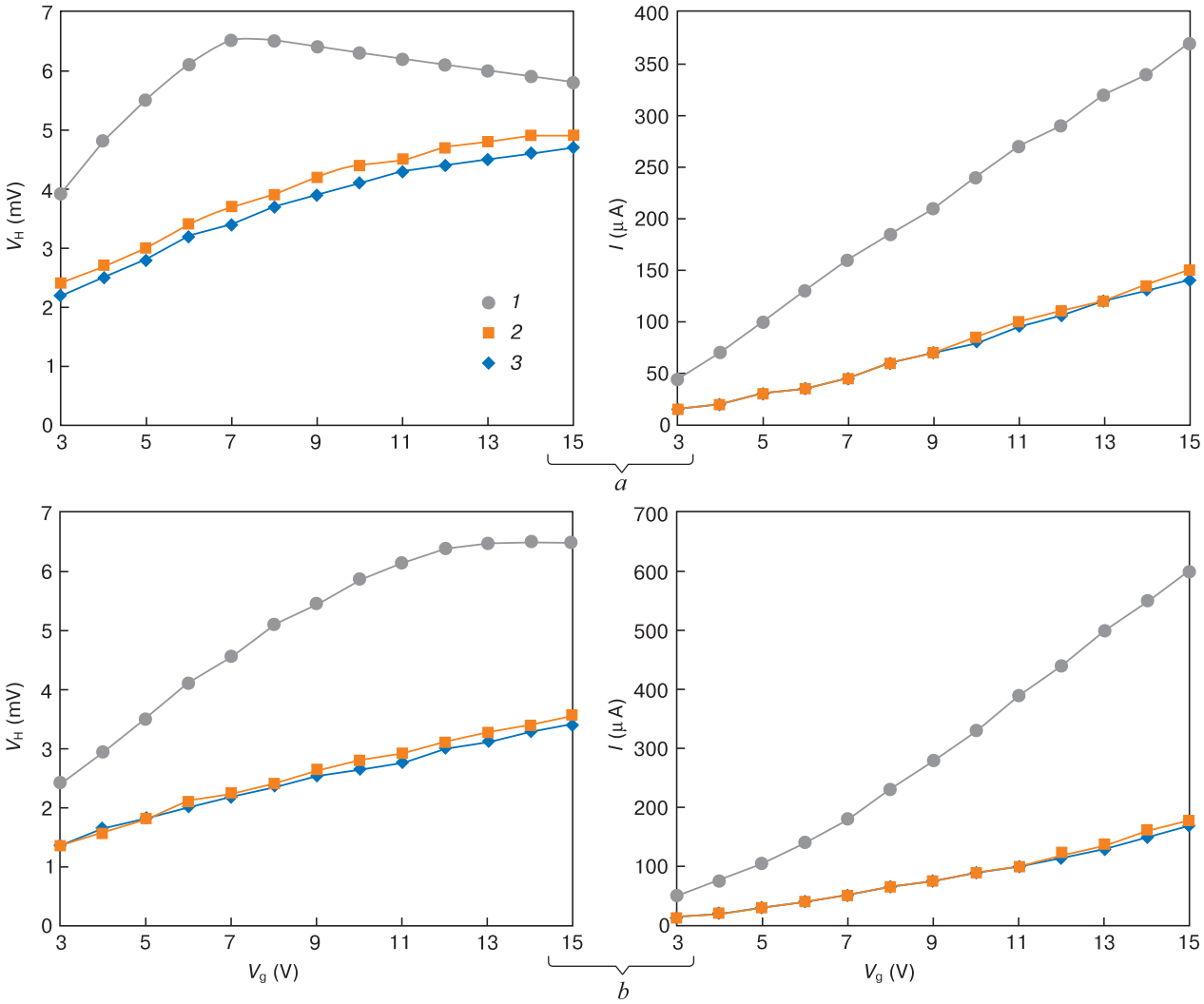

Figure 3. Hall voltage and channel current dependences on gate bias V_g for different gate bias modes and different FHS power voltages V_d at $B = 50$ mT: (*a*): $V_d = 5$ V; (*1*) $V_g = V_{g1}$, $V_{g2} = 0$ V; (*2*) $V_g = V_{g2}$, $V_{g1} = 0$ V; (*3*) $V_g = V_{g1} = V_g$; (*b*): $V_d = 10$ V; (*1*) $V_g = V_{g1}$, $V_{g2} = 0$ V; (*2*) $V_g = V_{g2}$, $V_{g1} = 0$ V; (*3*) $V_g = V_{g1} = V_g$

V_g voltage range studied. One can also point out that the FHS channel current I increases more than twofold when both the gates are switched on. For the entire gate voltage range studied the ratio of the double gate bias channel current to the single gate bias channel current is twice as large as the ratio of the respective Hall voltages, in accordance with the data summarized in the Table 1. There the notations I_{2g} and I_g stand for the channel current for bias V_g applied to both the gates and to one of the gates, respectively. Similarly, the notations V_{H2g} and V_{Hg} stand for the Hall voltage for bias V_g applied to both the gates and to one of the gates, respectively.

The above regularity can be accounted for by the influence of the coupling effect between the gates of the control field effect transistors of the FHS in double gate bias mode. It was shown [18] that for this type of SOI MOS transistors working in interface electron accumulation mode, the charge centroid may shift to the SOI channel bulk. The bulk carrier mobility is always higher than that at the SiO_2–Si interface.

Table 1. FHS channel current and Hall voltage ratios for different gate bias modes.

V_d, V	V_g, V	I_{2g}/I_g	V_{H2g}/V_{Hg}
5	3	3.0	1.6
5	5	3.3	1.8
5	7	3.6	1.7
5	9	3.0	1.4
5	12	2.8	1.4
5	15	2.6	1.3
10	3	3.3	1.7
10	5	3.5	1.7
10	7	3.9	2.0
10	9	4.0	2.0
10	12	3.9	2.0
10	15	3.8	1.9

For a Hall transistor, e.g. an FHS, this may account for the increase in the Hall voltage for double gate bias mode in comparison with single gate bias mode because the contribution of electron scattering at surface states decreases and the effective electron mobility in the channel increases (it is well known that Hall's e.m.f. is proportional to the carrier mobility [19]). The decrease in the Hall

signal when the gate bias is higher than the channel power voltage (Fig. 3) is accounted for by the effect of the transverse electric field on the electron mobility [20].

Regarding the channel current one should bear in mind that the FHS contains two parallel-connected Hall type elements (Fig. 2). Hence there are contributions to the channel current both from the increase in the carrier concentration in the electron accumulation layers at the top and bottom SiO_2–Si interfaces and from the increase in the electron mobility in each of the conducting layers.

4. Conclusion

It was shown that in a field Hall element based on thin-film SOI MOS transistor working by electron accumulation at SiO_2–Si interface boundaries, the coupling effect increases the absolute magnetic sensitivity of the device and thus allows fabricating magnetic field sensors based on SOI transistors. These sensors are suitable for operation in high temperature and radiation environments.

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