Design and Integration of the Readout Electronics for ATLAS Liquid Argon Calorimeter for HL-LHC

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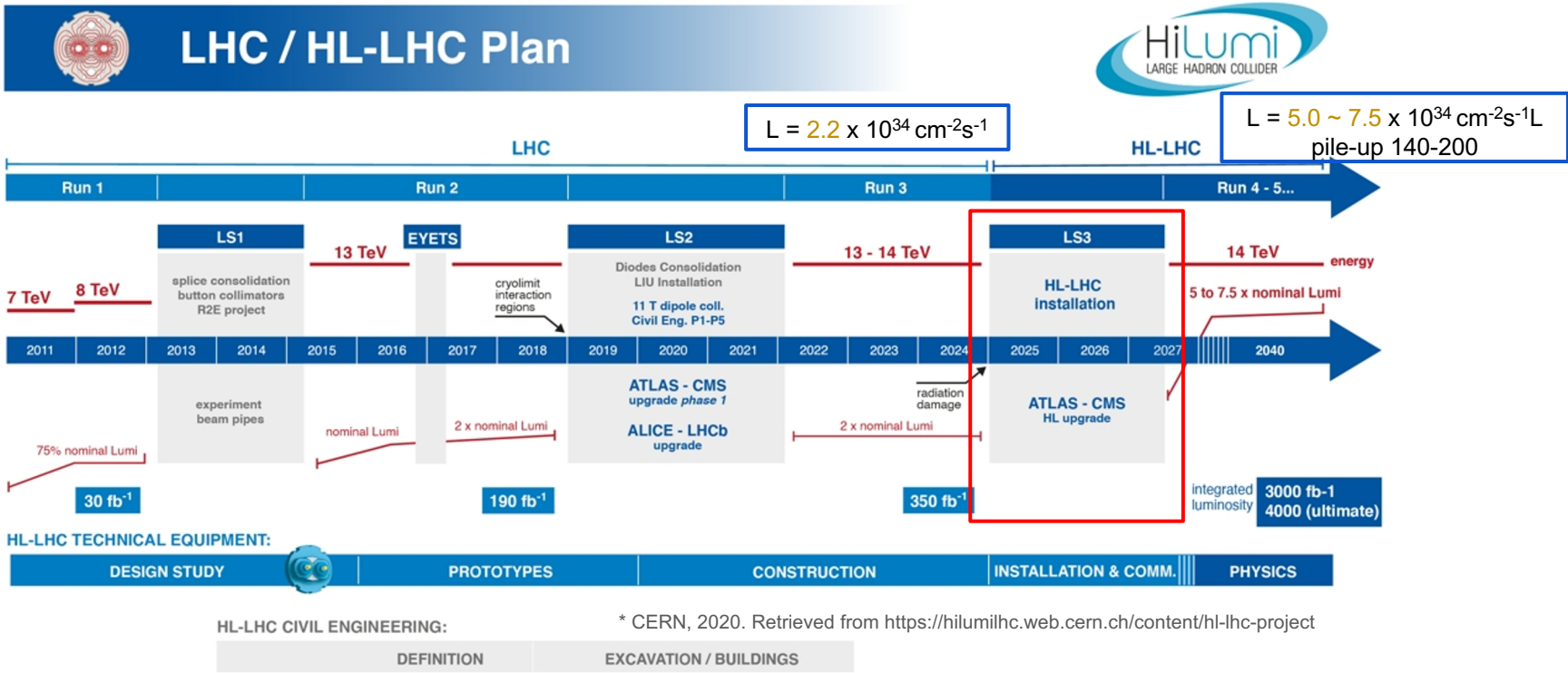
LHC / HL-LHC Plan

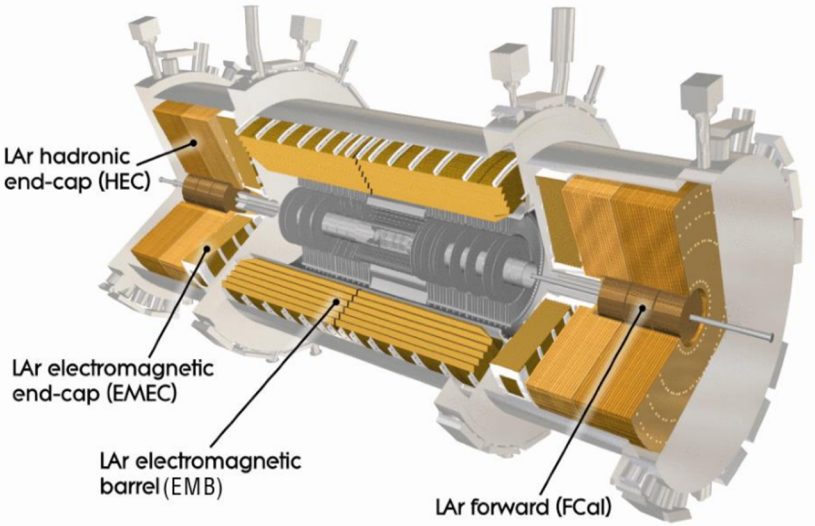


* CERN, 2020. Retrieved from https://hilumilhc.web.cern.ch/content/hl-lhc-project

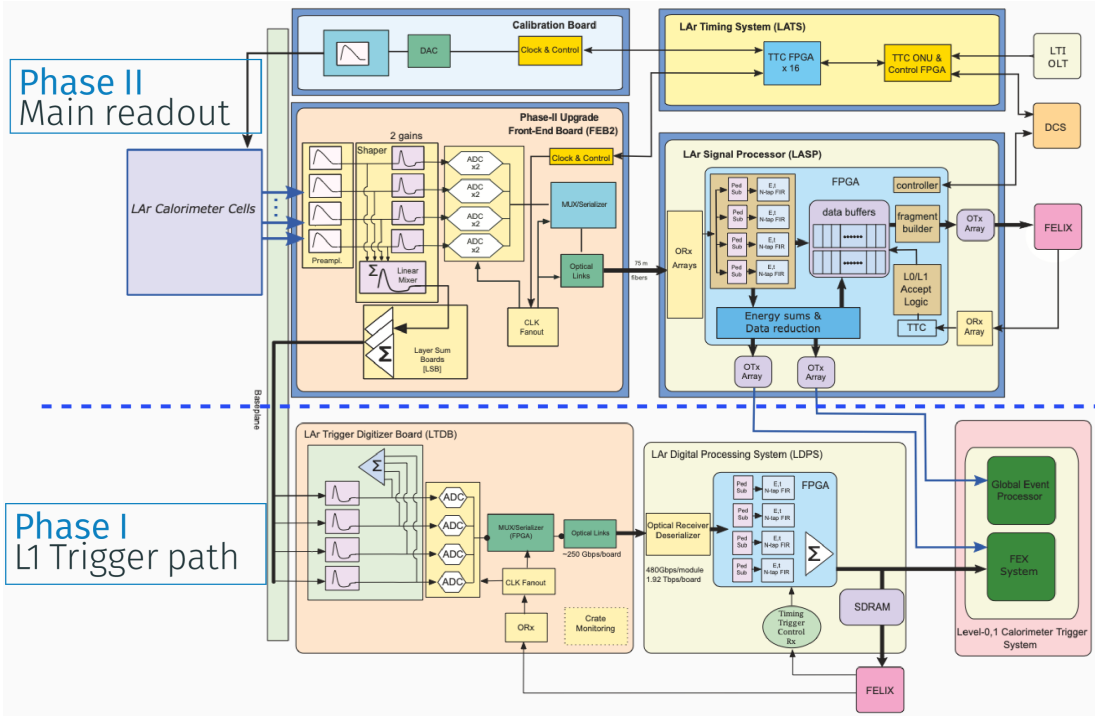
- HL-LHC: very large pileup, radiation tolerance, new ATLAS trigger scheme etc.
- ATLAS Phase 1 upgrade installation is being finalized. The Phase 2 upgrade installation will happen during LS3 (from 2025) of LHC

ATLAS Liquid Argon Calorimeters

- Four parts of the LAr Calorimeter: HEC, EMEC, EMB, FCal
  - Active material: LAr
  - Passive material: lead (EMEC, EMB), copper (HEC), copper & tungsten (FCal)
- A total of 182,468 cells
- Record energies in a range from ~ 50 MeV to ~ 3 TeV per cell. Resolution: $\sigma E/E = 10\%/\sqrt{E} \oplus 0.7\%$ out to $|\eta| < 3.2$
- LAr Calorimeters themselves are expected to operate reliably during the HL-LHC period
- LAr Readout Electronics need to be replaced
  - Meet new ATLAS TDAQ requirements
  - Improved radiation hardness
  - Two-gain system will improve systematics on $H \rightarrow \gamma\gamma$ mass



LAr Phase II Readout Electronics Architecture

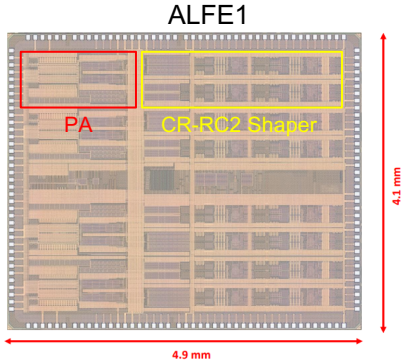


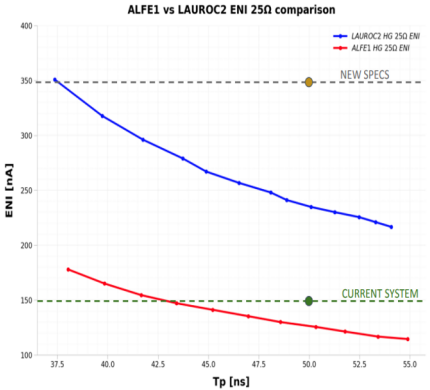
- Phase I upgrade
  - LAr Trigger Digitizer Boards (LTDB)
  - LAr Digital Processing Blade (LDPB)
- 1524 FEB2 in FEC (replace FEB)
  - PA/Shaper ASIC (16b)
  - ADC ASIC (14 bit, 40 MSPS)
  - lpGBT/VTRx+ optical link
- ~ 124 New Calibration Board in FEC (replace the current Calibration Board)
  - ASICs for HF switch and DAC
- LAr Signal Processor to replace the ROD
  - ~ 380 ATCA-based LASP and sRTM (smart Rear Transition Module)
  - Readout the FEB2
- LATs LAr Timing System
  - ~ 20 LATOURNETT (LAr Timing trigger cOntrol distribUtion and fRoNt End moniToring/configuraTion) is being developed
  - Distribute and received control, monitoring and clock to/from FEB2 and calibration board

PA/Shaper ASIC

- ASIC requirements for EM and FCAL
  - 2 designs in CMOS 130nm evaluated: LAUROC2 and ALFE1
  - Analog processing of signals on 4 channels: amplification, CR-RC2 shaping, split on 2 gain scales
  - > 16-bit dynamic range, 4-ch trigger sum output
- ALFE1
  - Zin: 25Ω ± 5% to 50MHz, 50Ω ± 5% up to 30 MHz
  - INL: < ± 0.1%
  - 25/50 Ω - HG ENI (@1.5nF/330pF): 135 nA / 45 nA
  - No degradation under TID test up to 180 kRad

LAr has decided to choose ALFE2 as baseline prototype

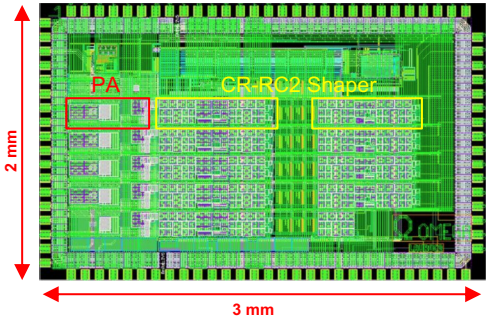


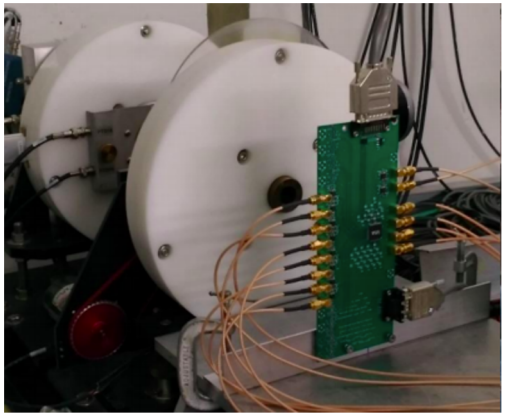


PA/Shaper ASIC (2)

- LAUROC2
  - I2C and trigger sum integrated
  - Zin: 25 Ω ± 15%, 50Ω ± 5% up to 20 MHz
  - INL: < ± 0.2%
  - 25/50 Ω - HG ENI (@1.5nF/330pF): 270 nA / 75 nA
  - TID and SEE tests are good
  - Feature complete design
- HPS1 ASIC for HEC
  - HEC Pre-Shaper and Shaper: based on the LAUROC1 shaper design
  - First pre-prototype
  - Complete performance characterization ongoing
    - *Programmability, waveforms, linearity ok*
    - *Noise and cross-talk will be improved for the next iteration*
  - Irradiation for TID at TRIUMF
    - *No performance degradation observed*

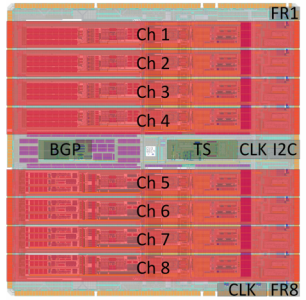
LAUROC2

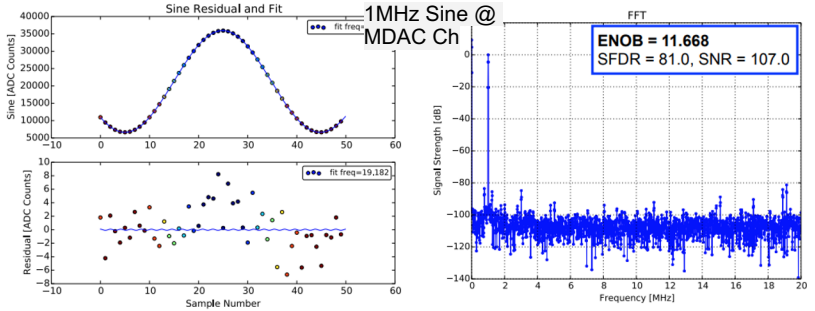


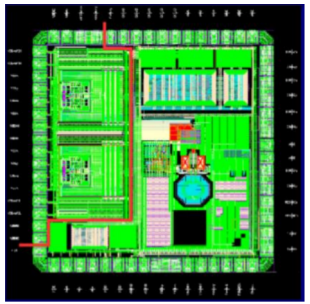


ADC ASICs

- Requirements
  - 14-bit dynamic range, >11 bit ENOB
  - 40 MSPS sampling rate
  - Low power, radiation tolerant up to 180 kRad
  - ePort data interface to lpGBT
- COLUTA ADC (TSMC 65 nm CMOS)
  - COLUTAv3: feature complete design
  - 8 channels : 4 DRE + 4 MDAC
  - Preliminary COLUTAv3 results
    - Dynamic range and ENOB well within specs
    - Coherent noise < 0.2 LSB, cross-talk < 0.1%
    - Long-term stability tests performed
- Commercial IP (of ADESTO/S3) ASIC v1.2
  - Alternate use of ADC IP core developed for CMS ECAL
  - Chips fully functional
  - Performance seems on par with previous iteration
  - Detailed caracterisation to be performed

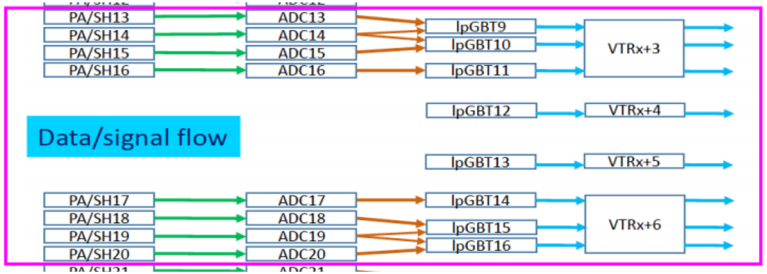


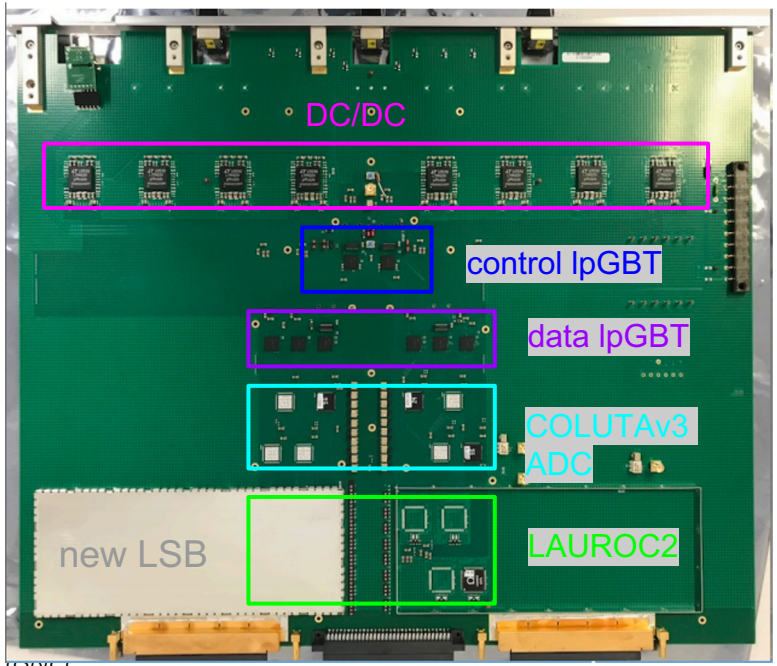




LAr has decided to choose COLUTA4 as baseline prototype

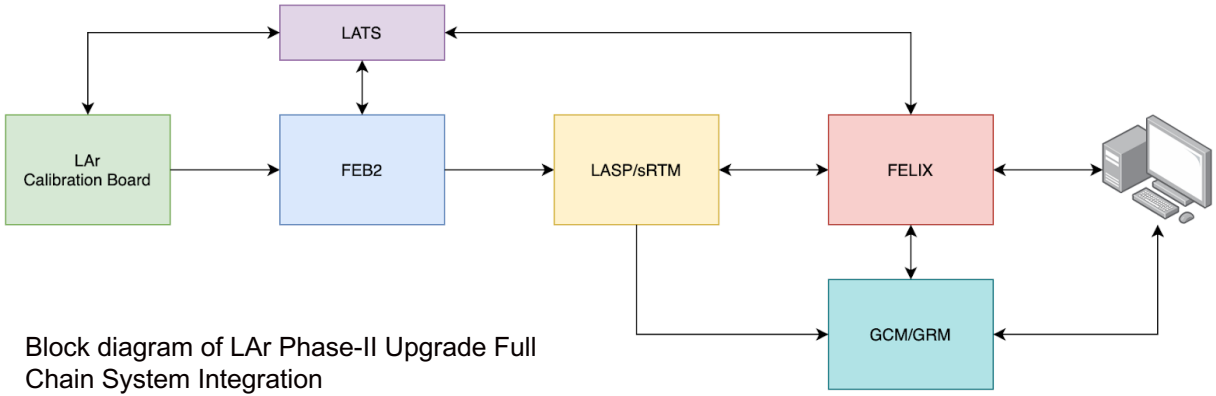
FEB2 Prototype Boards



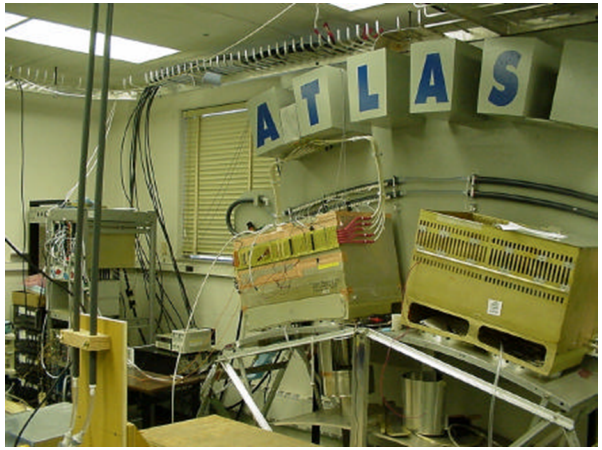


- Three development stages
  - Analog Testboard (2019)
    - 2 (LAUROC1 PA/S + COLUTAv2 ADC) + lpGBT
    - Verified full readout chain PA/S + ADC + optical data links
  - Slice Testboard (2020, now being tested)
    - 8 (LAUROC2 PA/S + COLUTAv3 ADC + lpGBT) chips, 32 LAr channels available
    - Aim to demonstrate multi-channel performance, bi-directional control links
  - Full 128-ch FEB2 Prototype (2021~2022)
    - 22 DAQ links @ 10.24 Gbps
- All ASICs work well on the slice test board, uplink data path verified
- Now integrate with FELIX for high capacity readout, then extensive analog testing

System Integration



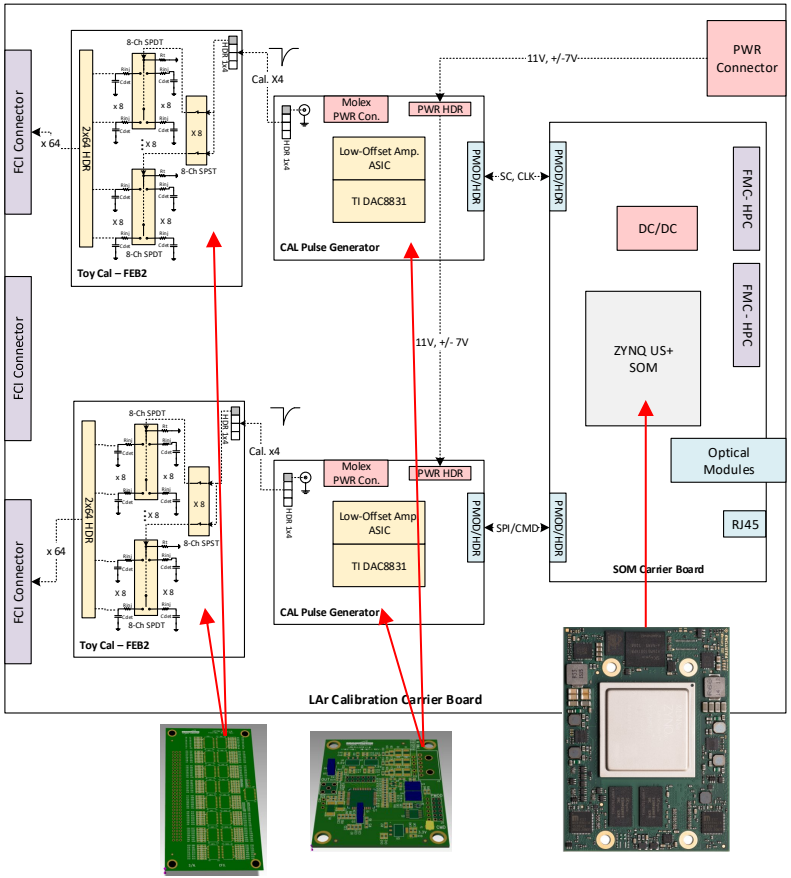
Block diagram of LAr Phase-II Upgrade Full Chain System Integration



Picture of the mockup at BNL

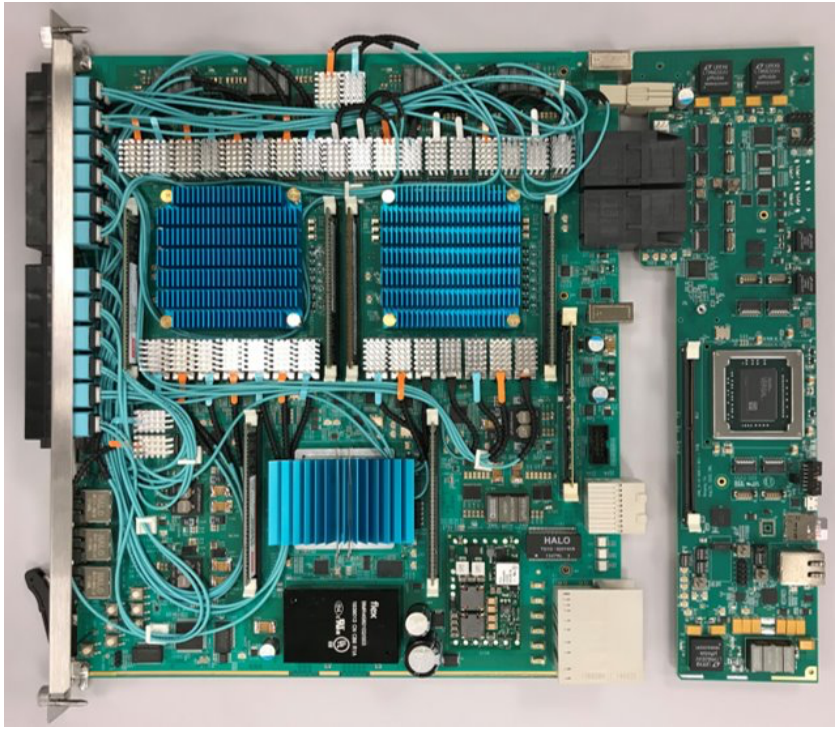
- To validate the system design before the production
- To use the current LAr mockup at BNL with additional developments
  - The mockup at BNL Physics Department reproduces, with high fidelity, the mechanical and electrical properties of the ATLAS LAr calorimeter.
  - It was used to integrate the ATLAS LAr electronics in original construction and the LTDB for Phase I.

Calibration Test board



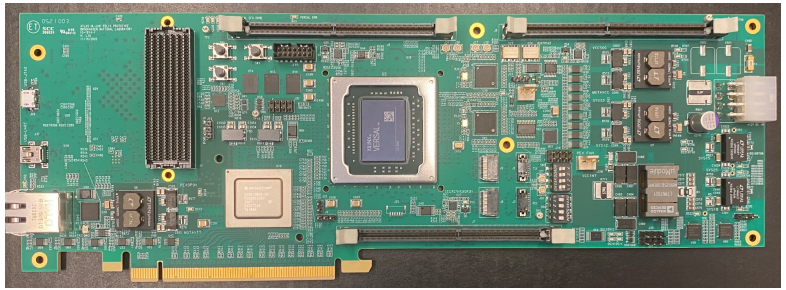
- Calibration test board will be used before the Calibration prototype board becomes available.
- A Carrier Board fitting the FEC has been designed, to integrate:
  - The Toy Calorimeter modules (64ch)
  - The Pulse Generator module
  - FPGA Evaluation board to:
    - Receive the clock and trigger from the FELIX system
    - Control the pulser DAC
- The Slice Test Board/FEB2 software can control the FPGA module via the optical link or a parallel GbE Connection to perform injection test and scan with the Slice Test Board and FEB2
- The Carrier, Toy Calorimeter, and Pulse Generator are currently in production

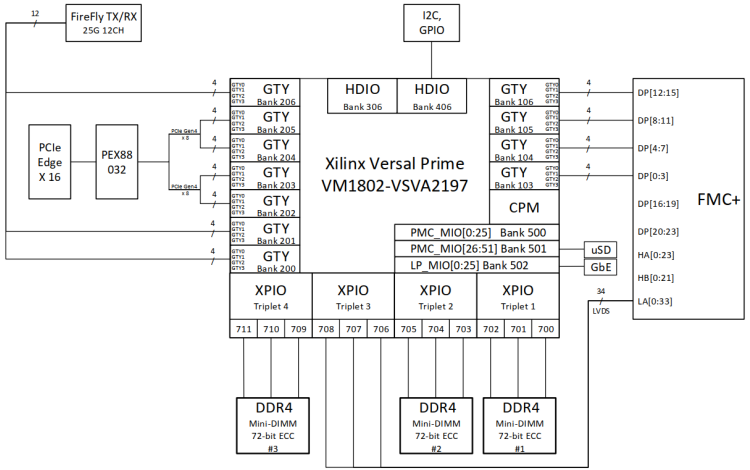
GCM and GRM



- Global Common Module (GCM) is an ATCA-based module and Generic Rear transition Module (GRM) have been developed to receive and process the data from the front-end electronics.
- GCM/GRM will be used for system integration tests with LASP/sRTM.
- GCM
  - Two XCVU13P and One XCZU19EG
    - QSFP/UART/SD/DDR4
    - GbE/I2C/SPI
  - FireFly (18 pairs) running @25Gbps
    - 8 pairs for each VU13P FPGA
    - 1 pair shared with two VU13P for GRM
    - 1 pair for ZYNQMP
- GRM
  - One VM1802 versal FPGA
  - FireFly (4 pairs) running @25Gbps

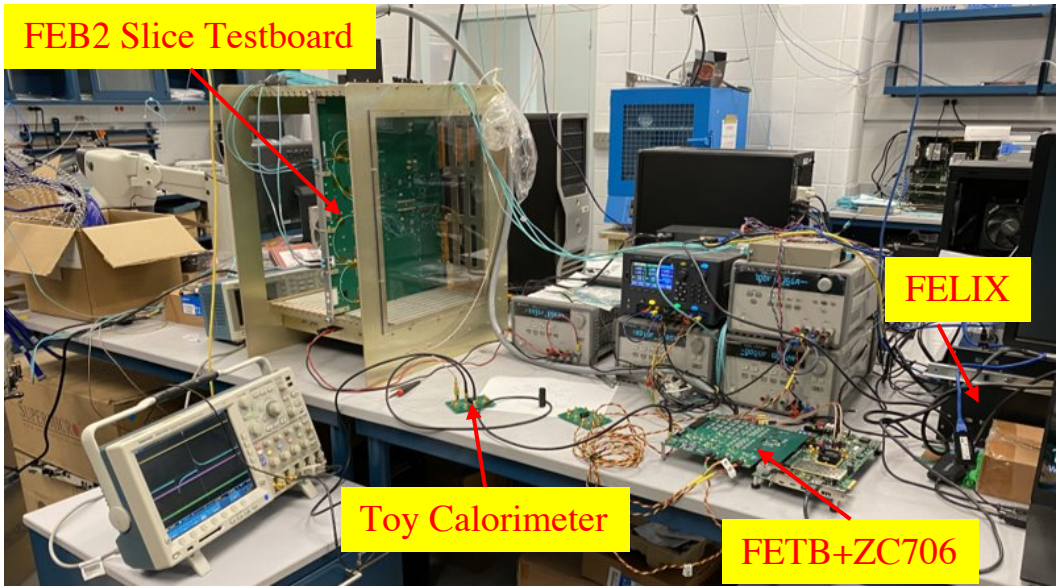
FELIX for HL-LHC

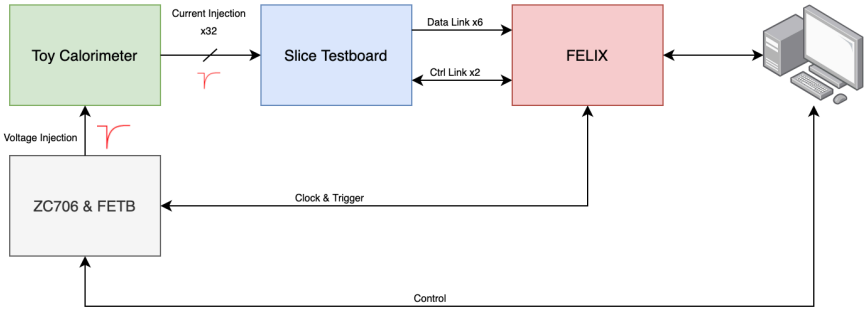


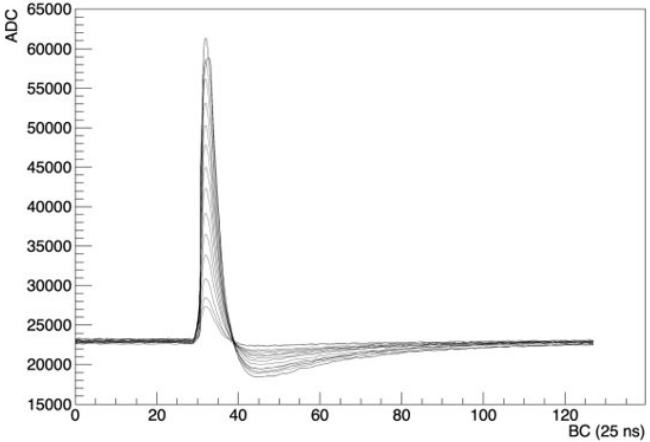


- The FELIX will be used for system integration tests for LAr+TDAQ system
- Xilinx Versal FPGA XCVM1802
- PCIe Gen4 x 16, up to 256 GT/s
  - 16 x GTY links (16 Gbps, CCIX not supported)
  - PCIe Gen4 switch for dual x8 to x16 conversion
- 12 x FE-Links
  - One pair of Samtec Firefly 25G 12-Ch module
- 3 x Mini-UDIMM DDR4 Modules w/ ECC
  - Accessible by both PL and PS through NoC
- FMC + connector for mezzanine card
  - ATLAS/DUNE variant
  - 34 x differential pairs from XPIO banks
  - 16 x GTY links

System Integration for FEB2 Slice Testboard







Preliminary result for LAr pulse injections with different amplitude

Summary

- Baseline designs of ASICs are chosen.
  - ALFE2 has been chosen as PA/Shaper baseline.
  - COLUTA4 has been chosen as ADC baseline.
- Prototype boards design are proceeding.
- The system integration is a critical effort to validate the system design before the production.