22.8 GHz Substrate Integrated Waveguide Analog Frequency Divide-by-3 Circuit

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***Abstract*— A 22.8 GHz analog frequency divide-by-3 circuit is presented based on an injection locked oscillator. Substrate integrated waveguide (SIW) technology is used to implement the input and output sections of the frequency divider circuit. The input SIW section at the gate of the active device permits the introduction of the injection signal at the third harmonic frequency of the oscillator, while the output section is designed to maximize the DC-RF conversion efficiency of the oscillator circuit. A prototype is fabricated presenting a measured DC-RF efficiency of 38.5% at 7.603 GHz output frequency with 3.7 dBm output power. An injection locking bandwidth of 301.4 MHz was obtained for a 1.5 dBm input injection signal at 22.8 GHz.**

***Index Terms*— Substrate integrated waveguide (SIW), oscillator, injection locking, analog frequency divider, harmonic balance**

I. Introduction

SUBSTRATE integrated waveguides (SIW) and circuits (SIC) find good application in microwave and millimeter wave applications due to the fact that they combine attractive properties from both microstrip and waveguide technologies, such as ease of fabrication, high performance including good isolation and low losses, and heat handling capability [1]. As a result there are numerous implementations of passive circuits in SIW technology demonstrating its potential as an alternative to traditionally used microstrip or waveguide technologies. Furthermore, combining active devices with passive SIW structures or embedding them within the SIW itself has led to the development of active SIW circuits such as oscillators, mixers, amplifiers and active antennas [1].

Analog frequency dividers have advantages such as low dissipated power and high frequency of operation, while one of the challenges associated with their design is the limited operating input frequency range [2]-[8]. This paper presents an analog divide-by-3 frequency divider in SIW technology. The design is based on an injection locked oscillator with the input injection signal at 22.8 GHz. The circuit can be used as part of the local oscillator frequency synthesizer circuitry of radar or communication transceivers operating at the 24 GHz Industrial, Scientific and Medical (ISM) frequency band.

The novelty of the design consists of implementing both the input and output sections of the divider in SIW technology and introducing an output section topology similar to the one used in switching amplifiers [9], oscillators [10], and multipliers [11] leading to an increased DC-RF efficiency. The use of a half-mode SIW as a high pass filter placed at the input section of an analog divider has been proposed in [8] taking advantage of the cutoff frequency of the SIW and thus minimizing the loading effect of the input to the divider at the fundamental frequency. In this work, the input section of the divider consists of two cascaded SIW sections, a first one used to set the oscillation frequency and a second one acting as a high pass filter isolating the high frequency input from loading the oscillator at the fundamental frequency. The output SIW section is designed to present a short at the second harmonic frequency at the output node of the active device of the divider. The use of SIW technology may provide a further advantage over microstrip technology in higher operating frequencies due to reduced losses [1]. A prototype was fabricated and measured presenting a 38.5% DC-RF efficiency at 3.7dBm output RF power, and a 301.4 MHz locking bandwidth for a 1.5dBm, 22.8GHz injection signal.

II. SIW Divider Design

The analog divider circuit is based on a harmonically injection locked oscillator. The oscillator is designed using the NE3514S02 HEMT transistor with a shorted waveguide section S_{i1} at its gate terminal and a parallel LC feedback at its source terminal (Fig. 1a). The oscillator output network consists of a SIW section S_{o1} in series with a shunt SIW section S_{o2} optimized to short the second harmonic at the device drain terminal and maximize the DC-RF efficiency. In a second step, the input section of the divider is formed by modifying the transistor gate circuit to include a 22.8 GHz input SIW section S_{i2} (Fig. 1b). The high-pass nature of the SIW S_{i2} allows one to minimize the effect of the input section on the oscillator performance while enabling the introduction of a harmonic injection signal. In a third and final step, the ideal waveguide components are substituted by SIW components optimized to match the ideal waveguide sections, using the commercial electromagnetic simulator Ansys HFSS (Fig. 1c).

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The frequency of oscillation is set by the dimensions of the waveguide sections S_{i1} and S_{o1}, as well as the feedback parallel LC network at the source terminal of the transistor formed by L_s and C_s. The bias networks of the gate and drain terminals consist of 3λ/2 long microstrip lines and radial stubs designed at 7.9 GHz. DC-blocking capacitors C_G and C_D are included in order to isolate the bias current from flowing into the input and output waveguide sections. The circuit is designed to oscillate at 7.722 GHz for a drain bias V_D = 1.0 V and gate bias V_G = -0.68 V, corresponding to a drain current I_D = 8.18 mA. The waveguide section S_{o2} together with S_{o1} lead to the suppression of the second harmonic component at the drain terminal. The oscillating condition is optimized using harmonic balance simulation and its stability verified with transient analysis. In simulation, the oscillator dissipates 9.12 dBm and generates 6.12 dBm with an efficiency of 50.1 % at the above biasing conditions.

The circuit was fabricated on 30 mil thick Arlon A25N substrate using an LPKF Protomat C100/HF circuit board plotter using a 250 um drill bit. The via holes were metalized using LPKF Proconduct paste. The dielectric permittivity and loss tangent of the substrate were 3.38 and 0.0025 respectively. The final design layout parameters and circuit components are listed in Table I.

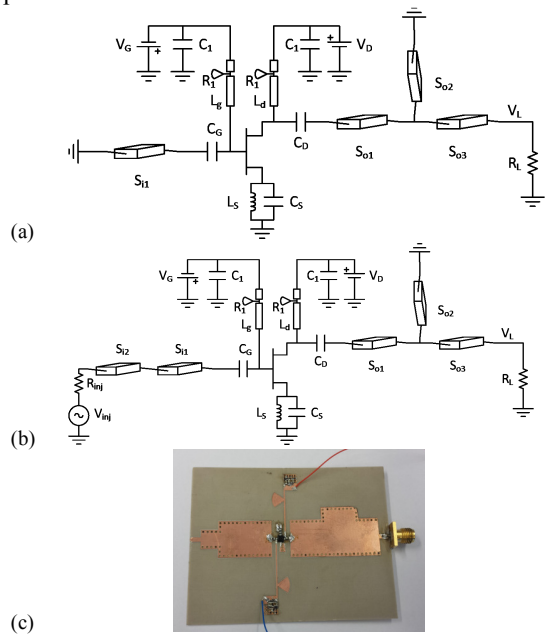

Fig. 1. SIW analog frequency divider circuit: a) oscillator schematic, b) divider schematic, c) photo of fabricated prototype.

TABLE I
CIRCUIT PARAMETERS AND COMPONENTS

Parameter	Value (*)
L_{So1}, L_{So2}, L_{So3}	12.45 mm, 5 mm, 7.75 mm
W_{So1}, W_{So2}, W_{So3}	13.5 mm
L_{Si1}, L_{Si2}	19.2 mm, 6.5 mm
W_{Si1}, W_{Si2}	13 mm, 6.0 mm
C_s	0.25 pF AVX ACCU-P 0603
C_D, C_G	0.7 pF AVX ACCU-P 0603
L_g, L_d, R_1	15.7 mm, 15.7 mm, 5.3 mm
C_1	1nF // 4.7 uF
L_s	0.4 nH (printed)
Via diameter, spacing	0.8 mm, 1.6 mm
HEMT	NE3514S02

(*) SIW section dimensions are listed as via center to center distance.

III. MEASUREMENTS

The fabricated prototype was first characterized as an oscillator, with its input port left open. Due to the high pass nature of the input SIW section the terminating impedance of the input port had a minimal effect at the oscillator performance. The measured circuit frequency, output and dissipated power and DC-RF conversion efficiency for a varying drain bias voltage and V_G = -0.68 V are shown in Fig. 2, 3 and 4 respectively. Simulated results are included in the figures for comparison. The measured performance of the oscillator is 3.7 dBm output power at 7.603 GHz with 38.5 % DC-RF efficiency (V_D = 1.0 V and V_G = -0.68 V). The oscillator dissipated and output power are reduced compared to simulation which leads to a corresponding reduction in the obtained efficiency. The oscillator efficiency remains above 30% for a drain bias voltage tuned from 0.8 V - 2.2 V. The measured oscillator frequency is approximately 1.55% less than the value obtained in simulation. Variations are attributed to component yields and manufacturing tolerances.

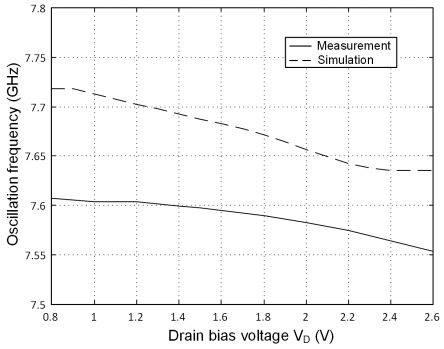

Fig. 2. SIW oscillator frequency versus drain bias voltage (V_G = -0.68 V).

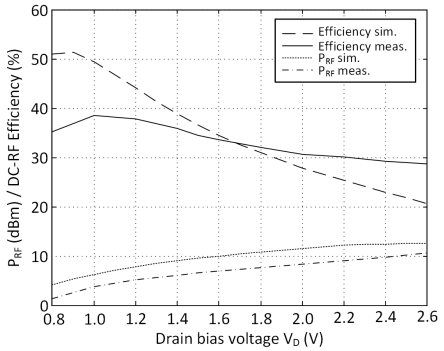

Fig. 3. SIW oscillator output power (P_{RF}) and DC-RF conversion efficiency versus drain bias voltage (V_G = -0.68 V).

The free-running oscillator phase noise was measured at 7.603 GHz and it is shown in Fig. 5. A phase noise value of -107.4 dBc/Hz at 1 MHz offset was obtained which corresponds to an oscillator figure of merit FoM [12] of 176.9 dB. The harmonic content of the oscillator spectrum is shown in Fig. 4. The 2nd and 3rd harmonic suppression is 13.6 dBc and 32.2 dBc respectively.

The analog divide-by-3 circuit performance was evaluated by injecting a 22.8 GHz signal at the input port of the

prototype using a signal generator and an Anritsu Universal Test Fixture (Model 3680V), and varying its frequency and power to determine the locking range. The results are shown in Fig. 6. It is shown that for 1.5 dBm injection signal power a locking bandwidth of 301.4 MHz is obtained, which covers the 250 MHz frequency span of the 24 GHz ISM frequency band.

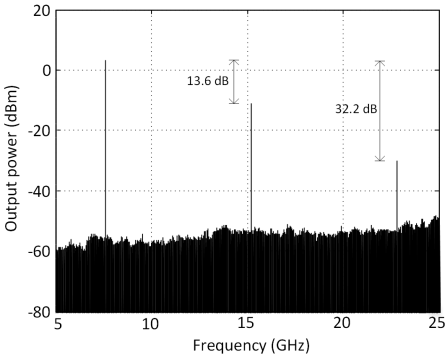

Fig. 4. Measured SIW free-running spectrum (V_D = 1.0 V, V_G = -0.68 V).

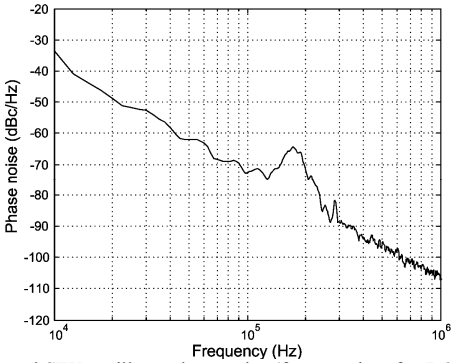

Fig. 5. Measured SIW oscillator phase noise (free-running, f = 7.603 GHz, V_D = 1.0 V, V_G = -0.68 V).

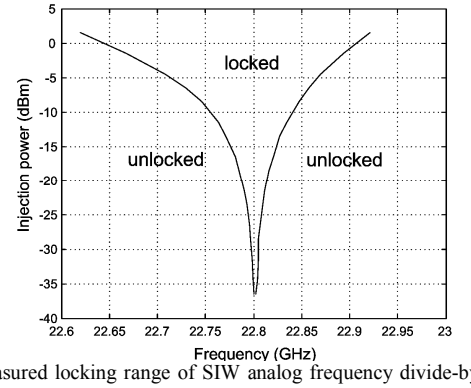

Fig. 6. Measured locking range of SIW analog frequency divide-by-3 circuit (V_D = 1.0 V, V_G = -0.68 V).

The proposed divider is compared with other divide-by-3 circuits in Table II. It presents an increased DC-RF conversion efficiency and it combines frequency conversion and sufficient locking bandwidth for the application under consideration, while it requires an injection power that is lower than its output RF power. An increased locking bandwidth can be achieved by introducing frequency tuning or switching capability to the divider through the use of varactor diodes, PIN diodes or MEMS.

IV. Conclusion

A 22.8 GHz analog divide-by-3 circuit is presented. The circuit is based on an injection locked oscillator topology, implemented in low cost SIW technology and optimized for a high DC-RF conversion efficiency of 38.5% and 3.7 dBm output power at 7.603 GHz. An injection bandwidth of 301.4 MHz at 22.8 GHz for an input power of 1.5 dBm is obtained which is sufficient for the circuit to be used as part of a local oscillator synthesizer circuit for 24 GHz ISM band applications.

TABLE II
Analog Frequency Divider Performance Comparison

Ref.	Div. R	Input Freq. (GHz)	P_{RF} (dBm)	P_{DC} (mW) (Eff. (%))	Lock. Range (MHz)/(%) (P_{inj} (dBm))
[2]	3	11.77 - 16.64 (*)	-7.25	(**) 4.2 (4.5)	425/3.0 (0)
[3]	3	23.17-27.49 (*)	-	(**) 4.28	1000/3.9 (4)
[4]	3	14.04-15.48 (*)	-	9.02	550/3.7 (0)
[5]	3	23.4	-10	17.82 (0.56)	3200/13.7 (0)
[6]	3	21.56-23.63 (*)	-4.96	(**) 1.25 (25.5)	250/1.1 (0)
[7]	3	22.3-26.3 (*)	-	1.7	100/0.42 (-12)
[7]	3	22.3-26.3 (*)	-	7	1300/5.42 (2)
[8]	9	27	-0.9	12 (6.8)	180/0.7 (20)
This work	3	22.8	3.7	6.09 (38.5)	301.4/1.3 (1.5)

(*) Varactor tuning. (**) Not including buffer power consumption.

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