



Dual Low Power Operational Amplifier, Single or Dual Supply

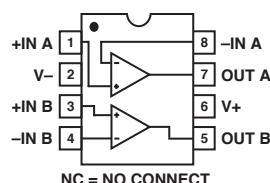
OP221

FEATURES

Excellent TCV_{OS} Match, $2 \mu V/^{\circ}C$ Max
Low Input Offset Voltage, $150 \mu V$ Max
Low Supply Current, $550 \mu A$ Max
Single Supply Operation, $5 V$ to $30 V$
Low Input Offset Voltage Drift, $0.75 \mu V/^{\circ}C$
High Open-Loop Gain, $1500 V/mV$ Min
High PSRR, $3 \mu V/V$
Wide Common-Mode Voltage
Range, V_- to within $1.5 V$ of V_+
Pin Compatible with 1458, LM158, LM2904
Available in Die Form

PIN CONNECTIONS

8-Lead SOIC
(S-Suffix)



GENERAL DESCRIPTION

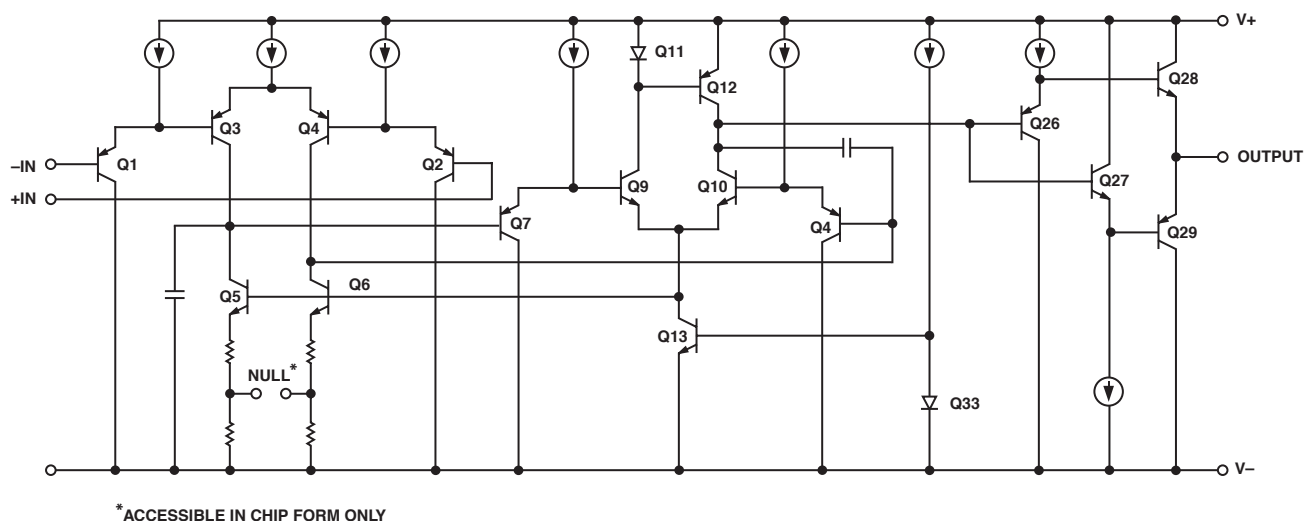
The OP221 is a monolithic dual operational amplifier that can be used either in single or dual supply operation. The wide supply voltage range, wide input voltage range, and low supply current drain of the OP221 make it well-suited for operation from batteries or unregulated power supplies.

The excellent specifications of the individual amplifiers combined with the tight matching and temperature tracking between channels

provide high performance in instrumentation amplifier designs. The individual amplifiers feature very low input offset voltage, low offset voltage drift, low noise voltage, and low bias current. They are fully compensated and protected.

Matching between channels is provided on all critical parameters including input offset voltage, tracking of offset voltage vs. temperature, non-inverting bias currents, and common-mode rejection.

SIMPLIFIED SCHEMATIC



REV. C

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OP221—SPECIFICATIONS (Electrical Characteristics at $V_S = \pm 2.5\text{ V}$ to $\pm 15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

OP221G						
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Offset Voltage	V_{OS}			250	500	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$		1.5	7	nA
Input Bias Current	I_B	$V_{CM} = 0$		70	120	nA
Input Voltage Range	IVR	$V_+ = 5\text{ V}$, $V_- = 0\text{ V}^1$ $V_S = \pm 15\text{ V}$	0/3.5 -15/13.5			V
Common-Mode Rejection Ratio	CMRR	$V_+ = -5\text{ V}$, $V_- = 0\text{ V}$ $0\text{ V} \leq V_{CM} \leq 3.5\text{ V}$ $V_S = \pm 15\text{ V}$ $-15\text{ V} \leq V_{CM} \leq 13.5\text{ V}$	75 80	85 90		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5\text{ V}$ to $\pm 15\text{ V}$ $V_- = 0\text{ V}$, $V_+ = 5\text{ V}$ to 30 V		32 57	100 180	$\mu\text{V/V}$
Large-Signal Voltage Gain	Avo	$V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$ $V_O = \pm 10\text{ V}$	800			V/mV
Output Voltage Swing	V_O	$V_+ = 5\text{ V}$, $V_- = 0\text{ V}$ $R_L = 10\text{ k}\Omega$ $V_S = 15\text{ V}$, $R_L = 10\text{ k}\Omega$	0.8/4 ± 13.5			V
Slew Rate	SR	$R_L = 10\text{ k}\Omega^2$	0.2	0.3		V/ μS
Bandwidth	BW			600		kHz
Supply Current (Both Amplifiers)	I_{SY}	$V_S = \pm 2.5\text{ V}$, No Load $V_S = \pm 15\text{ V}$, No Load		550 850	650 900	μA

SPECIFICATIONS

(Electrical Characteristics at $V_S = \pm 2.5 \text{ V}$ to $\pm 15 \text{ V}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$, unless otherwise noted.)

OP221G						
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Average Input Offset Voltage Drift ¹	TCV_{OS}			2	3	$\mu\text{V}/^\circ\text{C}$
Input Offset Voltage	V_{OS}			400	700	μV
Input Offset Current	I_{OS}	$V_{\text{CM}} = 0$		2	10	nA
Input Bias Current	I_{B}	$V_{\text{CM}} = 0$		80	140	nA
Input Voltage Range	IVR	$V_+ = 5 \text{ V}$, $V_- = 0 \text{ V}^2$ $V_S = \pm 15 \text{ V}$	0/3.2 -15/13.2			V
Common-Mode Rejection Ratio	CMRR	$V_+ = -5 \text{ V}$, $V_- = 0 \text{ V}$ $0 \text{ V} \leq V_{\text{CM}} \leq 3.5 \text{ V}$ $V_S = \pm 15 \text{ V}$ $-15 \text{ V} \leq V_{\text{CM}} \leq 13.5 \text{ V}$	70 75	80 85		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5 \text{ V}$ to $\pm 15 \text{ V}$ $V_- = 0 \text{ V}$, $V_+ = 5 \text{ V}$ to 30 V		57 100	180 320	$\mu\text{V}/\text{V}$
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15 \text{ V}$, $R_{\text{L}} = 10 \text{ k}\Omega$ $V_{\text{O}} = \pm 10 \text{ V}$	600			V/mV
Output Voltage Swing	V_{O}	$V_+ = 5 \text{ V}$, $V_- = 0 \text{ V}$ $R_{\text{L}} = 10 \text{ k}\Omega$ $V_S = 15 \text{ V}$, $R_{\text{L}} = 10 \text{ k}\Omega$	0.9/3.7 13.2			V
Supply Current (Both Amplifiers)	I_{SY}	$V_S = \pm 2.5 \text{ V}$, No Load $V_S = \pm 15 \text{ V}$, No Load		600 950	750 1000	μA

NOTES

¹Sample tested.²Guaranteed by CMRR test limits.

Matching Characteristics at $V_S = \pm 15 \text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

OP221G						
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Offset Voltage Match	ΔV_{OS}			250	600	μV
Average Noninverting Bias Current	$I_{\text{B}+}$				120	nA
Noninverting Input Offset Current	$I_{\text{OS}+}$			4	10	nA
Common-Mode Rejection Ratio Match ¹	ΔCMRR	$V_{\text{CM}} = -15 \text{ V}$ to 13.5 V	72			dB
Power Supply Rejection Ratio Match ²	ΔPSRR	$V_S = \pm 2.5 \text{ V}$ to $\pm 15 \text{ V}$			140	$\mu\text{V}/\text{V}$

NOTES

¹ ΔCMRR is $20 \log_{10} V_{\text{CM}}/\Delta\text{CME}$, where V_{CM} is the voltage applied to both noninverting inputs and ΔCME is the difference in common-mode input-referred error.² ΔPSRR is: $\frac{\text{Input-Referred Differential Error}}{\Delta V_S}$

OP221—SPECIFICATIONS (Matching Characteristics at $V_s = \pm 15\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ for OP221G, unless otherwise noted. G is sample tested.)

OP221G						
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Offset Voltage Match	ΔV_{OS}			400	800	μV
Average Noninverting Bias Current	I_{B+}	$V_{CM} = 0$			140	nA
Input Offset Voltage Tracking	$IC\Delta V_{OS}$			3	5	$\mu\text{V}^{\circ}\text{C}$
Noninverting Input Offset Current	I_{OS+}	$V_{CM} = 0$		6	12	nA
Common-Mode Rejection Ratio Match ¹	ΔCMRR	$V_{CM} = -15\text{ V to } 13.2\text{ V}$	72	80		dB
Power Supply Rejection Ratio Match ²	ΔPSRR			140		$\mu\text{V/V}$

NOTES

¹ ΔCMRR is $20 \log_{10} V_{CM}/\Delta\text{CME}$, where V_{CM} is the voltage applied to both noninverting inputs and ΔCME is the difference in common-mode input-referred error.

² ΔPSRR is: Input-Referred Differential Error
 ΔV_s

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	± 18 V
Differential Input Voltage	30 V or Supply Voltage
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$
Operating Temperature Range	
OP221G	-40°C to $+85^{\circ}\text{C}$
Lead Temperature (Soldering 60 sec)	300°C
Junction Temperature (T_J)	-65°C to $+150^{\circ}\text{C}$

Package Type	θ_{JA} (Note 2)	θ_{JC}	Unit
8-Lead SOIC(S)	158	43	$^{\circ}\text{C/W}$

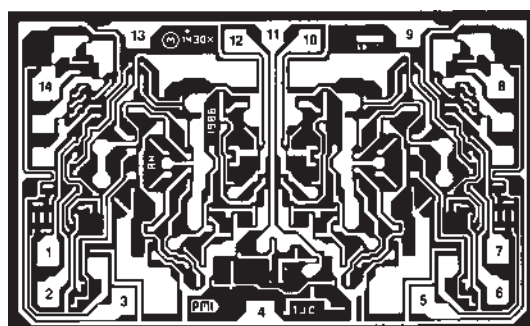
NOTES

¹Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

² θ_{JA} is specified for device soldered to printed circuit board for SOIC package.

ORDERING GUIDE

$T_A = +25^{\circ}\text{C}$ $V_{OS\text{ MAX}}$ (μV)	Plastic 8-Lead	Operating Temperature Range	Package Options
150			
150			
300			
500			
500			
500	OP221GS	XIND	RN-8



1. INVERTING INPUT (A)
2. NONINVERTING INPUT (A)
3. BALANCE (A)
4. V^-
5. BALANCE (B)
6. INVERTING INPUT (B)
7. NONINVERTING INPUT (B)
8. BALANCE (B)
9. V^+
10. OUT (B)
11. V^+
12. OUT (A)
13. V^+
14. BALANCE (A)

DIE SIZE 0.097 X 0.063 INCH, 6111 SQ. MILS
(2.464 X 1.600 MM, 3.94 SQ. MM)

NOTE: ALL V^+ PADS ARE INTERNALLY CONNECTED.

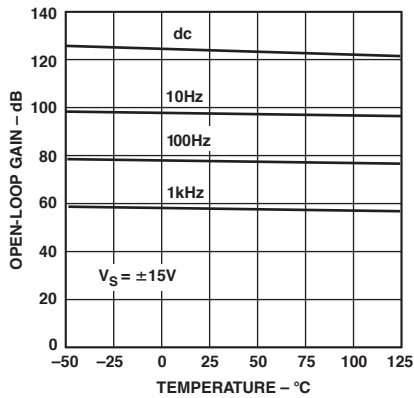
Figure 1. Dice Characteristics

CAUTION

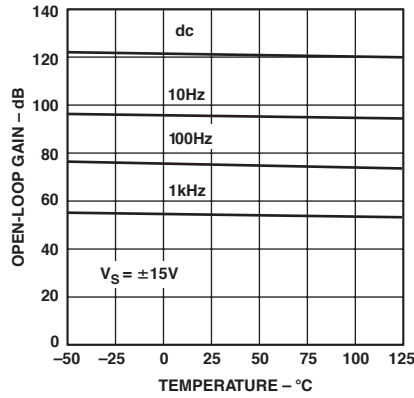
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP221 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



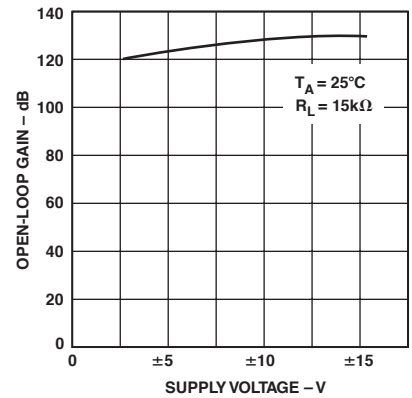
OP221–Typical Performance Characteristics



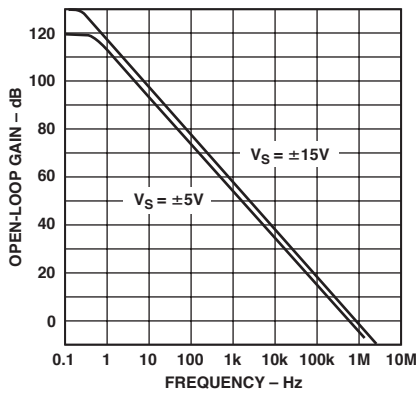
TPC 1. Open-Loop Gain at ± 15 V vs. Temperature



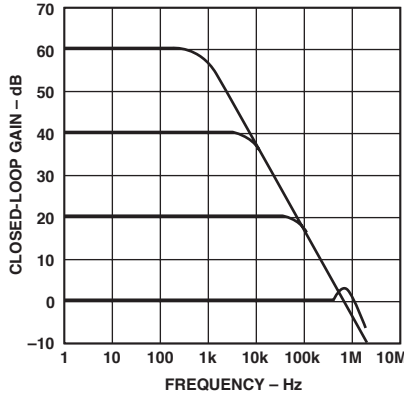
TPC 2. Open-Loop Gain at ± 5 V vs. Temperature



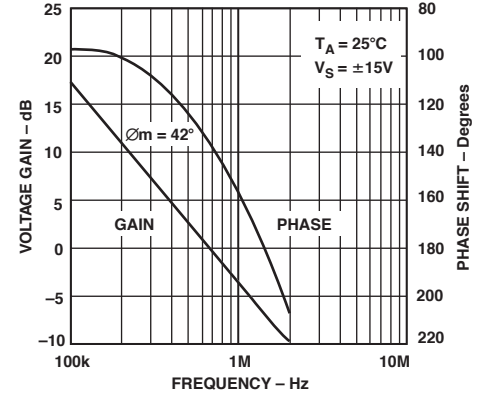
TPC 3. Open-Loop Gain at vs. Supply Voltage



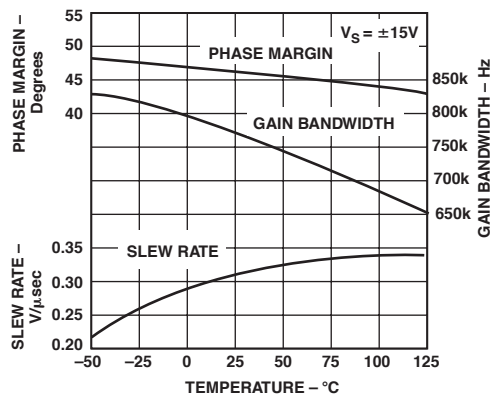
TPC 4. Open-Loop Gain at ± 15 V vs. Frequency



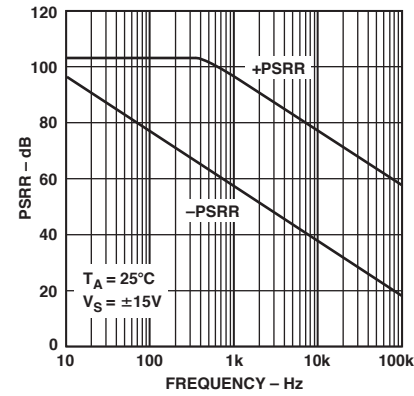
TPC 5. Closed-Loop Gain vs. Frequency



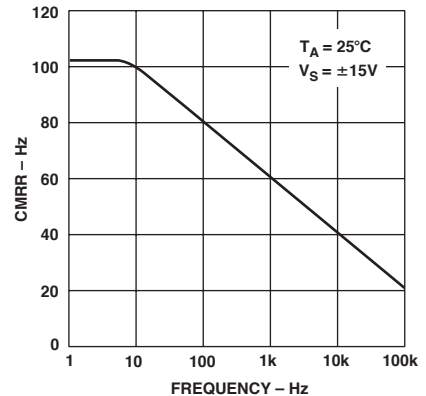
TPC 6. Gain and Phase Shift vs. Frequency



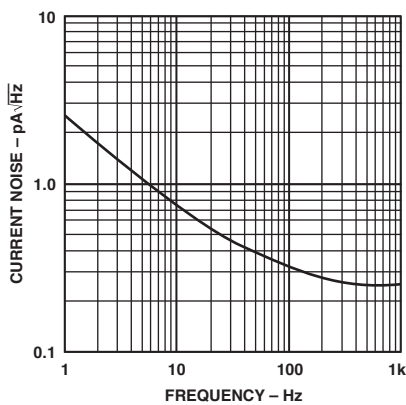
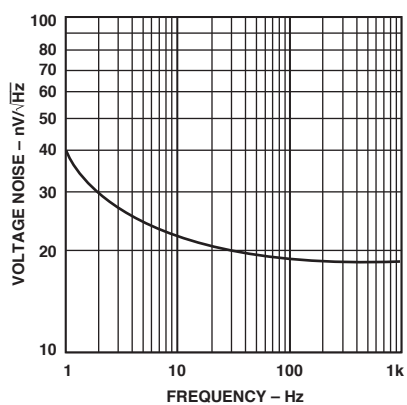
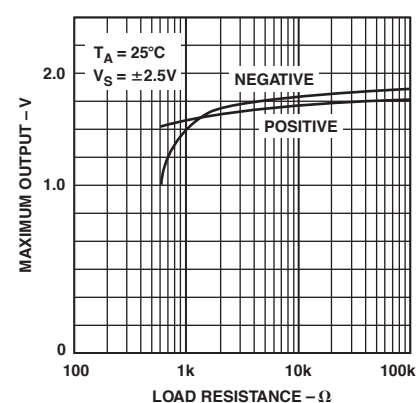
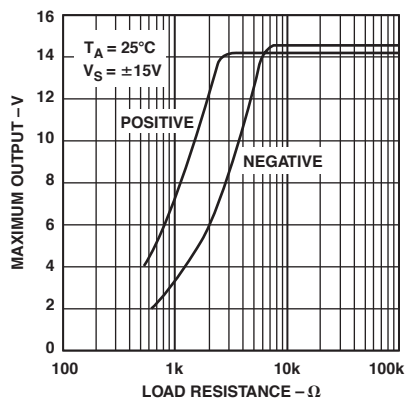
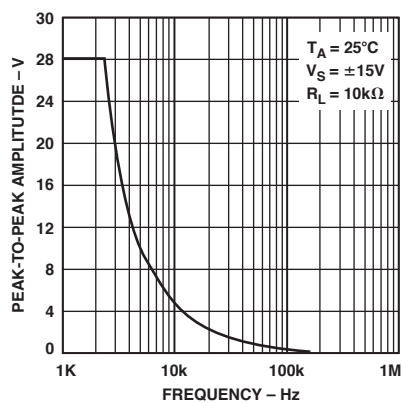
TPC 7. Phase Margin, Gain Bandwidth, and Slew Rate vs. Temperature



TPC 8. PSRR vs. Frequency



TPC 9. CMRR vs. Frequency



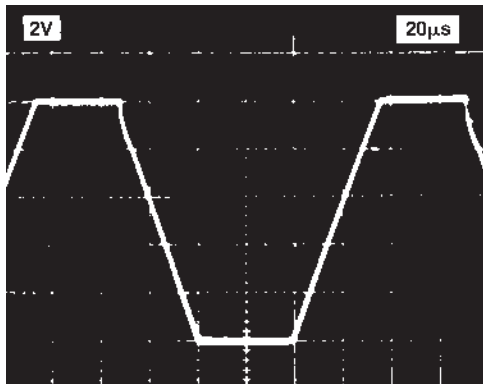


Figure 2a. Noninverting Step Response

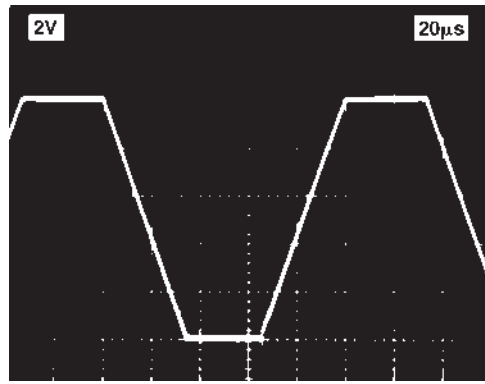


Figure 3a. Inverting Step Response

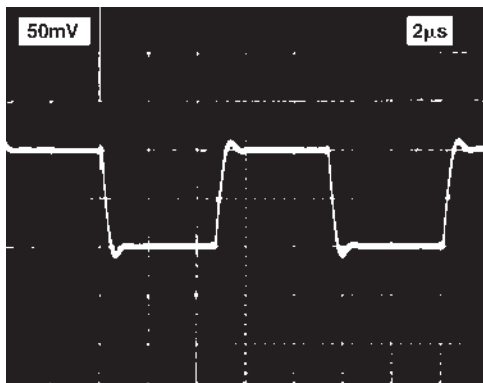


Figure 2b. Noninverting Step Response

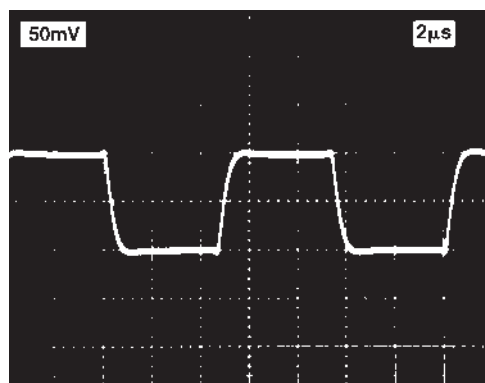


Figure 3b. Inverting Step Response

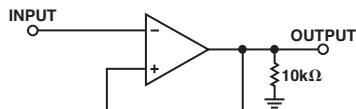


Figure 4. Noninverting Test Circuit

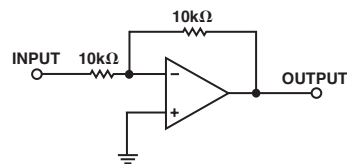


Figure 5. Inverting Test Circuit

SPECIAL NOTES ON THE APPLICATION OF DUAL MATCHED OPERATIONAL AMPLIFIERS

Advantages of Dual Monolithic Operational Amplifiers

Dual matched operational amplifiers provide the engineer with a powerful tool for designing instrumentation amplifiers and many other differential-input circuits. These designs are based on the principle that careful matching between two operational amplifiers can minimize the effect of dc errors in the individual amplifiers.

Reference to the circuit shown in Figure 6, a differential-in, differential-out amplifier, shows how the reductions in error can be accomplished. Assuming the resistors used are ideally matched, the gain of each side will be identical. If the offset voltages of each amplifier are perfectly matched, then the net differential voltage at the amplifier's output will be zero. Note that the output offset error of this amplifier is not a function of the offset voltage of the individual amplifiers, but only a function of the difference (degree of matching) between the amplifiers' offset voltages. This error-cancellation principle holds for a considerable number of input referred error parameters—offset voltage, offset voltage drift, inverting and noninverting bias currents, common mode and power supply rejection ratios. Note also that the impedances of each input, both common-mode and differential-mode, are high and tightly matched, an important feature not practical with single operation amplifier circuits.

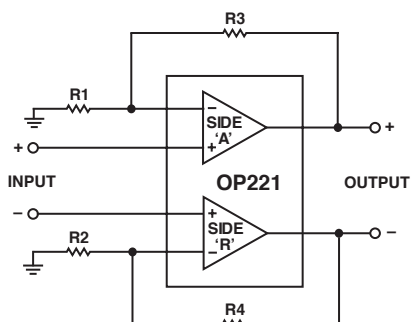


Figure 6. Differential-In, Differential-Out Amplifier

INSTRUMENTATION AMPLIFIER APPLICATIONS

Two-Op Amp Configuration

The two-op amp circuit (Figure 7) is recommended where the common-mode input voltage range is relatively limited; the common-mode and differential voltage both appear at V1. The high open-loop gain of the OP221 is very important in achieving good CMRR in this configuration. Finite open-loop gain of A1 (Ao1) causes undesired feedthrough of the common-mode input. For $A_d/A_o \ll 1$, the common-mode error (CME) at the output due to this effect is approximately $(2 A_d/A_o1) \times V_{CM}$. This circuit features independent adjustment of CMRR and differential gain.

Three-Op Amp Configuration

The three-op amp circuit (Figure 8) has increased common-mode voltage range because the common-mode voltage is not amplified as it is in Figure 7. The CMR of this amplifier is directly proportional to the match of the CMR of the input op amps. CMRR can be raised even further by trimming the output stage resistors.

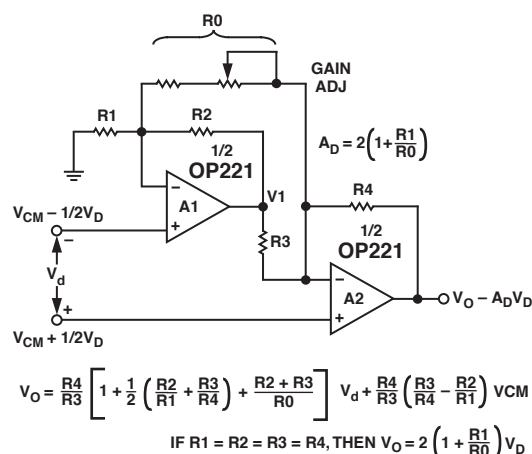


Figure 7. Two-Op Amp Circuit

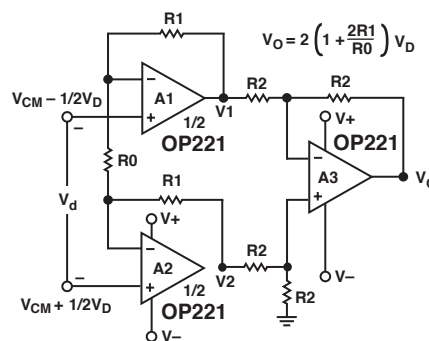
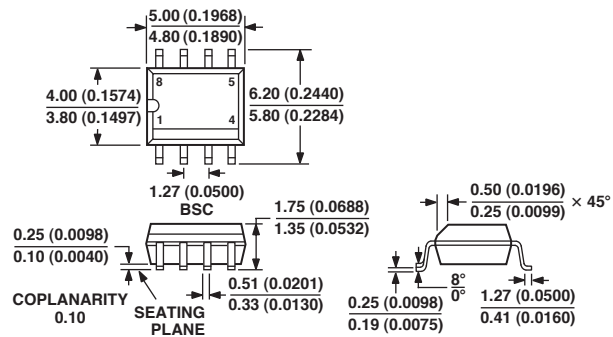


Figure 8. Three-Op Amp Circuit

OUTLINE DIMENSIONS

**8-Lead Standard Small Outline Package [SOIC]
Narrow Body
(RN-8)**

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Revision History

Location	Page
10/02—Data Sheet changed from REV. B to REV. C.	
Deleted 8-Lead Cerdip Package (Q-8)	Universal
Edits to SPECIFICATIONS	2–4
Edits to ABSOLUTE MAXIMUM RATINGS	5
Edits to ORDERING GUIDE	5
Updated OUTLINE DIMENSIONS	10
6/02—Data Sheet changed from REV. A to REV. B.	
Edits to 8-Lead SOIC Package (R-8)	10
09/01—Data Sheet changed from REV. 0 to REV. A.	
Edits to PIN CONNECTIONS	1
Global deletion of references to OP221B and OP221C	2, 3, 4
Edits to WAFER TEST LIMITS	4
Edits to ABSOLUTE MAXIMUM RATINGS	5
Edits to ORDERING GUIDE	5
Edits to PACKAGE TYPE	5

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