A 2.45 GHz Energy-autonomous Wireless Power Relay Node

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***Abstract* — This paper describes the design and experimental characterization of a battery-less bi-directional 2.45-GHz circuit operating in oscillator mode as a wireless power transmitter or in rectifier mode as an energy harvester, with a measured efficiency greater than 50% in both operating states. The DC voltage harvested in rectifier mode provides the drain bias for the oscillator. The FET-gate self-bias mechanism is exploited in both functionalities, to get rid of gate external bias. Bi-directionality is based on the time-reversal properties of a harmonic-suppression oscillator. Energy autonomy is possible at received RF power as low as -4 dBm. This is obtained by means of a bias-assisting feedback loop, consisting of a single matched low-power diode in shunt configuration. A hybrid prototype is demonstrated with the ability to operate as an energy-autonomous power relay node by switching between the transmit and receive power modes.**

***Index Terms* — Microwave oscillator, wireless power transfer, energy harvesting, rectifier, autonomous circuit, battery-less.**

I. Introduction

Miniaturized low-power densely distributed wireless systems are becoming an enabling technology in various applications, from environmental monitoring, e-health, home and industrial automation [1]. Their main advantages are fast and economical deployment, absence of wiring infrastructure, and seamless dynamic repositioning of devices. Several solutions have been pursued to reduce energy consumption [2] as well as to develop high-efficiency harvesting capabilities in order to eliminate the need for battery replacement thus reducing maintenance cost [3], [4]. In such scenarios, strategically located dedicated RF sources can help increase battery lifetime through wireless power delivery to sensors distributed in the source coverage area. One of the issues in RF energy harvesting (EH) solutions is the unknown and often variable RF link (rectenna location and polarization), which can threaten the effective use of energy-autonomous wireless systems. A useful figure of merit for wireless power transfer (WPT) links is the total efficiency from the input of the transmitting antenna to the output of a DC-DC converter [4]:

$$\eta_{TOT} = \eta_{RF-RF} \cdot \eta_{RF-DC} \cdot \eta_{DC-DC} = \frac{P_{RX}}{P_{TX}} \cdot \frac{P_{DC}}{P_{RX}} \cdot \frac{P_{ST}}{P_{DC}} \quad (1)$$

It consists of the product of three contributions: the radio-link, the rectenna and the DC-DC converter efficiencies. Only if intentional RF sources are available $\eta_{RF\text{-}RF}$ can be kept sufficiently high and maximized by design of both transmit and receive parts of the WPT system.

In view of a seamless reconfiguration of architectures based on wireless devices, it is of great interest to rely on devices integrating energy harvesting and wireless power transfer capabilities, thus acting on demand either as a user or as a wireless power provider. If such devices operate bi-directionally to exploit themselves the harvested power or to act as power relay nodes, with the highest possible conversion efficiency, they can be used to provide energy to randomly but closely located wireless devices. In this way such wireless devices can dynamically relocated counting on these power relay nodes.

The added value of this two-step power transmission can be put into evidence by simply referring to Friis equation. The radio-link efficiency $\eta_{RF\text{-}RF}$ between the RF source and the device (tag) can now be split into two terms: the efficiency of the link between the source and the relay node:

$$\eta_{TX-RELAY} = \frac{P_{RX}^{RELAY}}{P_{TX}} = G_{TX} \cdot G_{RX}^{RELAY} \cdot \left(\frac{\lambda}{4\pi \cdot d_{TX-RELAY}} \right)^2 \quad (2)$$

and the efficiency between the relay node and the tag:

$$\eta_{RELAY-TAG} = \frac{P_{RX}^{TAG}}{P_{TX}^{RELAY}} = G_{TX}^{RELAY} \cdot G_{TAG} \cdot \left(\frac{\lambda}{4\pi \cdot d_{RELAY-TAG}} \right)^2 \quad (3)$$

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where G_{TX} is the gain of the RF source antenna, G_{RX}^{RELAY} is the gain of the relay node antenna in rectifier-mode of operation, G_{TX}^{RELAY} is the gain of the relay node antenna in oscillator-mode of operation, G_{TAG} is the gain of the final user antenna.

The key feature of the proposed approach is the possibility to exploit, the high gain of the relay receiving antenna G_{RX}^{RELAY} during the energy harvesting phase, and the relay regenerated power P_{TX}^{RELAY} in the second power-transmission phase. This way the distance $d_{TX\text{-}RELAY}$ can be maximized in the point-to-point transmission described by (2). Whereas, when the relay operates as a RF source, the use of a non-directive relay antenna is compensated by an increased amount of available power P_{TX}^{RELAY}. In this way longer distances $d_{RELAY\text{-}TAGS}$ are expected to be covered. Therefore, the use of the relay node is convenient from a two-fold point of view: for a given distance, the overall link budget is improved; for a given P_{TX}, the powering range is extended.

Bidirectional systems have been proposed in the literature by exploring the time reversal duality [5]. In [6], a 2.4 GHz IMPATT diode based oscillating rectenna is demonstrated with 85% RF-to-DC efficiency as a rectifier and 1% DC-to-RF efficiency as oscillator operating at 3 GHz. This publication highlights the challenges in designing such circuits which consist of maintaining a high efficiency in both operating modes as well as controlling the oscillation frequency and rectifier bandwidth. A promising solution for medium power transfer (on the order of a few watts), is presented in [4], where it is demonstrated that class-F RF power amplifiers exhibit comparable efficiencies when operated as self-synchronous rectifiers. In [7], this concept is extended to a 2.14-GHz 85% efficient 10-W class-F^{-1} rectifier and a Fourier expansion-based theory for various classes of harmonically-terminated rectifiers (C, F, F^{-1}) is developed. In [8] the concept is extended to 10GHz in a GaN MMIC, and in [9] to a two-stage GaN MMIC.

A reconfigurable class-E oscillator/rectifier in the UHF band is presented in [10] to operate with RF power in the mW range. Excellent conversion efficiencies are obtained for both operating modes, but they are strictly dependent on the device bias conditions that need be supplied by external DC batteries.

This paper presents a solution that, for the first time, is able to achieve this functionality without the need for external batteries, by using the energy stored during the rectifier operation mode. A schematic block of the system overview is reported in Fig. 1: to perform the two operations, we use the very same nonlinear circuit, where two switches are simultaneously driven to position 1, for oscillator operation, and to position 2, for rectifier operation. After the first encouraging results obtained in [11], the present paper develops a systematic description of the system design procedure. The principal nonlinear mechanisms enabling its operation modes are deeply discussed and the criticalities associated with their modeling limitations are presented. A second version of the prototype is then presented and the autonomous operation of the oscillator/rectifier is extensively demonstrated by means of both simulated and experimental results. Furthermore the paper presents a physical demonstration of the automatic switching between the two operations.

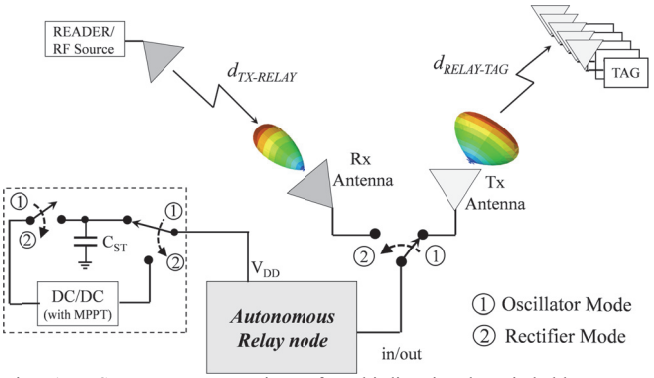

Fig. 1. System representation of a bi-directional switchable energy autonomous power relay node: switch in state 1 corresponds to rectifier operating mode; switch in state 2 corresponds to oscillator operating mode.

The main operating principle is the exploitation of the gate self-bias mechanism of the MESFET [12] for oscillation start-up and rectifier operations with no need for DC biases. For this purpose a medium power HEMT with weakly negative threshold voltage is chosen, thus enabling to start the device operation from floating gate conditions in both transmit and power-receive modes with the same conversion efficiency. In rectification mode, a novel and simple solution based on a single-diode matched network is used as a bias assisting loop, thus allowing rectification at RF power levels as low as -4 dBm. The network is suitably isolated during oscillator operation by means of a coupler optimized together with the entire nonlinear circuit.

Self-sustainability and bi-directionality of the system are then obtained by a sequence of two operations. First the system is set in rectifying mode to harvest the needed DC voltage for biasing the oscillator, and such power can be intentionally provided by the RF sources. For this purpose, some recent researches have provided the design rules for transmitting ad-hoc RF signals able to increase the RF-to-DC conversion efficiency of the receiver [13, 14]. The DC energy can be stored in a super-cap or managed for subsequent use. Second, the system can switch into transmitting mode by using the harvested DC power to start oscillation.

The remainder of the paper is organized as follows. Section II provides an overview of the possible system implementation and addresses the main issues to be solved for the successful autonomous power relay node operation. Sections III and IV discuss the nonlinear design of the node: starting from the oscillator design, the rectifier topology is then derived. For the two subsystems, the nonlinear design results are carefully compared with the experimental validations.

The two main new mechanisms adopted, which are the exploitation of floating gate, for both operations, and the diode-based nonlinear network to enhance gate self-polarization in rectifying mode, are analyzed by means of extensive discussion of the nonlinear simulation results. Section V describes the measurement set-up that is adopted to experimentally prove the switching between the two operations, in order to confirm the ability of the system to behave as an energy-autonomous power relay node.

II. Circuit Level Description of the System

Simultaneous optimization of both operating modes (oscillator and rectifier) is performed by means of nonlinear harmonic balance (HB) simulations with optimization goals on the DC-to-RF oscillator efficiency and on RF-to-DC rectifier conversion efficiency. In this way the oscillator and rectifier operations can coexist in the same linear network, without affecting their optimum performances. The accuracy of the nonlinear simulation is highly dependent on the physical consistency of the adopted FET model, that is its ability to provide, in a synthetic way, a physically consistent global description of the complex phenomena that determine the device performance with a uniform accuracy. For the present case a nonlinear model, with the circuit equivalent topology provided in [15] and shown in Fig. 2, is needed. The same model accuracy for positive, zero and negative drain-source voltages is mandatory to correctly describe the device conduction and displacement nonlinear currents in both oscillator and rectifier operating conditions of the system [16], where the source and drain terminals roles are interchanged. In particular the nonlinear capacitance models for C_{GS}, C_{GD} and C_{DS} are required to satisfy energy constraints all over the drain-source voltage variations; the gate-source and gate-drain diodes are needed to interchange their role as the drain voltage changes its polarity. The R_{CS}, R_{CD} and R_{CG} resistances can be used to model the non-quasi static effect of the charging mechanism [15].

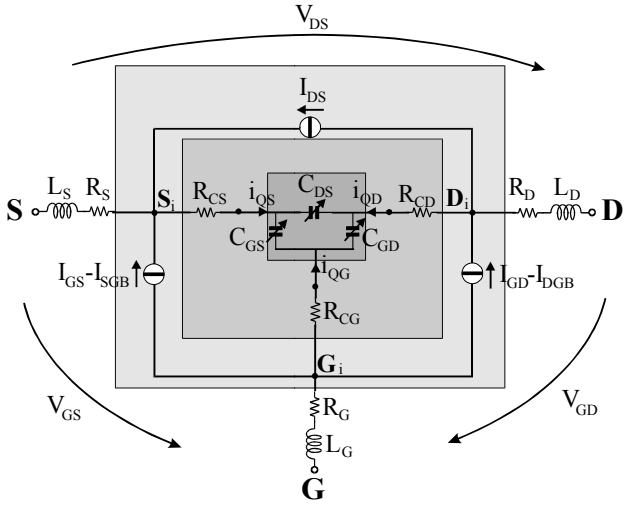

Fig. 2. Schematic topology of a large-signal bilateral FET model with the drain and source terminals topologically interchangeable [15].

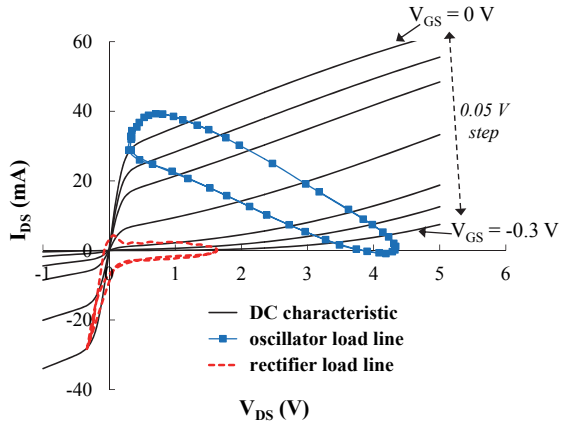

Fig. 3. DC characteristics of the bilateral FET model, parametrized by V_{GS} for $V_{DS}>0$, and by V_{GD} for $V_{DS}<0$, and dynamic load lines in both operating modes.

For the present case we have implemented in ADS a nonlinear model available from the device manufacturer: an acceptable physical consistency with respect to these mechanisms has been preliminary tested for the selected device: in Fig. 3 the DC characteristic are plotted, parametrized by V_{GS} for $V_{DS}>0$, and by V_{GD} for $V_{DS}<0$, showing that the model is able to describe the device symmetry [15]. The dynamic load lines for both the operating modes are given in the same figure: the importance of the third quadrant of the I-V characteristics is evident from the rectifier-mode load line behavior.

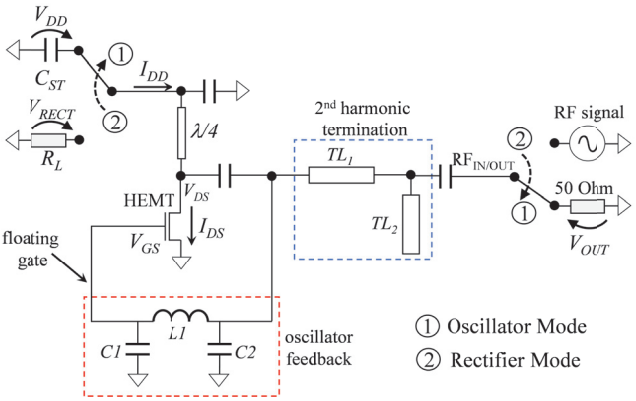

Fig. 4 Circuit schematic of the bidirectional energy autonomous power relay node, with 2nd harmonic termination.

III. Self-Bias Oscillator: Design and Validation

The circuit topology adopted for the oscillator is shown in Fig. 4, with the switches in State 1. It is designed to obtain a 2.45 GHz Class-F oscillator by using a negative threshold voltage device, with a Colpitts-like feedback, embedded in a linear sub-network that is optimized to ensure a class-F second harmonic termination. The higher harmonics were not terminated.

To maximize the DC-to-RF efficiency, the intrinsic drain impedance must satisfy the Class-F harmonic termination condition [17], in addition to the oscillation conditions. For this reason, the harmonic balance optimization used in this paper aims to simultaneously meet the Barkhausen conditions and the maximum DC-to-RF oscillator conversion efficiency, in a suitable range of drain biases. Ideally the latter condition can be searched during the oscillator design by adding the following constraints to the ratio between the drain voltage and current harmonics among the design goals:

$$Z_h(V_{DDi}) = \frac{V_{DS,h}(V_{DDi})}{I_{DS,h}(V_{DDi})} = \begin{cases} < \varepsilon & if\ h\ is\ odd \\ > M & if\ h\ is\ even \end{cases} \tag{4}$$

$$V_{DDi} = V_{DD\,\min}, \ldots, V_{DD\,\max}$$

where V_{DDi} is the drain bias spanning in the interval where oscillation condition is met, ε and M are low and high thresholds, respectively, h is the harmonic frequency index of the adopted spectrum. For the present design 64 harmonics plus DC have been used, but condition (4) has been applied only for $h = 2$.

The active device is a JFET Renesas NE3509M04 with a negative threshold voltage of -0.5 V. The advantage of a negative threshold is two-fold: 1) the oscillation build-up is possible in the absence of a gate bias, that is, in floating-gate condition; 2) the bias point for optimum conversion efficiency can be reached, by exploiting the gate self-biasing mechanism of the transistor [12].

This is explained with reference to the nonlinear FET model of Fig. 2: as oscillation starts, the gate is floating and the RF signal flows into the gate-source junction through the

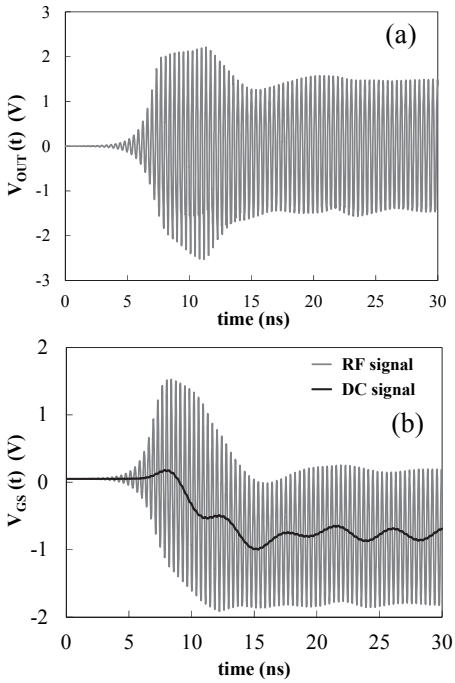

Fig. 5 Simulated transient behavior of the oscillator: (a) oscillator output voltage waveform; (b) gate voltage waveforms (grey curve: RF component; black curve: DC component)

feed-back drain-to-gate capacitance C_{GD}. Due to the Schottky-barrier rectifying property of the gate junction, the RF gate-source voltage generates a DC gate current and the gate capacitance C_{GS} is charged to a negative voltage, thus obtaining a self-biased transistor. In our oscillator topology (Fig. 4) this mechanism is enhanced by the optimized external feed-back network.

The transient analysis results of the oscillator start-up are summarized in Fig. 5 where the simulated waveforms of the gate-to-source voltage and of the oscillator output voltage are plotted. Initially, the drain and gate voltages are zero. During oscillation start-up, the self-bias mechanism drives the gate terminal to a negative voltage, the threshold voltage (or lower), thus allowing the oscillator to operate in a high-efficiency region with a reduced conduction angle. This is highlighted in the same figure where the transient behaviour of

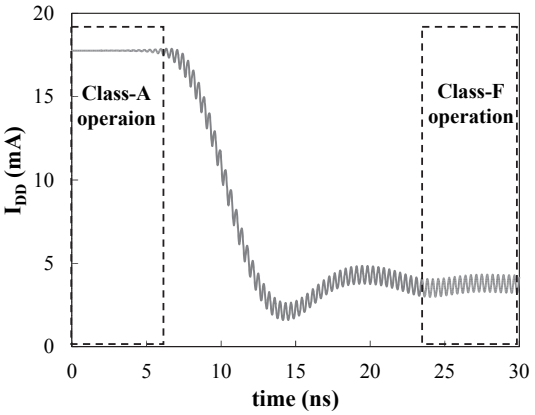

Fig. 6 Simulated transient behavior of the oscillator bias current.

the DC components of the gate-to-source voltage is superimposed to the time-variable waveform.

The shorter the time needed to reach the oscillator class-F steady-state regime, the lower is the power dissipated during the oscillator start-up, the longer is the oscillator steady-state operation. This is a critical aspect for energy autonomy of the system, since the energy stored during rectifier operation should be totally exploited to support the oscillator steady-state regime. Fig. 6 shows the transient behavior of the drain bias current I_{DD}, representing the transistor transition from a high-loss Class-A to a low-loss Class-F operations: in small-signal condition, during start-up, the circuit requires quite a lot of drain current; after oscillation build-up the gate terminal is negatively self-biased and the DC drain current is minimized. The DC power consumed to extinguish the oscillator transient has been minimized in the present design process and could be further reduced by using devices with shorter channel length. In Fig. 7 the simulated and measured oscillator performance in terms of conversion efficiency and generated output power are plotted again versus the drain bias, while Fig. 8 shows the oscillation frequency and gate voltage variations with the drain bias as the tuning variable.

To verify by measurements the circuit in oscillator mode an external bias is used to provide drain polarization (switches of Fig. 4 are in State 1). In Fig. 7 the measured DC-to-RF conversion efficiency and oscillator output power are superimposed to the simulated ones with varying drain supply voltage. The behavior of the measured and simulated quantities are in good agreement, but simulations have been overestimated of about a 15% with respect to measurements. This is probably due to the differences between the HEMT model available for nonlinear simulation and the real device.

The oscillator efficiency is over 50% for the entire drain supply range starting from 2 V. The oscillator mode has a maximum DC-to-RF conversion efficiency of 52.5% at 4.2 V drain bias voltage and an output power of 14 dBm (Fig. 7).

Fig. 9 shows the frequency spectrum of the oscillator, for a drain bias of 4.8 V. The effect of the second harmonic termination is clear from figure inspection. In fact the second harmonic is about 20 dB below the other harmonics.

The frequency spectrum is measured using an Agilent E4440A PSA spectrum analyzer with a resolution bandwidth of 3 MHz.

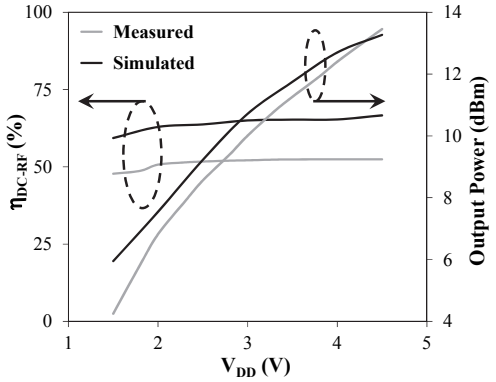

Fig. 7 Measured and simulated oscillator RF-to-DC efficiency and output power with respect to drain bias.

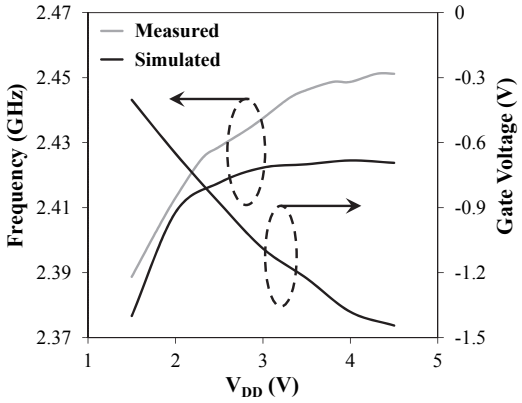

Fig. 8 Simulated gate self-bias voltage, and measured and simulated oscillation frequency, with respect to drain bias.

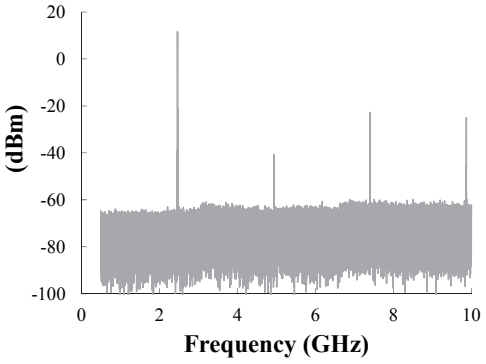

Fig. 9 Measured oscillator output power spectrum.

The oscillator phase noise is shown in Fig. 10. A phase noise of -115 dBc/Hz at 1 MHz from the carrier is measured using the Agilent E4448A PSA vector signal analyzer with span 3 MHz and resolution bandwidth of 1 kHz: the instrument noise floors at frequency offsets of 10 kHz, 100 kHz, and 1 MHz are -116 dBc/Hz, -122 dBc/Hz, and -145 dBc/Hz, respectively. The phase noise measurement has been carried out by biasing the prototype with a 4.5-V battery in order to eliminate supply noise.

IV. Self-Bias Rectifier: Design and Validation

The goal of this section is to present the design and the simulated performances of the oscillator used as rectifier,

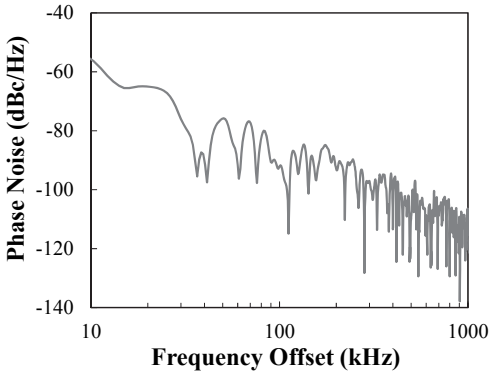

Fig. 10 Measured phase noise of the oscillator/rectifier circuit in oscillator mode.

without any external bias. By means of the Time Reversal Duality (TRD) principle [4], rectifiers with high RF-to-DC conversion efficiency can be derived in a straightforward manner from the design of high conversion efficiency amplifier [18] and oscillator [19]. The available solutions usually are not intended for fully autonomous systems and thus make use of external batteries, to adjust the gate bias in rectifier mode, or adopt a different RF gate termination for the rectifier operation. Here we show a possible procedure to get rid of external battery and of gate termination tuning. Fig. 4 shows the external ports arrangement of the system of Fig. 1 in order to operate as a rectifier (switches in State 2): the drain is disconnected from the DC bias path and is loaded by R_L, which is optimized during the rectifier nonlinear design. The oscillator output port is now fed by the incoming RF signal at 2.45 GHz.

Ideally, by means of the TDR principle, oscillator and rectifier drain voltage and current are related by equations:

$$\begin{cases} V_{DS}^{OSC}(t) = V_{DS}^{RECT}(-t) \\ I_{DS}^{OSC}(t) = -I_{DS}^{RECT}(-t) \end{cases} \quad (5)$$

thus preserving the intrinsic class-F behavior of the transistor. Consequently proper device polarization needs be ensured to provide conversion efficiency in rectifier mode, similar to the one obtained in oscillator mode (Fig. 7). However, to pursue the goal of fully energy-autonomous system, thus getting rid of external batteries, two main issues still need be solved: i) to reach self-synchronized conditions, between the gate and drain voltages, namely waveforms with opposite-phase; ii) to properly select the non-linear device operating points for several possible RF input power levels, by exploiting the FET self-bias mechanism only. Indeed synchronous operation has demonstrated to ensure best rectifier conversion efficiency [18]. In this way a truly seamless switching between the two modes of operation can be performed.

Thus to meet the self-synchronization and maximize the efficiency, a nonlinear optimization of the same circuit topology for the concurrent maximization of the oscillator/rectifier performance has been carried out. As shown in section II a nonlinear device model with accuracy and physical consistencies in the first as well as in the third

quadrant of the I-V characteristics (Fig. 3), is mandatory. The load resistance R_L, that plays a crucial role in achieving the best rectifier conversion efficiency, is determined inside the same design procedure, and an optimum value of about 680 Ω is obtained. It is noteworthy that this design is carried out taking into account a range of possible incoming RF power levels, which correspond to different, and possibly conflicting, nonlinear regimes.

Figs. 11, 12 summarize the results of the non-linear system optimization for the rectifier operation mode. In Fig. 11(a) the simulated RF-to-DC efficiency is plotted. Fig. 11(b) shows the simulated output DC voltage, across the optimum DC load, resulting from the system nonlinear optimization. These plots predict that the circuit is able to operate with efficiency higher than 60 % starting from about +3.8 dBm of input power. This performance is then preserved over a 12-dB RF input power range. From the same plot we get the corresponding DC voltage available at the rectifier output.

The same figure shows the corresponding measured data, too: the circuit is able to operate with efficiency higher than 40% starting from input power as low as 4 dBm. This performance is preserved over a 14 dB range in input power.

Starting from the floating condition ($V_{GS} \cong 0$), Fig. 12 shows the evolution of the DC gate voltage versus input RF power using the self-bias mechanism.

At the lower interval of RF power levels, V_{GS} remains approximately zero; as the power increases, weak rectification is observed up to a selected value at which the DC gate voltage reaches a value lower than the transistor threshold voltage. Increasing further the RF power drives the transistor more deeply in the depletion region, but this does not affect the efficiency performances of the rectifier.

Additionally in Fig. 11 it is shown that the circuit operating in the rectifier mode exhibits hysteretic behavior versus input power. Starting from the minimum RF power levels (solid line), rectification is possible only over 4 dBm. Whereas for decreasing input power (dashed line) the measured rectifier operates down to 1.1 dBm. This further limits the input power ranges for which the circuit could rectify, since operating in the hysteresis zone between 1.1 dBm and 4 dBm is undesirable. In the next subsection we show how we solve this problem by designing a network to act as a bias-assisting loop in rectifier mode without affecting the oscillator mode.

A. Bias-Assisting Loop Rectifier

As previously mentioned, one drawback of combined oscillator/rectifier circuits based on gate self-bias is that, depending on the transistor threshold voltage, a minimum RF input power is needed to start rectifier operation. To overcome this limitation a simple network, based on a matched low-power diode in shunt configuration, is included to bias the gate when the intrinsic transistor mechanism is not active yet. In this way the best RF-to-DC conversion efficiency at lower input power levels can be obtained. The bias assisting loop is optimized to operate at low input power levels when the self-bias mechanism is not yet sufficient.

The loop is designed in such a way that it does not affect

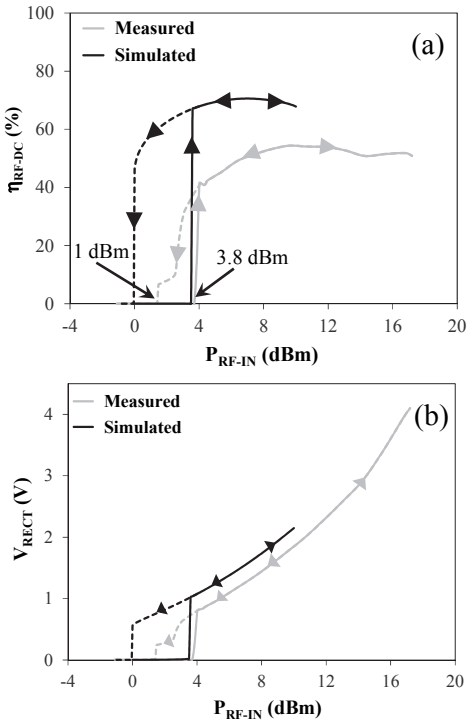

Fig. 11 Measured and simulated RF-to-DC conversion efficiency (a) and output voltage (b) for the oscillator/rectifier circuit operating in rectifier mode, as a function of the input RF power.

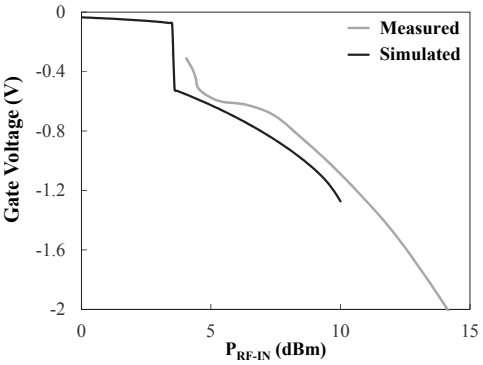

Fig. 12 Measured and simulated self-bias gate voltage as a function of the input RF power.

the oscillator mode operation, while providing the minimum gate bias to start rectification. Fig. 13 shows the modified architecture of the oscillator/rectifier. The bias-assisting loop is connected to the rectifier input (oscillator output) by means of a microstrip coupler, which drives a sample of the incoming RF signal at 2.45 GHz to the diode through a suitably optimized stepped-impedance, with open-stub, matching network. A Schottky diode (Skyworks SMS7630-079) is chosen and is arranged in shunt configuration providing a negative DC voltage at the transistor gate port. The two quarter-wave lines in the assisting loop play the role of RF blocks, thus ensuring isolation between the Class-F oscillator and the bias-assisting loop. In addition they provide the DC path for the Schottky diode and the transistor gate. Coupling and isolation coefficients of the coupler are designed to reach

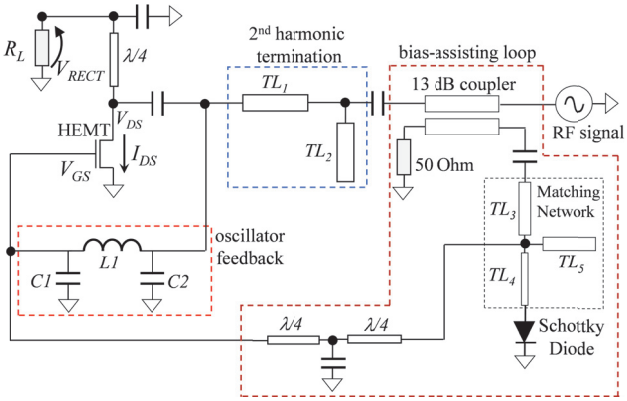

Fig. 13 Oscillator/rectifier system schematic with bias assisting loop.

the best compromise between high isolation between oscillator and bias assisting loop (demanding for high coupler directivity) and minimum power to activate the diode (demanding for low coupler directivity). For the present design a 13-dB coupling has been chosen, resulting in a directivity of 10 dB and an insertion loss of 0.8 dB at 2.45 GHz. A 5% RF-to-DC efficiency degradation has been observed, but the oscillator performance is preserved.

Figs. 14 and 15 show the final optimization results for the system of Fig. 13. In Fig. 14 the DC component of the gate voltage is plotted against input RF power: the minimum activation voltage of -0.3 V is now available at RF input power of -8 dBm. The corresponding simulated RF-to-DC conversion efficiency is shown in Fig. 15: an efficiency better than 60 % is ensured for RF power levels ranging from -4 to 10 dBm.

It is noteworthy that for simplicity the same load is used here for any input power level. We expect possible improvement in efficiency by using a proper DC-to-DC converter to dynamically emulate the optimum load, for any possible RF input [20].

To experimentally characterize the circuit in rectifier mode, the drain bias is disconnected and an input RF signal at 2.45 GHz is fed into the RF port (switches in State 2). The input power levels are varied from -6 dBm up to 18 dBm and the output DC voltage is measured across the output load R_L. Fig. 16 shows the measured output voltage and RF-to-DC conversion efficiency as a function of input power. The same DC load, equal to the one obtained by circuit simulation, was used for these measurements.

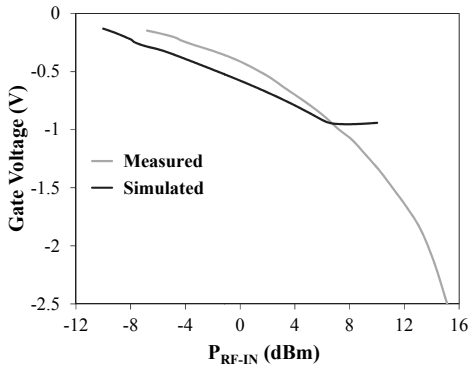

Fig. 14 Measured and simulated self-bias gate voltage with bias-assisting loop as a function of the input power.

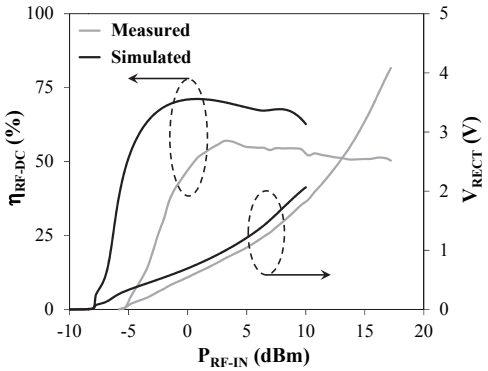

Fig. 15 Measured and simulated RF-to-DC conversion efficiency and output voltage with bias-assisting loop as a function of the input power.

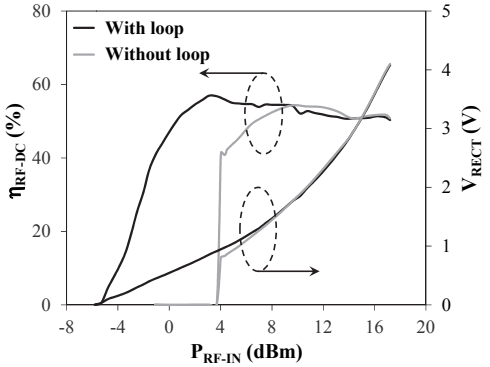

Fig. 16 Measured RF-to-DC conversion efficiency and output voltage, with and without bias-assisting loop as a function of the input power.

The measured plots show that the circuit is able to operate with efficiency higher than 40% starting from input power as low as -2 dBm. This performance is preserved over a 20 dB range in input power. The circuit is able to operate even at lower input power levels but with reduced efficiency (20% efficiency for -3 dBm input power).

Note that numerical convergence was difficult to be obtained during nonlinear circuit simulation to provide the results of Figs. 11, 12, 14, 15. Indeed, the circuit simulator was able to handle problems up to about 10 dBm of RF powers, while measurements could be carried out up to 18 dBm.

Fig. 16 shows the measured rectifier performance with and without the bias-assisting loop: in the absence of the loop the rectifier operates over a reduced input power range, approximately from -4 dBm to 18 dBm. A comparison of the two plots again confirms the key role of the bias-assisting loop in enhancing the system performance: it starts from +4 dBm with 45% of efficiency. Indeed, with the bias-assisting loop, the minimum voltage required to start gate self-biasing is reached with input power levels as low as -3 dBm; whereas without the loop this operation can be safely started only if a 4 dBm input power is available.

V. Experimental Demonstration of the Energy-Autonomous Power Relay Node Operation

The prototype shown in Fig.17(a) is realized on an Arlon AN25N substrate (ε_r=3.38; tan(δ) = 0.0025; thickness = 0.508 mm). Two testing ports are placed for measuring the directional coupler insertion loss and the input matching of the bias-assisting loop. Fig. 17(b) shows the circuit layout with details on microstrip dimension (in mm). The adopted SMD components are capacitors from Murata (GRM1885). At the in/out port an RF switch can be used to connect the node to a directive receiving antenna or to a non-directive transmitting one.

As experimental verification of the energy-autonomous power relay node feasibility, the measurement of the transient waveforms in both the rectifying and power transmitting phases have been carried out. The block diagram of the measurement set up is shown in Fig. 18; the in/out port of the prototype of Fig. 17(a) are alternatively connected to an RF signal generator (HP B3752A) or to an RF oscilloscope (Tektronix DPO72304DX) through a commercial switch (Skyworks SKY13350-385LF).

The measurement procedure is carried out in two steps: i) the switch is connected to port 2, i.e. the signal generator; ii) the switch is commuted by means of an external command and is connected through port 3 to the scope. Hence in the first step the system acts as a rectifier and stores energy into the capacitor C_{ST}. When a stable value of drain voltage is reached, the second step starts and the system oscillation is captured by the scope. As preliminary test, a 50µF is used for the storage capacitance which will be substituted by a DC-to-DC converter able to wake-up the system for low RF input power levels [20, 21]. For the present measurement set-up we simply

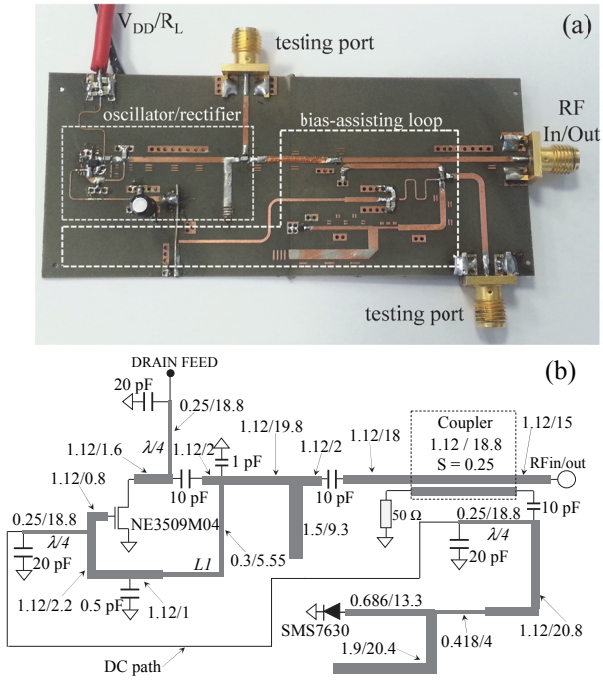

Fig. 17 (a) photo of the fabricated prototype of the bi-directional system with bias-assisting feedback loop; (b) circuit layout with microstrip dimension in mm (width/length).

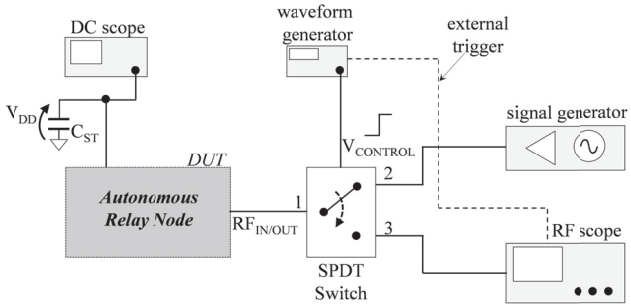

Fig. 18 Block diagram of the measurement set-up.

make use of a higher input power of 8 dBm, resulting in a rectifier output voltage (V_{DD}) of about 2.4 V, in open circuit condition. This value is able to start oscillation as previously shown in the transient behavior of Fig. 7. Fig. 19 shows a photo of the laboratory set-up.

Fig. 20 reports the measurement of the device oscillation transient. Specifically, in Fig. 20(a) discharging of the capacitor C_{ST} is shown as the V_{DD} voltage decreasing with respect to time. Whereas Fig. 20(b) shows the behavior of the circuit: as soon as the RF switch is commuted, the circuit is loaded by a 50 Ω resistor, with a drain bias equal to 2.4 V. These conditions are sufficient for the oscillation build-up. In Fig. 20(b) it can be observed that, after oscillation build-up, the RF output voltage decreases in time in the same way as voltage in the storage capacitor does. The oscillator regime is observed for a 28-ms time interval: this interval is related to

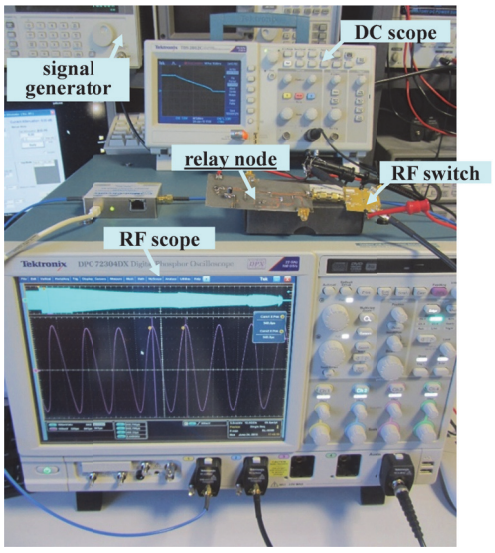

Fig. 19 Photo of the measurement set-up.

the chosen value of the storage capacitor C_{ST} (50 µF). This choice has been driven by the scope constraint in terms of available memory and sampling rate (12.5 GS/s). For example for a C_{ST} of 1 mF and a reduced sampling rate, the measured oscillation lasts more than half a second.

VI. Conclusion

In this paper, the theoretical and experimental aspects of an energy autonomous wireless node are presented. The node can

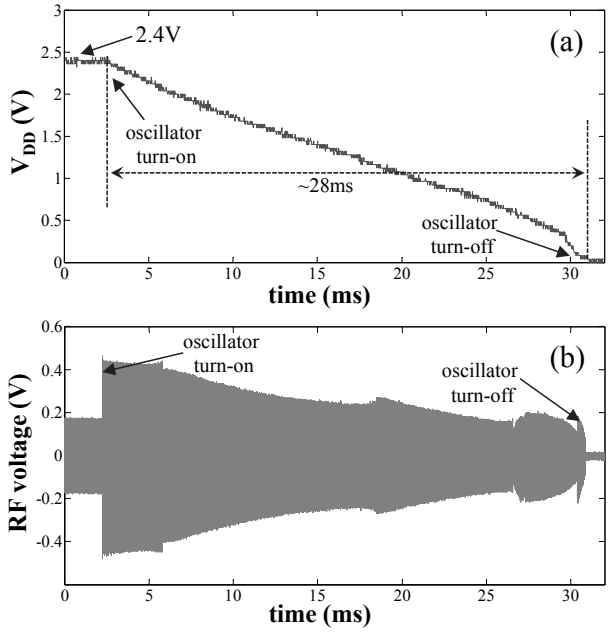

Fig. 20 Measured discharge waveform (a), and transient oscillation waveform (b) of the prototype of Fig. 17(a).

operate continuously without a battery, and demonstrates the same efficiency at 2.45GHz in rectifier power-receive mode and oscillator power-transmit mode. The receiver starts operating at input power levels below 0 dBm and remains in a robust oscillatory regime over a wide range of drain supply voltages.

Based on the previously demonstrated time-reversal property, a new oscillator design is developed using a MESFET floating-gate property for self-biasing. An additional feedback network improves the performance of the system. In the rectifier mode of operation, the gate self-bias is enhanced by a single short-circuited diode. An RF switch is included in the prototype and allows first energy reception and storage, and subsequently power generation for oscillating transmit mode of operation. Measured and simulated results for the 2.45 GHz hybrid prototype are in good agreement, and the circuit is amenable to monolithic integration.

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