Bulletin of Electrical Engineering and Informatics
Vol. 9, No. 1, February 2020, pp. 87~93
ISSN: 2302-9285, DOI: 10.11591/eei.v9i1.1468

Design of a low-power compact CMOS variable gain amplifier for modern RF receivers

M. J. Alam[1], M. A. S. Bhuiyan[2], M. T. I. Badal[3], M. B. I. Reaz[4], N. Kamal[5]
[1,4,5]Electrical, Electronic and Systems Engineering, Universiti Kebangsaan Malaysia, Malaysia
[2]Electrical and Electronics Engineering, Xiamen University Malaysia, Malaysia
[3]Department of Electronic and Telecommunication Engineering, RMIT University, Australia

Article Info

Article history:

Received Jan 3, 2019
Revised Mar 2, 2019
Accepted Sep 26, 2019

Keywords:

CMOS
Receiver
RF
VGA

ABSTRACT

The demand for portability has speeded up the design of low-power electronic communication devices. Variable gain amplifier (VGA) is one of the most vulnerable elements of every modern receiver for the proper baseband processing of the signal. CMOS VGAs are generally suffered from low bandwidth and small gain range. In this research, a two-stage class AB VGA, each stage comprising of a direct transconductance amplifier and a linear transimpedance amplifier, is designed in Silterra 0.13-µm CMOS utilizing Mentor Graphics environment. The post-layout simulation results reveal that the VGA design achieves the widest bandwidth of >200 MHz and high gain range from -33 to 32 dB. The VGA dissipates only 2mW from a single 1.2 V DC supply. The core chip area of the VGA is also only 0.026 mm^2 which is also the lowest compared to recent researches. Such a VGA will be a very useful module for all modern communication devices.

Corresponding Author:

M. T. I. Badal,
Department of Electronic and Telecommunication Engineering,
RMIT University, Melbourne, VIC 3000, Australia.
Email: torikul.uniten@gmail.com

1. INTRODUCTION

The desire for portability and low cost forces the scientists to design very compact and power-efficient communication appliances [1-3]. The continuous advancement in CMOS technology made the realization of fabricating fully integrated receivers easy maintaining the optimum performance. As a consequence, low-power, portable and low-cost RF communication gazettes such as RFID, Bluetooth, Zigbee, Wi-Fi, WLAN devices are available nowadays [4-8].

The variable gain amplifier is one of the most vulnerable constituents in a receiver for the proper baseband processing of the signal [9-10]. In communication RF receivers, the VGA is normally employed to perform the role of stabilizing the signal processed by the baseband circuitry irrespective of the actual signal strength intercepted by the antenna [11-14]. In portable communication devices, VGA is required to operate with low power supply voltage [15-16] and low power dissipation [17-18]. Advancement in the process technology allows devices with low supply voltages. As a result, most low power integrated circuits use power supply voltages below or less than 1.2 V. Designing a low power, wide bandwidth, and highly linear CMOS VGA is very crucial at low supply voltages [19-20]. Figure 1 shows a typical RF receiver front-end including a variable gain amplifier.

There are two types of realizing the VGA circuits. The first one utilizes a switching scheme to adjust among various passive feedback elements, thus generates discrete gain steps. It is often known as digitally

controlled VGA. The second one is an analog linear-in-dB type, where an analog gain control signal controls an adjustable transconductance or resistance. The architectures have their own advantages and disadvantages [21-22]. It is well known that the negative feedback can be utilized to reduce distortion, provided linear feedback elements are available. Typically, only passive elements meet linearity requirements. Therefore, to utilize passive feedback elements in a VGA, they must be selectively switched into the signal path. Since this type circuits can utilize the benefit of negative feedback, they are still able to achieve decent linearity for large output voltages, but the discrete gain levels can be disadvantages for some receivers. For example, wireless communication systems, the signal phase should be continuous, and therefore, the discrete gain step VGA is not preferred [23-24].

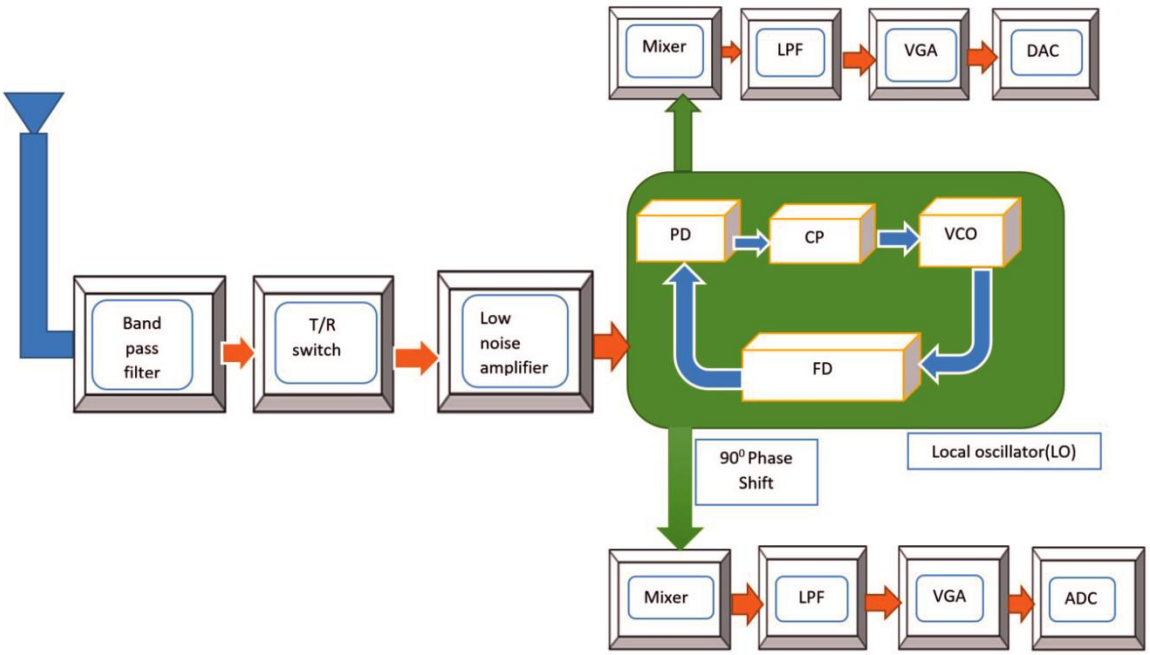

Figure 1. A typical RF receiver front-end

To achieve continuous control of the gain, one or more parameters of the circuit, such as the bias current or the bias voltage, can be continuously varied. The advantage of this type of circuits is that the gain can be varied smoothly between extreme values. The disadvantage is that the linearity of such an amplifier is typically poor. Since altering the bias point of an inherently nonlinear device varies the gain, the only way to achieve acceptable distortion performance is to keep the signal levels low. In analog VGA design, the control mechanism is the prime issue and depending on that several VGA circuit architectures have been proposed by the researchers such as pseudo-exponential function, quasi-exponential function, current steering, feedback tuning, Cherry-Hooper VGA. There are modifications as well as the addition of extra circuits have been reported to these designs to obtain specific performance specifications [25-26]. Most of them have suffered from nonlinearity, low gain, narrow bandwidth and high power dissipation. Therefore, a very compact VGA design with better performance is very important for low-power communication devices. This research illustrates the design of a two-stage low power, wide bandwidth, and compact class AB variable gain amplifier in Silterra 0.13 µm CMOS process. The proposed VGA overcomes the constraints of the small bandwidth and small gain range at small supply voltages at a very compact die.

2. RESEARCH METHOD

The building blocks of the proposed two-stage VGA circuit are illustrated in Figure 2. Each block comprises of a cascaded linear transconductance amplifier (Gm cell) and a linear transimpedance amplifier (TIA) along with feedback through shunt resistors to keep the bandwidth stable during voltage gain variation. In this design, a source degeneration differential input Gm cell (N1–N2, Rs) and a current mode TIA

(P1–P6, N3–N6) has been cascaded in order to maximize the bias current efficiency, transconductance at a supply voltage as shown in Figure 3. From the small signal analysis of each stage of the amplifier, the voltage gain of each stage of the two-stage VGA is determined from the values of the Gm and the Rm. The values of the Gm and Rm of the transconductor part can be evaluated as:

$$G_m = \frac{(g_{in})}{(1+g_m R_s + sR_s C_{gs})} \quad (1)$$

$$R_m = -\frac{(R_f A_i - R_{in})}{(1+A_i)} \quad (2)$$

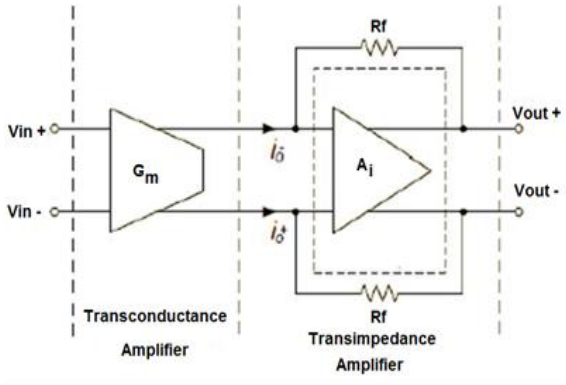

Figure 2. Design of the single stage variable gain amplifier circuit

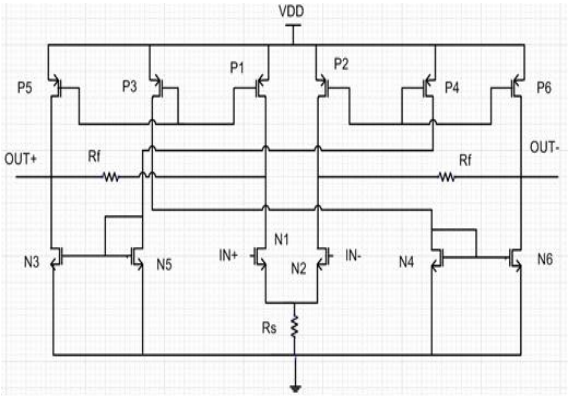

Figure 3. Schematic of the single stage of the VGA circuit

Where A_i and R_{in} correspond to the current gain and the input resistance of the amplifier and C_{gs} correspond to the gate-source capacitance of the Gm cell. If the value of Ai is much greater than unity, the value of R_m can be considered to be equal to $-R_f$. This implies that in order to achieve a linear variable gain amplifier, a linear R_m with high-gain is needed.

$$A_i = \frac{g_{mx}}{g_{mi}+sC_x}\left(1+\frac{g_{my}}{g_{my}+sC_y}\right) \quad (3)$$

$$R_{in} = \frac{1}{(g_{mi}+sC_x)} \quad (4)$$

Where g_{mi}, g_{mx} and g_{my} are transconductance of P1–P2, P3–P6 and N3–N6 respectively. At low frequencies, the value of R_m can be estimated as:

$$R_m = -\frac{\alpha\left[2R_f - \frac{1}{g_{mx}} + s\frac{C_y}{g_{my}}\left(R_f - \frac{1}{g_{mx}}\right)\right]}{2\left[1+\alpha+s\left(\frac{C_y}{g_{my}}\left(1+\frac{\alpha}{2}\right)+\frac{C_x}{g_{mi}}\right)+s^2\frac{CxCy}{g_{mi}g_{my}}\right]} \quad (5)$$

It is worth mentioning that, the transistor sizes are kept as small as possible to achieve smaller size without degrading the performance of the amplifier. Two stages of the proposed VGA are tied together with proper impedance matching. Table 1 shows the component sizes used in each stage of the VGA.

Table 1. Components used in the single stage VGA circuit

Components	Size
P1- P2	1/0.13 (µm/µm)
P3-P6	100/0.13 (µm/µm)
N1-N2	100/0.13 (µm/µm)
N3-N4	30/0.13 (µm/µm)
N5-N6	10/0.13 (µm/µm)
Rs	2K
Rf	600K

3. RESULTS AND ANALYSIS

The VGA, in this research, has been designed and simulated in Eldo RF simulator of the Mentor Graphics utilizing Silterra 0.13-µm standard CMOS process technology. The circuit is powered by a single 1.2 V DC supply. The results presented in this article are post-layout simulation results. Figure 4 and Figure 5 show two types of gain response curves by changing the value of feedback resistor (Rf) from 15k to 500k and source degeneration resistance (Rs) from 10k to 1M, respectively. The VGA shows the highest and the lowest gain of 32dB and -33 dB with Rs=500k, and Rs=15k, respectively. The varying values of Rf from 10k to 1M varies the bandwidth from 30 MHz to 200 MHz. The VGA dissipated approximately 2 mW at the 1.2 V supply voltage.

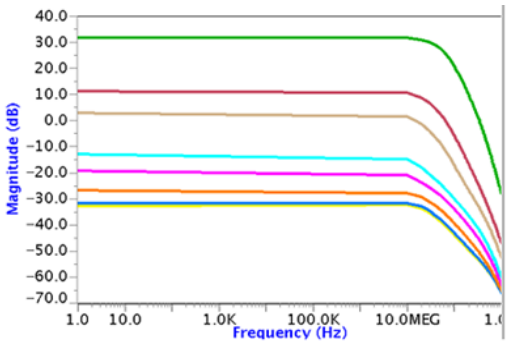

Figure 4. Gain responses by varying feedback resistor (Rf)

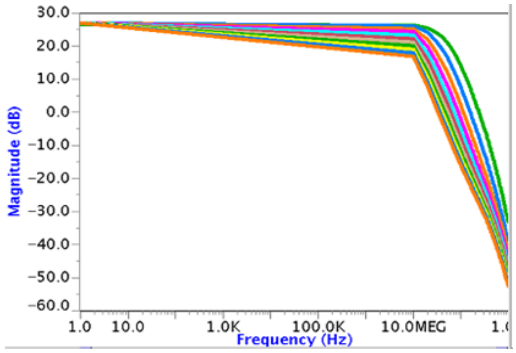

Figure 5. Gain responses by varying source degeneration resistor (Rs)

The Monte Carlo analysis of the proposed VGA for maximum gain is shown in Figure 6. In Monte Carlo analysis, for 50 runs or counts, the values of the maximum gain were between 31.7 dB and 32.7 dB. The results implies that the performance parameters of the VGA were stable within the acceptable range. Figure 7 shows the core layout of the proposed two-stage VGA circuit. In this design, multi-finger structure has been implemented for transistors with large aspect ratios to ensure better conductivity. The dimension of the core VGA is only (160×162) μm^2.

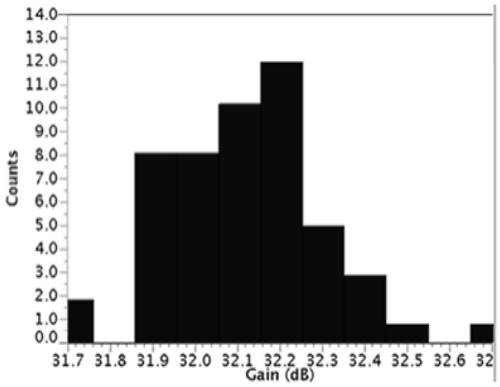

Figure 6. Monte Carlo analysis of the VGA for maximum gain

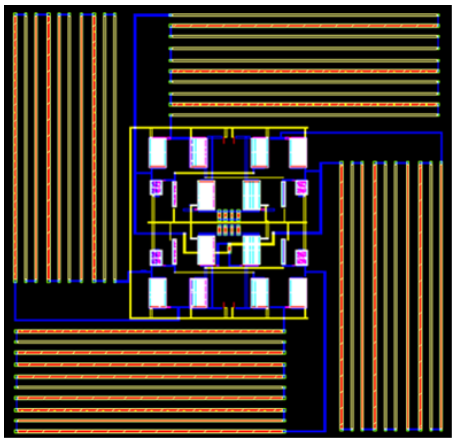

Figure 7. Core layout of the proposed VGA circuit

The performance of the proposed variable gain amplifier is presented in Table 2. The results are also compared with other previously published VGA designs. The comparative study confirms that the proposed VGA has the widest bandwidth of >200 MHz and smallest die area of 0.026 mm^2. It also shows very competitive power dissipation, and gain range.

Table 2. Performance comparison of variable gain amplifiers

Ref.	CMOS process (µm)	Gain range (dB)	Bandwidth (MHz)	Supply voltage (V)	Power dissipation (mW)	Die area (mm^2)
[17]	0.18	-30 to 65	>32	1.8	22	-
[18]	0.18	-39 to 55	>4	1.8	20.5	0.42
[26]	0.18	16.4	-	1.8	14.4	0.036
[24]	0.13	0 to57	>10	1.2	4.44	0.58
[23]	0.18	60	-	1	0.14	-
[25]	0.18	-7.5 to19.5	~15	1.8	~9.2	-
This work	0.13	-33 to 32	>200	1.2	2	0.026

4. CONCLUSION

In communication receivers, the VGA is essential to stabilize the uncertain signal strength received at the antenna for proper baseband processing. Wide bandwidth VGA design in downscaled CMOS process is very challenging for the researchers. In this research, a compact design of two-stage class-AB variable gain amplifier in Silterra 0.13-µm CMOS process is proposed to meet the goal. The post-layout simulation results reveal that VGA has the widest bandwidth of >200 MHz and smallest die area of 0.026 mm^2. It also shows competitive power dissipation, and gain range.

REFERENCES

[1] T. I. Badal, M. B. I. Reaz, M. A. S. Bhuiyan, and N. Kamal, "CMOS transmitters for 2.4-GHz RF devices: design architectures of the 2.4-GHz CMOS transmitter for RF devices," *in IEEE Microwave Magazine*, vol. 20, no. 1, pp. 38-61, Jan 2019.

[2] S. Fazel and J. Javidan, "A highly efficient and linear class AB power amplifier for RFID application," *Bulletin of Electrical Engineering and Informatics*, vol. 4, pp. 147–154, 2015.

[3] M. A. S. Bhuiyan *et al.*, "Active inductor based fully integrated CMOS transmit/receive switch for 2.4 GHz RF transceiver," *Anais da Academia Brasileira de Ciências*, vol. 88, pp. 1089-1098, 2016.

[4] R. Radzuan *et al.*, "0.18µm-CMOS rectifier with boost-converter and duty-cyclecontrol for energy harvesting," *Bulletin of Electrical Engineering and Informatics*, vol. 7, pp. 161-168, 2018.

[5] K. A. Rosli *et al.*, "A comparative study on SOI MOSFETs for low power applications," *Research Journal of Applied Sciences, Engineering and Technology*, vol. 5, pp. 2586-2591, 2013.

[6] Z. Liu, Y. Wu, C. Zhao, J. Benedikt, and K. Kang, "A 5-Gb/s 66 dB CMOS variable-gain amplifier with reconfigurable DC-offset cancellation for multi-standard applications," *in IEEE Access*, vol. 6, pp. 54139-54146, 2018.

[7] M. J. Uddin *et al.*, "A CMOS power splitter for 2.45 GHz ISM band RFID reader in 0.18 µm CMOS technology," *Technical Gazette*, vol. 20, pp. 125-129, 2013.

[8] M. A. S. Bhuiyan *et al.*, "Design trends in fully integrated 2.4 GHz CMOS SPDT switches," *Current Nanoscience*, vol. 10, pp. 334-343, 2014.

[9] M. Asemani *et al.*, "Improving linearity of CMOS variable-gain amplifier using third-order intermodulation cancellation mechanism and intermodulation distortion sinking techniques," *International Journal of Engineering*, vol. 30, pp. 192-198, 2017.

[10] R. Oneț, M. Neag, I. Kovács, M. D. Țopa, S. Rodriguez, and A. Rusu, "Compact variable gain amplifier for a multistandard WLAN/WiMAX/LTE receiver," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 1, pp. 247-257, Jan 2014.

[11] M. T. I. Badal *et al.*, "Low power high-efficiency shift register using implicit pulse-triggered flip-flop in 130 nm CMOS process for a cryptographic RFID tag," *Electronics*, vol. 5, no. 4, pp. 92, 2016.

[12] M. A. S. Bhuiyan *et al.*, "Design of an active inductor based LNA in Silterra 130 nm CMOS process technology," *Journal of Microelectronics, Electronic Components and Materials*, vol. 45, no. 3, pp. 181-194, 2015.

[13] M. T. I. Badal, M.B.I. Reaz, M.A.S. Bhuiyan, and Chitra A. Dhawale, "Nano CMOS charge pump for readerless RFID PLL," *Journal of Microelectronics, Electronic Components and Materials*, vol. 49, no. 2, pp. 53-60. 2019.

[14] M. A. S. Bhuiyan *et al.*, "Design architectures of the CMOS power amplifier for ISM band applications: An overview," *Electronics*, vol. 8. no. 5, pp. 477, 2019.

[15] M. T. I Badal *et al.*, "Advancement of CMOS transimpedance amplifier for optical receiver," *Transactions on Electrical and Electronic Materials*, vol. 19, no. 2, pp. 73-84, 2019.

[16] M. T. I. Badal *et al.*, "High-resolution time to digital converter in 0.13 µm CMOS process for RFID phase locked loop," *Journal of Engineering Science and Technology*, vol. 14, no. 4, pp. 1776-88, 2019.

[17] Chan Tat Fu and Howard Luong, "A CMOS linear-in-dB high-linearity variable-gain amplifier for UWB receivers," *2007 IEEE Asian Solid-State Circuits Conference*, Jeju, pp. 103-106, 2007.

[18] H. D. Lee, K. A. Lee, and S. Hong, "A wideband CMOS variable gain amplifier with an exponential gain control," *in IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 6, pp. 1363-1373, June 2007.

[19] M. Dongi and M. Jalali, "A wideband CMOS VGA with dB-linear gain based on active feedback and negative capacitance," *Iranian Conference on Electrical Engineering (ICEE)*, Tehran, pp. 506-510, 2017.

[20] Khumsat P., Thanachayanont A., and Sakphrom S., "A compact class-AB CMOS variable gain amplifier," *ECTI International Conference*, pp. 85-88, 2007.

[21] L. He, L. Li, D. Zhao, and Z. Wang, "A low-power wide gain range digitally controlled variable gain amplifier with a wide tuning bandwidth for 60 GHz applications," *IEEE 17th Annual Wireless and Microwave Technology Conference (WAMICON)*, Clearwater, FL, pp. 1-4, 2016.

[22] H. Liu *et al.*, "A wideband analog-controlled variable-gain amplifier with dB-linear characteristic for high-frequency applications," *in IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 2, pp. 533-540, Feb 2016.

[23] Ghanavati B., "Low-voltage high dynamic range CMOS exponential function generator," *Applied mathematics in Engineering, Management and Technology*, vol. 3, pp. 250-256, 2015.

[24] L. Qianqian *et al.*, "CMOS linear-in-dB VGA with DC offset cancellation for direct-conversion receivers," *Journal of Semiconductors*, vol. 32, pp. 105007, 2011.

[25] H. Elwan, A. Tekin, and K. Pedrotti, "A differential-ramp based 65 dB-linear VGA technique in 65 nm CMOS," *in IEEE Journal of Solid-State Circuits*, vol. 44, no. 9, pp. 2503-2514, Sept 2009.

[26] Y. Yu, Y. Yang, and Y. E. Chen, "A compact wideband CMOS low noise amplifier with gain flatness enhancement," *in IEEE Journal of Solid-State Circuits*, vol. 45, no. 3, pp. 502-509, March 2010.

BIOGRAPHIES OF AUTHORS

Md Joherul Alam was born in Bangladesh in 1993. Currently he is working as a graduate engineer at Vibe Tech Australia. He received his Bachelor of Eng. degree in electrical and electronic engineering from Universiti Tenaga Nasional (UNITEN) in 2016. His research interests include Electronics, Signal processing, Electro materials, Synthesis and characterisation, RFIC design, VLSI design, Microchip design, and Fabrication.

Mohammad Arif Sobhan Bhuiyan was born in Chittagong, Bangladesh in 1985. He received his B.Sc. and M.Sc. degree in Applied Physics, Electronics and Communication Engineering from the University of Chittagong, Bangladesh, in 2006 and 2007, respectively. He received his PhD from Universiti Kebangsaan Malaysia, Malaysia in 2017. He is currently an Assistant Professor at the department of Electrical and Electronics Engineering, Xiamen University Malaysia, Malaysia. His research interest is in the field of VLSI and Wireless Communication.

Mamun Bin Ibne Reaz was born in Bangladesh, in December 1963. He received his B.Sc. and M.Sc. degree in Applied Physics and Electronics, both from University of Rajshahi, Bangladesh, in 1985 and 1986, respectively. He received his D.Eng. degree in 2007 from Ibaraki University, Japan. He is currently a Professor in the Department of Electrical, Electronic and Systems Engineering, Universiti Kebangsaan Malaysia, Malaysia involving in teaching, research and industrial consultation. He is a Senior Associate of the Abdus Salam International Centre for Theoretical Physics (ICTP), Italy since 2008. He is also a Senior Member of IEEE. He has vast research experiences in Japan, Italy and Malaysia. He has published extensively in the area of IC Design, Biomedical application IC and Smart Home. He is author and co-author of more than 300 research articles in design automation, IC design for biomedical applications and Smart Home. He is also the recipients of more than 50 research grants (national and international).

Mohammad Torikul Islam Badal was born in Bangladesh in 1992. Currently he is doing his PhD in Silicon based Photonics in the department of Electrical and Telecommunication Engineering at RMIT University, Australia. He received his Master in Science from Universiti Kebangsaan Malaysia (UKM) in 2018 and B. Eng degree in electrical and electronic engineering from Universiti Tenaga Nasional (UNITEN) in 2015. His research interests include Silicon Photonics, Microelectronics, RFIC design, VLSI design, Microchip design, and Fabrication.

Noorfazila Kamal Noorfazila Kamal was born in Perak, Malaysia in 1979. From 1997 to 2000, she was educated at Universiti Teknologi Malaysia (UTM), in Johor Bharu, Malaysia, where she obtained a Bachelor's Degree in Computer Engineering with honour. In 2001 she worked as a tutor in the The Department of Electrical, Electronic and Systems Engineering, Universiti Teknologi Malaysia. In October 2002, she joined The Department of Electrical, Electronic and Systems Engineering, Universiti Kebangsaan Malaysia. In October 2005, she was granted a scholarship from Ministry of Higher Education Malaysia to pursue her study at School of Electrical & Electronic Engineering, The University of Adelaide. Currently She is a Senior Lecturer in Universiti Kebangsaan Malaysia. Her research interest include low power RFIC design for different applications.