E/W-Band CPW-based Amplifier MMICs Fabricated in a 60 nm GaN-on-Silicon Foundry Process

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***Abstract* — This paper presents an experimental evaluation of two co-planar waveguide (CPW) based E/W-band amplifier MMICs realised in a 60 nm GaN-on-Si foundry process. A one-stage amplifier and a two-stage amplifier realised in this process have a measured maximum gain of 8 dB and 16 dB at 73-74 GHz, respectively. The two amplifiers have a measured gain of 3 dB and 7 dB at 93 GHz when the drain voltage (V_d) is 10 V and the drain current (I_d) is 15 mA per stage. The two-stage amplifier has a measured noise figure (NF) of 2.7-3.8 dB and 2.9-4.1 dB at 90-95 GHz when the I_d is 10 mA and V_d is 5 V and 10 V, respectively. The measured NF of this amplifier is equal to 4-6 dB at 92-95 GHz when an I_d of 10-20 mA is used in each stage with same drain bias.**

***Keywords* — 60 nm GaN-on-Si MMIC process, W-band amplifiers, noise characterization, power handling.**

I. Introduction

Gallium Nitride-on-Silicon (GaN-on-Si) semiconductor processes have recently emerged as a viable option for Monolithically Microwave Integrated Circuits (MMICs) targeting wireless communications and radar applications up to the millimetre (mm)-wave range incl. e.g. 5G NR solutions [1-6]. The power handling capabilities of GaN-on-Si transistors are not as high as that of GaN-on-Silicon Carbide (GaN-on-SiC) based active devices but Silicon wafers are cheaper and more easily available on the global market. GaN-on-Si technologies have also the potential to scale the wafer dimensions up to 6-8" and beyond thereby reducing the chip fabrication cost. It can be highly attractive to use the same technology for Transmit and Receive Modules (TRM), especially in the mm-wave range where applications such as e.g. 5G may require compact electronically steerable active antenna arrays [3-6]. Presently, there are few open foundries in Europe and overseas that can offer GaN-on-Si MMICs at 30 GHz and beyond. A 10 W power amplifier (PA) and a single-chip 3W TRM with 3 dB noise figure (NF) at Ka-band were realised by the foundry OMMIC in a 100nm GaN-on-Si process [4]. Recently, OMMIC has developed a 60 nm GaN-on-Si process targeting E-band wireless communication and W-band short-range radar applications (i.e. at 60-110 GHz). A microstrip 60 nm GaN-on-Si PA shows an output power of 28 dBm at 89 GHz and 21 dBm at 94 GHz (i.e. last stage transistors can deliver 14-20 dBm) [5]. OMMIC's 60 nm GaN-on-Si process (D006GH) may be used for high-power and low-noise MMICs up to W-band (75-110 GHz). Here, we present experimental and simulated results of grounded co-planar waveguide (CPW) based E/W-band MMICs fabricated in this advanced foundry process. The results include small-signal s-parameters, noise figure (NF) and large-signal data up to 110 GHz. A two-stage amplifier realised using this process has a measured NF around 3-4 dB at 90-95 GHz when the drain current (I_d) is 5 mA per stage and the drain voltage (V_d) is 5-10 V. This amplifier has a measured NF of 4-6 dB at 92-95 GHz when an I_d of 10-20 mA is used in each stage to obtain a higher gain and linearity. The presented two-stage amplifier has a measured gain of 6.5-7.6 dB at 92-95 GHz when V_d is 10 V and I_d is equal to 15 mA per stage. The measured output 1 dB compression (P1dB) is 9 dBm and 13 dBm when V_d is 10 V and I_d is 14 mA and 28 mA per stage, respectively.

II. 60 nm GaN-on-Si Passive and Active Test Circuits

Further details on OMMIC's 60 nm GaN-on-Si MMIC process can be found in [4-6]. Microstrip lines made on 100 µm thick GaAs substrates may be used up to 80 GHz as the substrate thickness should be limited to about a tenth of the guided wavelength to prevent undesired higher-order transmission modes from occurring. This explains the use of CPWs in our E/W-band MMIC designs as the GaN-on-Si substrate thickness used here is 100 µm and the dielectric constant of Si is similar to that of GaAs. Passive and active CPW test structures were simulated in ADS/EMPro using the foundry-provided process design kit and on-wafer s-parameter measurements were done with RF probes connected to an HP 8510C/8510XF network analyzer. Fig. 1a shows a micrograph of a 2.3 mm long (50 Ω) CPW line included on the same process run to determine the transmission line properties. Fig. 1b shows that the measured and EM-simulated forward transmission and input reflection coefficients (s_{21} and s_{11}) of this CPW line are in a relatively close agreement. The measured and simulated transmission losses are equal to 0.3-1.4 dB and 0.4-2.1 dB at 2-110 GHz, respectively (i.e. up to 0.6 dB/mm and 0.9 dB/mm). The measured s_{11} is below -18 dB in this frequency range.

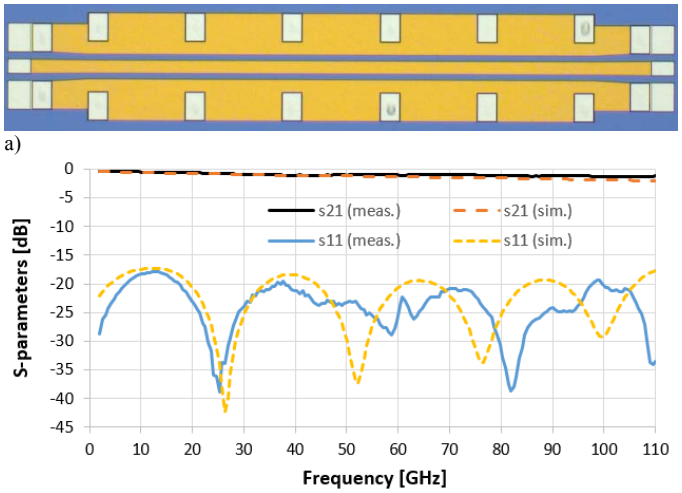


Fig. 1. a) Micrograph of a 2.3 mm long CPW line fabricated in a 60 nm GaN-on-Si MMIC process and b) measured and simulated forward transmission s_{21} and input reflection s_{11}, respectively.

The active CPW based MMICs that were fabricated on the same 60 nm GaN-on-Si process run included also more fundamental test structures such as HEMT devices with a different number of gate fingers (n) and unit gate width (W_u). Fig. 2a shows a micrograph of a HEMT device with the total gate width (W_g) dimensions equal to 2x22 µm. On-wafer measured and simulated s-parameters of this transistor with an applied drain-to-source voltage (V_{ds}) of 5.5 V and a drain-to source current (I_{ds}) equal to 15.7 mA are shown in Fig. 2b. The measured and simulated s_{21} are equal to 2.3-9.7 dB and 2.7-10.6 dB at 2-110 GHz, respectively. The measured reverse transmission (s_{12}) is below -13.6 dB (sim. better than -15 dB). The reference planes during these measurements were moved to the gate and drain terminals after calibration was done with dedicated on-wafer TRL standards. The target frequency range of this MMIC component design investigation is E/W-band or more precisely at 92-95 GHz for certain identified dual-use applications (radar, communication). Thus, it is important to specify how the small-signal gain at those frequencies is effected by the chosen transistor dimensions and DC bias point. The measured gain of a device with almost the double gate width size (2x40 µm) and V_{ds}=8 V, I_{ds}=26.0 mA is 3.0-3.1 dB at 92-95 GHz whereas the 2x22 µm transistor with V_{ds}=5.5 V, I_{ds}=15.7 mA results in a 0.7-0.8 dB higher gain at 92-95 GHz (s_{21}=3.8 dB). The current densities of these two devices are similar and the smaller gate width size can obtain a higher gain (lower noise) but inferior linearity.

III. W-Band GaN-on-Si CPW-Based Amplifier MMICs

Figures 3a and 3b show circuit schematic and micrograph of a one-stage CPW E/W-band amplifier MMIC fabricated in a 60 nm GaN-on-Si foundry process (the area is 950x814 µm^2). The gate and drain voltages (V_g and V_d) are applied using the two DC bias lines that each are connected to a tee-junction close to the gate and drain terminals, respectively.

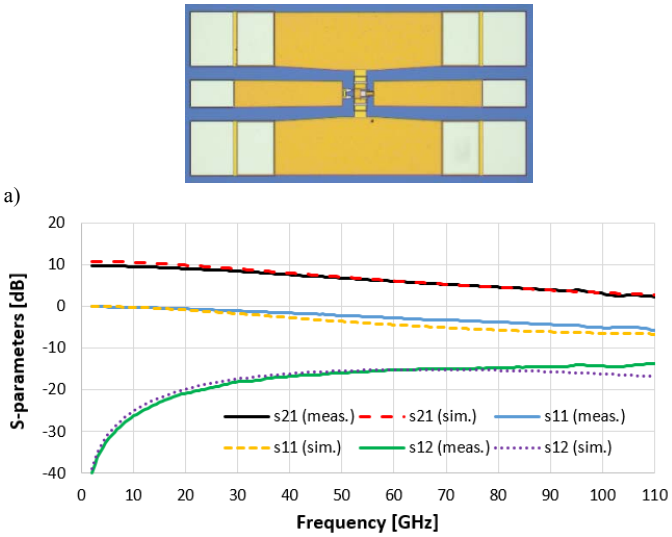


Fig. 2. a) Micrograph of a 60 nm GaN-on-Si HEMT device (2x22 µm gate width) and b) measured and simulated s-parameters (V_{ds}=5.5 V, I_{ds}=15.7 mA).

The input and output matching networks contain the series and shunt capacitors C_{in1}, C_{in2}, C_{g1}, C_{g2}, C_{d1} and C_{out} connected to the tee-junctions using different transmission lines (TL_i) [7]. On-chip resistors, 50 Ω at the input and in the gate supply as well as 20 Ω at the drain supply are used to ensure the amplifier is unconditionally stable. Figs. 4a and 4b show the corresponding circuit schematic and micrograph of a cascaded two-stage CPW amplifier MMIC in a 60 nm GaN-on-Si process (the area used is 1256x814 µm^2).

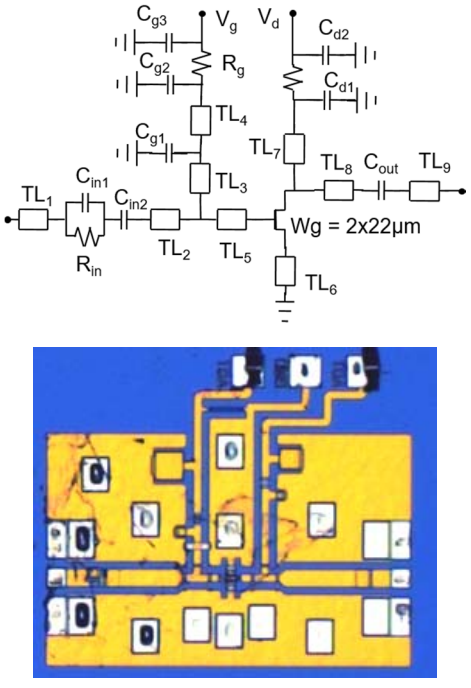
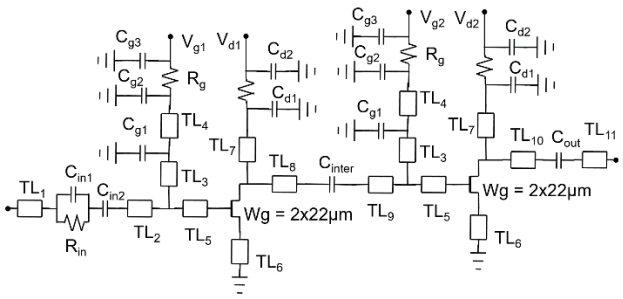


Fig. 3. a) Circuit schematic and b) micrograph of a single-stage CPW based E/W-band amplifier MMIC fabricated in a 60 nm GaN-on-Si foundry process.



a)

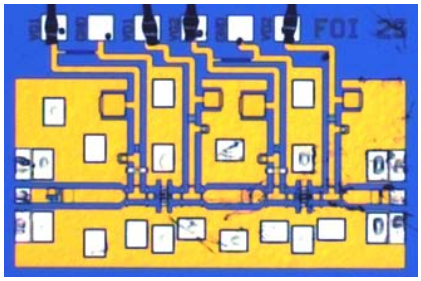


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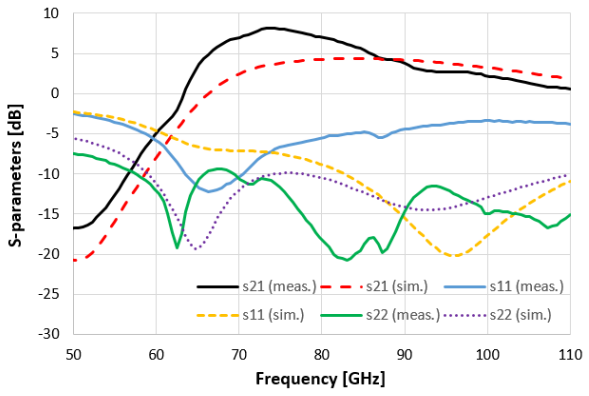
Fig. 4. a) Circuit schematic and b) micrograph of a cascaded two-stage CPW E/W-band amplifier MMIC fabricated in a 60 nm GaN-on-Si foundry process.

The 1-stage and 2-stage GaN-on-Si E/W-band amplifier MMICs were characterised using RF probes after assembly in a DC bias test fixture with some additional off-chip decoupling capacitors. Measured and simulated s-parameters of those amplifier designs at two different DC bias points are shown in Figs. 5a-d, respectively. The amplifier MMICs were simulated in ADS/EMPro using the EM-simulated results of the passive structures and the foundry transistor model (W_g=2x22 µm). During characterisation and in the simulations the drain DC bias current (I_d) and V_d of the 1-stage amplifier were initially set to 18 mA and 5.5 V, respectively. The measured maximum s_{21} is then 8.2 dB at 73.8 GHz and s_{21}=2.7-3.1 dB at 91.6-95.4 GHz. Compared with the simulated s_{21} which peaks at 84 GHz (4.3 dB) the measured s_{21} curve below 70 GHz is shifted 2-5 GHz towards lower frequencies. The measured gain is up to 4.6 dB higher than simulated below 87 GHz while it is 1 dB lower than anticipated above 92 GHz. Whereas the measured and simulated output return losses are in a relatively close over-all agreement (s_{22}<-9 dB above 56 GHz and 58 GHz, respectively) the measured minimum s_{11} occurs at a much lower frequency than simulated (at 66.3 GHz compared with at 96 GHz). Simulations imply that this discrepancy may be explained by a difference in the measured and simulated s_{11} data that was found from the on-wafer characterisation of transistors with the same dimensions as used in the two amplifier designs (2x22 µm).

For the 1-stage amplifier the measured max gain is reduced with 0.8 dB at 74.4 GHz when V_d =10 V and I_d=15 mA while s_{21} is increased with 0.2-0.4 dB to 3.1-3.3 dB at 91.6-95.4 GHz. Using a higher V_d and lower I_d causes a slightly higher amplifier gain at 92-95 GHz while gain is reduced at lower frequencies. The 2-stage amplifier has a measured gain of 16 dB at 72.7 GHz and s_{21}=5.3-6.5 dB at 91.8-95.1 GHz when V_d =5.5 V, I_d=36 mA while s_{21} is increased with 1.1-1.2 dB to 6.5-7.6 dB at 91.8-95.1 GHz when V_d =10 V and I_d=30 mA (see Figs. 5c and 5d).



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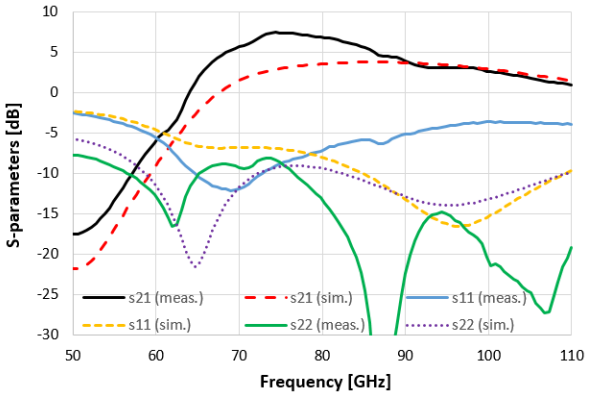

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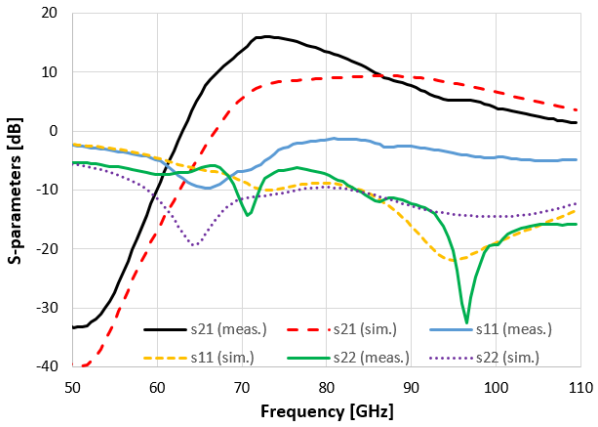

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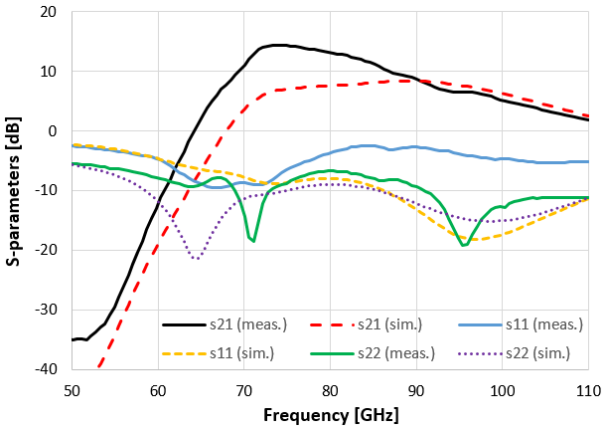

d)

Fig. 5. Measured and simulated s-parameters of two GaN-on-Si E/W-band amplifier MMICs: a) 1-stage (V_d=5.5 V, I_d=18 mA), b) 1-stage (V_d=10 V, I_d=15 mA), c) 2-stage (V_d=5.5 V, I_d=36 mA), b) 2-stage (V_d=10 V, I_d=30 mA).

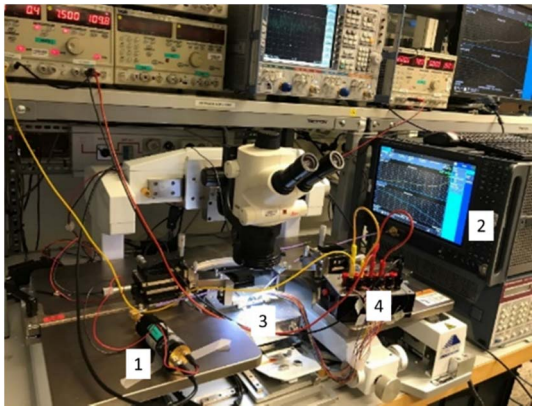

Fig. 6. Measurement setup for the 90-100 GHz noise figure characterisation (1. noise source, 2. spectrum analyser, 3. Probe station and 4. DC bias connections).

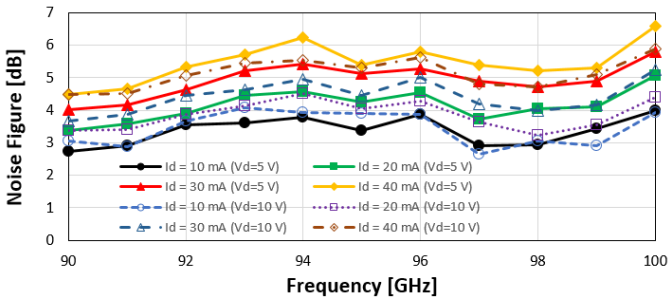

Fig. 7. Measured noise figure data of a two-stage 60 nm GaN-on-Si amplifier MMIC at 90-100 GHz (I_d=10-40 mA and V_d=5V and 10 V, respectively).

Noise figure characterisation was done using a Keysight N9041B UXA spectrum analyser with built in software for noise figure measurements (see Fig. 6). A Millitech 90-100 GHz noise source (NSS-10-R1520) was connected to the input of the Device Under Test (DUT) via an adapter, cable and RF probe (an RF probe and a cable was also used to connect to the 110 GHz spectrum analyzer used). The compensation for the expected losses due to the different interconnects in the noise figure measurement set-up is done in the instrument's noise figure analyser mode. Figure 6 shows the measured NF data of a 2-stage GaN-on-Si amplifier at different values of I_d and V_d. This 2-stage amplifier has a measured NF of 2.7-3.8 dB and 2.9-4.1 dB at 90-95 GHz when I_d is 10 mA and V_d is equal to 5V and 10V, respectively. The measured NF is in the range of 4-6 dB at 92-95 GHz when I_d is 20-40 mA (10-20 mA per stage) to enable a higher amplifier gain and linearity. Compared with some earlier W-band GaN-on-SiC amplifiers which reported similar noise figures (3-6 dB) [7-8] GaN-on-Si amplifiers used e.g. in single-chip front-ends may be an interesting alternative for applications where a higher level of integration (lower cost) and low noise/high linearity are required.

The large-signal properties were determined using an RF signal generator connected to a W-band up-converter as the power source at the input of the DUT and the calibrated amplifier output power level was then measured with a W-band power sensor. The tested amplifier MMICs were connected to measurement equipment using RF probes, cables and an adapter. The measured 1 dB compression point (P_{1dB}) is 9 dBm and 13 dBm at 95 GHz when V_d=10 V and I_d is 14 mA and 28 mA per stage, respectively. The measured saturated output power level is 15 dBm at 95 GHz. Compared with a 2-stage amplifier realised in a 50 nm GaN-on-Si process that reached 0.68 W/mm at 94 GHz (using a 2x50 µm device) [2] this result corresponds to a slightly higher power density of 0.72 W/mm even though smaller devices (2x22 µm) are used in the two amplifier designs.

IV. Conclusion

We presented an experimental evaluation of two CPW based E/W-band amplifier MMICs realised in a 60 nm GaN-on-Si open foundry process. A one-stage amplifier and a two-stage amplifier realised in this process have a measured maximum gain of 8 dB and 16 dB at 73-74 GHz, respectively. The two amplifiers have a measured gain around 3 dB and 7 dB at 92-95 GHz when V_d is 10 V and the I_d in each stage is 15 mA. The two-stage amplifier has a measured NF of 2.7-3.8 dB and 2.9-4.1 dB at 90-95 GHz when I_d is 5 mA per stage and V_d is 5V and 10 V, respectively. The measured NF is equal to 4-6 dB at 92-95 GHz when the I_d is 10-20 mA per stage. The measured output 1 dB compression occurs at 9 dBm and 13 dBm at 95 GHz when V_d is 10 V and I_d is 14 mA and 28 mA per stage, respectively. The measured saturated output power level is 15 dBm at 95 GHz. This translates to a relatively high power density of 0.72 W/mm for the 2x22 µm gate width devices used in the two amplifier designs. These results indicate extended possibilities of using low noise and high linearity GaN-on-Si amplifiers in highly integrated multifunctional single-chip front-ends as lower cost alternatives to GaN-on-SiC RF modules for E-band communication and W-band radar sensors.

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