Algorithms and Devices for Noncoherent Digital Radio Signal Processing

Oleg V. Chernoyarov, Alexey N. Glushkov, Vladimir P. Litvinenko, Boris V. Matveev, and Alexander A. Makarov

***Abstract*—From a single point of view, there are presented the digital noncoherent algorithms and devices for detecting and demodulating radio signals. These algorithms are introduced as requiring the least possible number of simple arithmetic operations to be implemented because they are based on the basic fast algorithm for digital processing of narrowband signals. The devices are presented for detecting arbitrary narrow-band radio signals or phase shift keyed signals, demodulating amplitude shift keyed, frequency shift keyed or differential phase shift keyed signals as well as for demodulating the signals that are phase-shift keyed in toto. The characteristics of the specified devices are considered and their noise immunity in Gaussian noise is estimated. The theoretical results obtained are confirmed by computer simulation.**

***Index Terms*—Noncoherent processing, signal detection, digital demodulation, modulated high-frequency signal, frequency selectivity, optimal reception, noise immunity**

I. Introduction

Processing of modulated high-frequency signals from the intermediate frequency receiver section output involves solving the problems of their detection or demodulation. In modern radio engineering, digital signal processing (DSP) has expanded intensively [1], [2]. In general terms, it includes, first, the signal sampling by an analog-to-digital converter (ADC) with the sampling frequency f_S determined by both the signal properties and the problem to be solved and then the subsequent calculation of the desired values by which the required decisions are made.

Coherent processing [3] includes phase locking of the received signal and the clock (reference) ADC generator. This provides maximum noise immunity of the decisions made, but requires more complex DSP equipment for its practical implementation.

Noncoherent processing [3] involves the formation of two quadrature channels by means of two reference generators whose signals are shifted by 90^o in phase (or a quarter-period in time). In this case, phase locking of the reference generator is not required, but the noise immunity of the made decisions is decreased.

When digital processing of high-frequency signals in real time is used, its performance can be determined by the number of arithmetic operations that must be carried out in software (based on digital signal processors) or hardware (based on field-programmable gate arrays) implementation of the algorithm over the period of the carrier frequency. Then, the actual problem is to develop fast algorithms and devices for digital signal processing [4] that provide the minimum number of simple arithmetic operations over signal period.

II. The Basic Algorithm for Noncoherent Processing of the Narrowband Radio Signal

The narrowband radio signal can be represented in the form

$$s(t) = S(t)\cos\left[2\pi f_0 t + \psi(t)\right]. \quad (1)$$

There f_0 denotes the carrier frequency, while $S(t)$ and $\psi(t)$ are the designations of the amplitude and the initial phase respectively that are slowly changing functions of time. To implement its quadrature processing, sampling by means of ADC is necessary through quarter-period $T_0/4 = 1/4 f_0$ [5], while the sampling frequency is equal to

$$f_S = 4 f_0. \quad (2)$$

Fig. 1 demonstrates the sampling procedure. There s_{1i}, s_{2i}, s_{3i} and s_{4i} denote the signal samples within the *i*-th period. Fig. 2 shows the block diagram of the device for time sampling. The samples s_{1i}, s_{2i}, s_{3i}, s_{4i} are divided into two sequences containing even and odd samples so that

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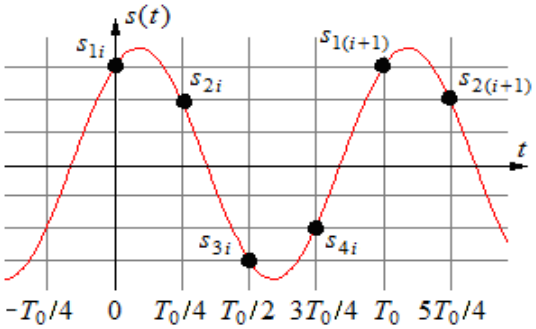

Fig. 1. Time diagram of the signal sampling.

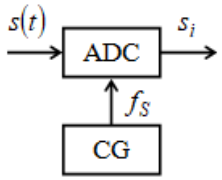

Fig. 2. The block diagram of the device for time sampling.

within each current period two quadrature samples are formed as follows

$$\begin{cases} x_{1i} = s_{1i} - s_{3i} = 2S\cos(\psi), \\ x_{2i} = s_{2i} - s_{4i} = 2S\sin(\psi). \end{cases} \quad (3)$$

Here S and ψ are the current amplitude and initial phase. From (3), it follows that the equality of the form of $\sqrt{x_{1i}^2 + x_{2i}^2} = 2S$ is satisfied.

For each period, there are calculated the differences of even and odd samples (3) then summarized for the last N periods:

$$\begin{aligned} y_{0i} &= \sum_{j=0}^{N-1} x_{1(i-j)} = \sum_{j=0}^{N-1} \left[s_{1(i-j)} - s_{3(i-j)} \right], \\ y_{1i} &= \sum_{j=0}^{N-1} x_{2(i-j)} = \sum_{j=0}^{N-1} \left[s_{2(i-j)} - s_{4(i-j)} \right]. \end{aligned} \quad (4)$$

Based on the differences x_{1i} and x_{2i} (3), the quadrature channels of signal processing are made while the sequences of these samples are shifted by quarter-period in time or by 90° in phase.

The calculation of the sums (4) for one period requires $2N$ subtraction and $2(N-1)$ summation operations. Thus, when the value of N is big, the direct implementation of the steps (4) leads to significant computational costs. For their decreasing, one takes into account that for each subsequent period the substantial part of operations is repeated many times.

The fastest (with the minimum number of operations) calculation of sums (4) is achieved, if $N = 2^n$ (where n is an integer). In Fig. 3, there is shown the block diagram of the fast basic algorithm for the noncoherent signal processing, while in Fig. 4 one can see its symbolic representation in the form of BA_n.

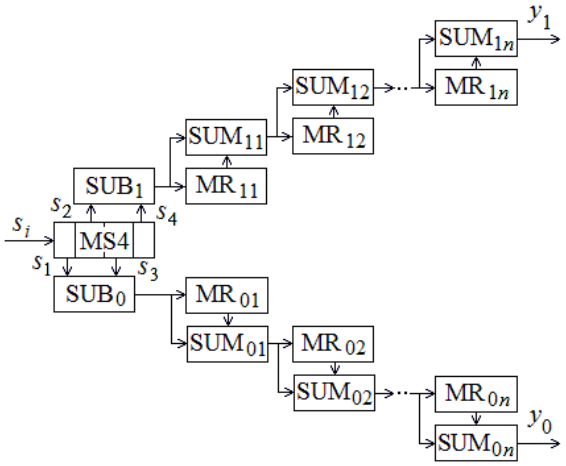

Fig. 3. The block diagram of the fast basic algorithm for the noncoherent processing of modulated radio signals.

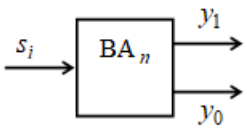

Fig. 4. The symbolic representation of the fast basic algorithm for the noncoherent processing of modulated radio signals.

The input signal $s(t)$ (1) is fed to the input of ADC which generates four samples over each signal period using a clock generator (CG). These samples are first transferred to the multibit shifter (MS4) that contains four samples. And only then the computational procedure (4) can be started.

In the subtractors SUB_0 and SUB_1, one computes the differences of odd x_{1i} and even x_{2i} samples (2). Then, one summarizes them with the content of multibit registers MR_{01} and MR_{11} containing the value x_{1i} and x_{2i}, respectively, that have been received during the previous processing period. The resulting sums of the two samples differences $x_{1i} + x_{1(i-1)}$ and $x_{2i} + x_{2(i-1)}$ are generated at the SUM_{01} and SUM_{11} outputs. After that, new values x_{1i} and x_{2i} are inserted into registers MR_{01} and MR_{11} replacing their previous content.

At the next stage, one calculates the sums of the four adjacent samples differences $x_{1i} + x_{1(i-1)} + x_{1(i-2)} + x_{1(i-3)}$ and $x_{2i} + x_{2(i-1)} + x_{2(i-2)} + x_{2(i-3)}$ in the summators SUM_{02} and SUM_{12}. Here, in the last cells of the multibit shifters MR_{02} and MR_{12}, occupying two memory cells each, one can see $x_{1(i-2)} + x_{1(i-3)}$ and $x_{2(i-2)} + x_{2(i-3)}$. Later on, the shift of the contents of the registers takes place, with out-of-date values being lost, while the values $x_{1i} + x_{1(i-1)}$ and $x_{2i} + x_{2(i-1)}$ saved in SUM_{01} and SUM_{11} are now transferred to the first register cells, free again at the moment. Then the device repeats the operation with that only difference that the number of memory cells in the multibit shifters is now changing from 4 to 8 and so forth, up to $2^{n-1} = N/2$, so that the sums of 8, 16 and more of the last received differences can be found. The last step of the algorithm is the computation of the responses of quadrature

channels y_{0i} and y_{1i} (4) in the summators SUM_{0n} and SUM_{1n}.

III. Digital Radio Signal Detector

A radio signal with an arbitrary modulation format can be described by the expression (1) with the specified properties of the slowly changing amplitude $S(t)$ and phase $\psi(t)$. Then the block diagram of the device for detecting an arbitrary radio signal has the form shown in Fig. 5.

By the responses y_{0i} and y_{1i} of the quadrature channels of the basic algorithm (Fig. 3), and under the signal amplitude $S(t)$ and phase $\psi(t)$ slowly changing over N periods, the value

$$z_i = \sqrt{y_{0i}^2 + y_{1i}^2} \approx NS(t_i) \tag{5}$$

is calculated in the quadratic block QT which provides the estimate of the received radio signal amplitude. In the resolver RS, the processing result z_i (5) is compared with the set threshold z_0 and if the threshold is exceeded then the decision R is made that the signal is present, otherwise – that it is absent.

The amplitude-frequency characteristic (AFC) of the detector is determined by the expression [6]

$$H(f) = \left|\sin(N\pi f / f_0)/\cos(\pi f / 2 f_0)\right|. \tag{6}$$

The form of AFC (6) is shown in Fig. 6, its pass band W_0 determined by the first zeros of AFC is equal to

$$W_0 = 2\Delta f = 2 f_0 / N. \tag{7}$$

The necessary requirement to be fulfilled to be able to determine the optimal threshold z_0 is to estimate the noise level at the detector output. It can be implemented through to the partial suppression of the signal component in the threshold z_0 estimation channel.

The block diagram of the radio signal detector applied for the estimation of the noise level [6] is presented in Fig. 7. As it can be seen, it includes the $(n-1)$-step basic algorithm BA_{n-1} with the subsequent summation of its output signals in the summators SUM_{0n} and SUM_{1n} and the formation of their differences in the subtractors SUB_{01} and SUB_{11}. As a result, the values (4) and

$$\begin{aligned} y'_{0i} &= \sum_{j=0}^{N/2-1} x_{1(i-j)} - \sum_{j=N/2}^{N-1} x_{1(i-j)}, \\ y'_{1i} &= \sum_{j=0}^{N/2-1} x_{2(i-j)} - \sum_{j=N/2}^{N-1} x_{2(i-j)} \end{aligned} \tag{8}$$

are calculated, while the values (5) and

$$z'_i = \sqrt{y'^2_{0i} + y'^2_{1i}} \tag{9}$$

are generated at the outputs of the quadratic blocks QT_1 and QT_2, respectively.

The value z_0 in the threshold former TF is set by averaged values of z'_i with the weight coefficient α which is determined according to the chosen optimality criterion [7].

In Fig. 8, by the dashed line there is shown the normalized AFC $H'(f - f_0)/2N$ of the channel of noise level estimation (9), while by the solid line – the AFC $H(f - f_0)/2N$ (6) of the channel of signal extraction [6]. From Fig. 8, it follows that in the channel of noise level estimation z'_i the signal is suppressed in the neighborhood of the carrier frequency.

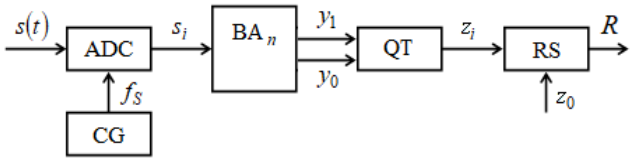

Fig. 5. The block diagram of the detector of an arbitrary radio signal with slowly changing amplitude and initial phase.

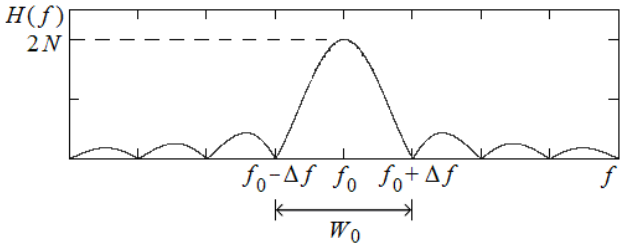

Fig. 6. The amplitude-frequency characteristic of the radio signal detector.

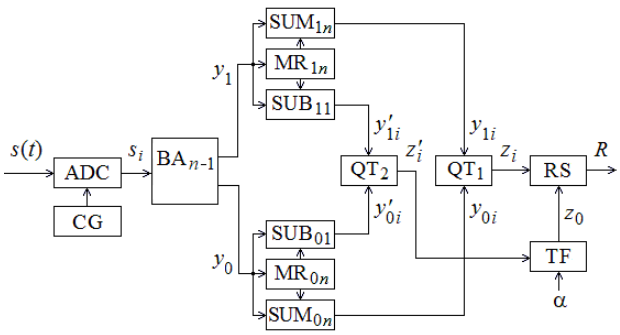

Fig. 7. The block diagram of the radio signal detector that estimates the noise level.

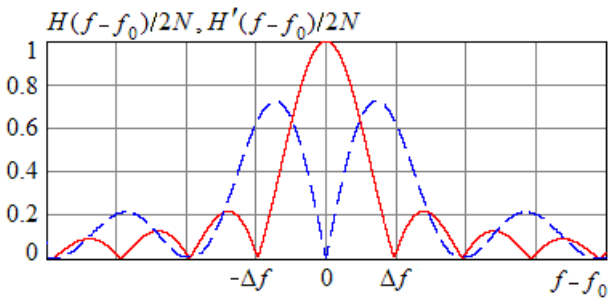

Fig. 8. The amplitude-frequency characteristics of the noise level estimation and signal extraction channels.

In Fig. 9, the dependences of z_i and z'_i are drawn upon the current period number while $N = 1024$ and the signal-to-noise ratio (SNR) [6]

$$h^2 = NS/\sigma_n^2 \tag{10}$$

is equal to 17 dB. Here σ_n^2 is the dispersion (mean power) of the noise.

If the signal is distorted by the Gaussian noise with independent samples and dispersion σ_n^2 [8], then in the signal presence the response z (5) is described by Rice distribution with the probability density [6]

$$w_s(z) = \frac{z}{2N\sigma_n^2}\exp\left[-\frac{z^2+(2NS)^2}{4N\sigma_n^2}\right]\mathrm{I}_0\left(\frac{Sz}{\sigma_n^2}\right),$$

while in the signal absence – by Rayleigh distribution with the probability density

$$w_n(z) = z\exp\left(-z^2/4N\sigma_n^2\right)/2N\sigma_n^2 . \tag{11}$$

In this case, for the set threshold z_0 the missing probability is determined as [6]

$$P_M = \exp\left(-\frac{h^2}{2}\right)\int_0^{u_0} u\exp\left(-\frac{u^2}{2}\right)\mathrm{I}_0(hu)\,\mathrm{d}u , \tag{12}$$

while the false alarm probability – as [6]

$$P_F = \exp\left(-u_0^2/2\right), \tag{13}$$

where $u_0 = z_0/\sigma_n\sqrt{2N}$. The dependences of P_M (12) (for the case when the SNR h (10) varies from 1 to 7) and P_F (13) are presented in Figs. 10a and 10b, respectively.

The response of the channel of noise level estimation is described by the Rayleigh probability density (11) and its mean value is equal to $z'_{\text{mean}} = \sigma_n\sqrt{\pi N}$. The estimate $\hat{z}'_{\text{mean}}$ of the mean value z'_{mean} can be obtained by the accumulation of the last received values of z'_k in the following way:

$$\hat{z}'_{\text{mean}} = \frac{1}{L}\sum_{k=1}^{L} z'_k .$$

Then for the threshold z_0, one gets

$$z_0 = \alpha\hat{z}'_{\text{mean}} .$$

In Fig. 11, by solid lines, there are shown the dependences of P_M and P_F upon the parameter α characterizing the detector immunity for various averaging sample sizes L. By dashed lines, the similar theoretical dependences are drawn while the threshold is known. As it

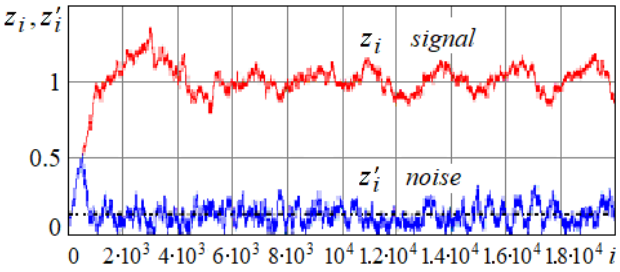

Fig. 9. The responses of the signal extraction and noise level estimation detector channels.

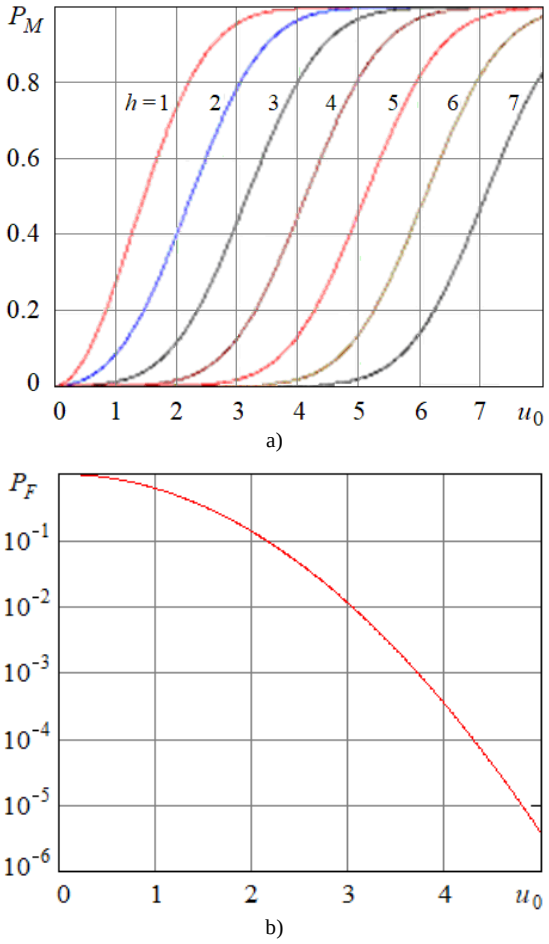

Fig. 10. The missing (a) and false alarm (b) probabilities while detecting an arbitrary radio signal.

can be seen, averaging the values of z'_k under $L > 20$ allows us to choose the value of α and to generate the estimate of the threshold level z_0 that provides the required noise immunity.

As it is well known, applying the phase shift keyed (PSK) signals makes it possible to implement the detector which provides high noise immunity. If the binary phase shift keying is used, then the radio signal (1) can be presented as

$$s(t) = S(t)\cos\left[2\pi f_0 t + \pi a(t)\right],$$

where $a(t) = 0$ or 1 is the modulating signal. While implementing the frequency doubling operation, the modulation is eliminated and the narrow-band (in the ideal case, harmonic) signal is produced which arrives to the input of the detector presented in Fig. 5 or 7.

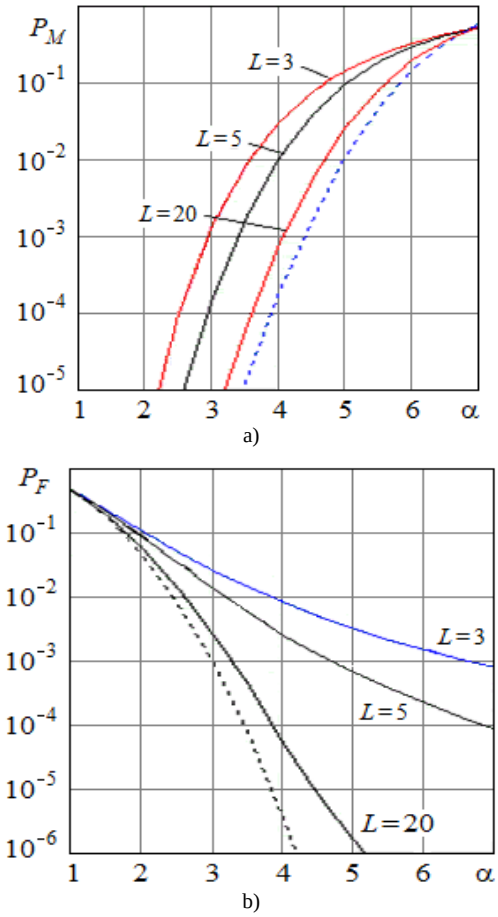

Fig. 11. The missing (a) and false alarm (b) probabilities while detecting an arbitrary radio signal.

In Fig. 12, there is presented the block diagram of the digital radio signal detector that can produce an improved estimate of the noise level of the narrowband signal. It is similar to the one that is shown in Fig. 7, but it provides an extended signal suppression band. Considering the circuit shown in Fig. 12, similarly to (8), one can get the following expressions for the responses of the channels of signal extraction and noise level estimation:

$$y'_{0i} = \sum_{j=0}^{N/4-1} x_{1(i-j)} - \sum_{j=N/4}^{N/2-1} x_{1(i-j)} - \sum_{j=N/2}^{3N/4-1} x_{1(i-j)} + \sum_{j=3N/4}^{N-1} x_{1(i-j)},$$
$$y'_{1i} = \sum_{j=0}^{N/4-1} x_{2(i-j)} - \sum_{j=N/4}^{N/2-1} x_{2(i-j)} - \sum_{j=N/2}^{3N/4-1} x_{2(i-j)} + \sum_{j=3N/4}^{N-1} x_{2(i-j)}. \quad (14)$$

According to (22), in Fig. 13, by the dashed line there is shown the normalized AFC $H''(f-f_0)/2N$ of the channel of noise level estimation, while by the dotted line – the AFC $H(f-f_0)/2N$ of the channel of signal extraction (Fig.6). As it follows from the comparison of the dependence $H''(f-f_0)/2N$ with the dependence $H'(f-f_0)/2N$ that is demonstrated in Fig. 8, the signal suppression frequency band in the neighborhood of $f-f_0=0$ does expand. It allows reducing the influence of the signal component on the estimate of the noise level.

The block diagram of the binary PSK signal detector [9] is shown in Fig. 14. In comparison with the circuit presented

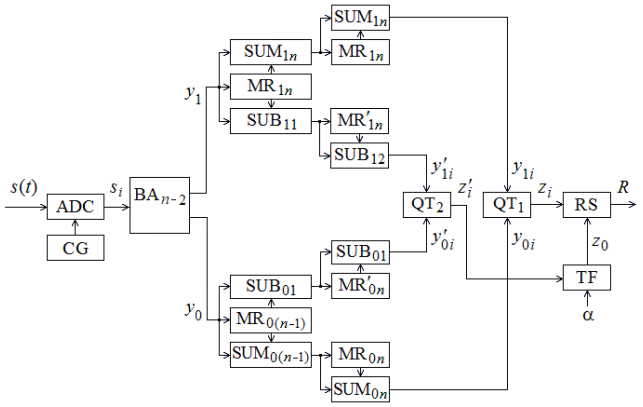

Fig. 12. The block diagram of the radio signal detector that estimates the noise level and provides an extended signal suppression band.

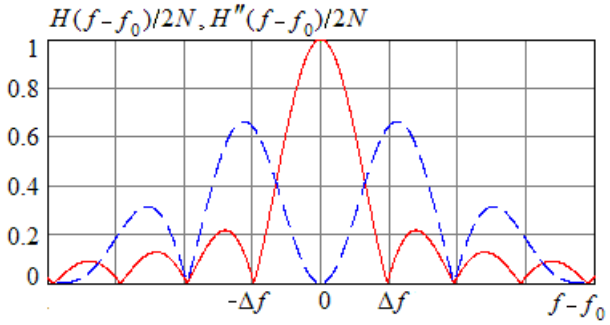

Fig. 13. The amplitude-frequency characteristics of channels of signal extraction and improved noise level estimation.

in Fig. 7 it additionally includes the frequency multiplier FM (with the multiplication factor of 2 or 4 for the binary or four-position phase shift keying, respectively). It can be implemented using the operations of calculating the module or multiplying the samples [9]. The sampling frequency is equal to $f_S = 8f_0$ for the binary PSK signal or $f_S = 16f_0$ for the four-position PSK signal.

In Fig. 15a, there is plotted the normalized spectrum $\tilde{G}_1(\Delta f_1) = G_1(\Delta f_1)/\max G_1(\Delta f_1)$ of the binary PSK signal passing through the filter with the pass band

$$W_1 = 312 \text{ kHz}, \quad (15)$$

while $\Delta f_1 = f - f_0$, the carrier frequency f_0 is 10 MHz and the symbol duration is 6.4 μs. In Fig. 15b, there is drawn the normalized spectrum of this signal $\tilde{G}_2(\Delta f_2) = G_2(\Delta f_2)/\max G_2(\Delta f_2)$, with $\Delta f_2 = f - 2f_0$, at the output of the frequency multiplier (doubler). As it can be

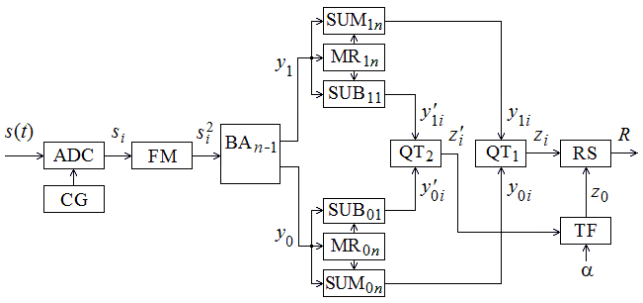

Fig. 14. The block diagram of the binary PSK signal detector that estimates the noise level.

seen, when the signal is doubled, its spectrum width narrows significantly and such signal can be extracted by the narrower detector.

In Fig. 16, the results of the statistical simulation of the PSK signal detector operation are presented. In this case, $N = 4096$ ($n = 12$), the pass band (7) is equal to $W_0 = 4.9$ kHz and it is much less than W_1 (15). The SNR at the detector input is 1.4 dB. It is presupposed that during the first time interval T_1 the mix of the PSK signal and the noise is observed and then only noise is received over the same interval. When the signal appears and disappears, the transient process of filling multi-bit shifters occurs in the detector.

As it can be seen, in stationary mode the reliable signal detection is ensured, even if the SNR is low enough.

IV. Digital Amplitude Shift Keyed Signal Demodulator

The block diagram of the amplitude shift keyed (ASK) signal demodulator with a passive pause is shown in Fig. 17. The sampling frequency is chosen according to (2) and the amplitude-frequency characteristic of the demodulator is the same as shown in Fig. 6.

In order to provide optimal matching of the demodulator with the received signal, the duration T_I of the signal information element should be $T_I = NT_0 = N/f_0$. In Fig. 18a, there are shown the timing diagrams of the normalized demodulator response $\tilde{z}_i = z_i / z_{\max}$ in the absence of interferences and in Fig. 18b – for the case when the signal is distorted by the band Gaussian noise while the SNR (10) is 20 dB. Here, by dotted line, the modulating signal is drawn. The decisions on the received information symbol (0 or 1) are made at the end of the signal element (when the ratio i/N is an integer).

It should be noted that the demodulator presented in Fig. 17 allows us to process multi-position ASK signals.

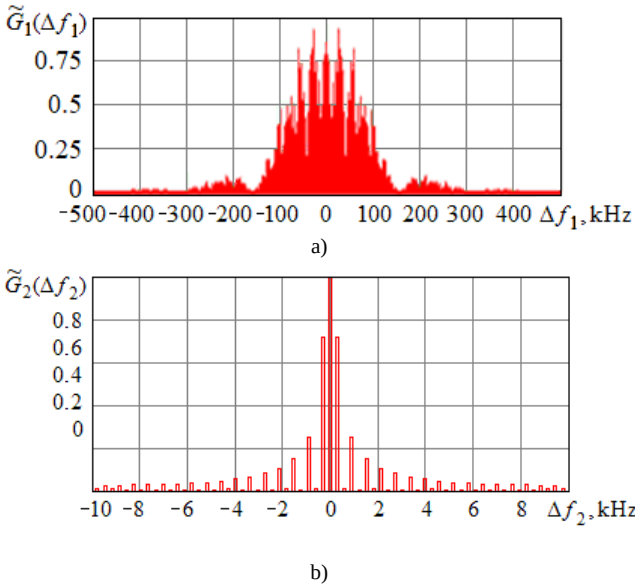

Fig. 15. The normalized spectrums of the binary PSK signal at the input of the detector (a) and at the output of the frequency multiplier (b).

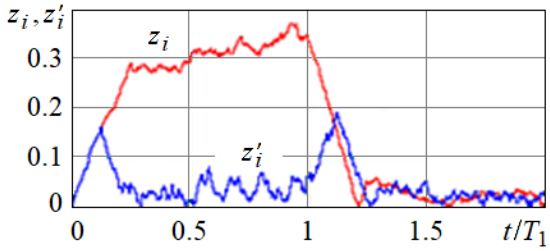

Fig. 16. The results of statistical simulation of the responses of the signal extraction and noise level estimation detector channels when receiving the binary PSK signal.

V. Digital Frequency Shift Keyed Signal Demodulator

The block diagram of the digital frequency shift keyed (FSK) signal demodulator [10] is demonstrated in Fig. 19.

As it can be seen, it is designed by means of two amplitude demodulators presented in Fig. 14 with the different sampling frequencies f_{S1} and f_{S2} such that

$$\begin{cases} f_{S1} = 4 f_{01}, \\ f_{S2} = 4 f_{02}. \end{cases}$$

Here f_{01} and f_{02} are the frequencies of the elements of the FSK signal while its mean frequency is

$$f_0 = (f_{01} + f_{02})/2.$$

The carrier frequencies of the signal elements can be presented as

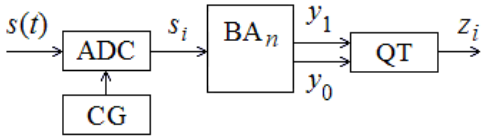

Fig. 17. The block diagram of the ASK signal demodulator.

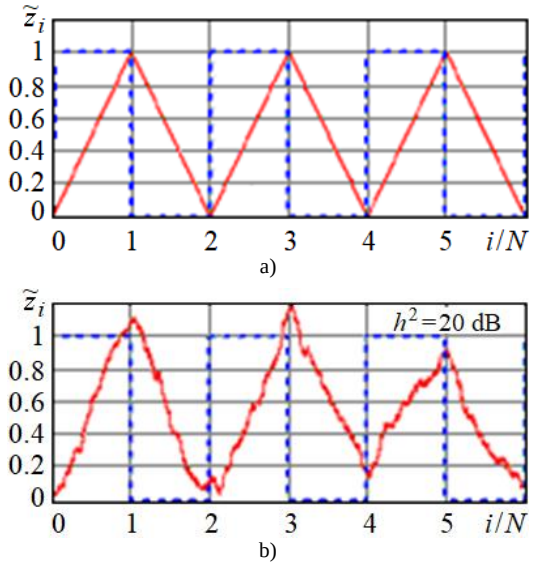

Fig. 18. The normalized responses of the ASK signal demodulator in the absence (a) and presence (b) of noise.

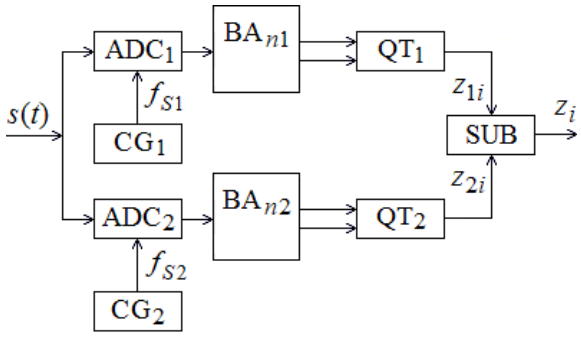

Fig. 19. The block diagram of the FSK signal demodulator.

$$\begin{cases} f_{01} = f_0 - F, \\ f_{02} = f_0 + F, \end{cases}$$

where $F = (f_{02} - f_{01})/2$.

The responses z_{1i} and z_{2i} are fed to the subtractor (SUB) and the resulting difference

$$z_i = z_{2i} - z_{1i}$$

is the output signal (decision statistics) of the demodulator.

The normalized AFC of the demodulator taking into account (6) is determined by the expression

$$H(f) = \frac{z}{S} = \left|\frac{\sin(N\pi f / f_{02})}{\cos(\pi f / 2 f_{02})}\right| - \left|\frac{\sin(N\pi f / f_{01})}{\cos(\pi f / 2 f_{01})}\right|. \quad (16)$$

In Fig. 20, the dependence (16) is shown on the frequency, if $N = 256$, $f_0 = 10$ MHz and

$$F = f_0 / 2N. \quad (17)$$

In Fig. 21, the time diagram $\tilde{z}(t) = z(t)/z_{\max}$ is drawn of the normalized response of the binary FSK signal demodulator as a function of the continuous (for the convenience) normalized time t/T_I when the duration of the information element is $T_I = NT_0$ and the relation (17) holds. By the dashed line the information symbols ± 1 are shown and by the points the decision times are marked.

When the FSK signal is received against Gaussian white noise, the probability of the demodulation error p_e is equal to [10]

$$p_e = \exp(-h^2/2)/2. \quad (18)$$

According to [3], this expression corresponds to the probability of error in the case when one deals with the optimal noncoherent reception of the orthogonal signals in the channel with an indefinite phase. Thus, the considered FSK signal demodulator is optimal and provides potential noise immunity in Gaussian noises.

VI. Digital Differential Phase Shift Keyed Signal Demodulator

When using the binary differential phase shift keying the information symbol is determined by the phase shift 0 or π between the received and previous elements. The block diagram of the differential PSK demodulator [11] is shown in Fig. 22.

The basic BA_n algorithm generates the quadrature response values y_{0i} and y_{1i} for the last received ith period. These values are stored in the multi-bit shifters $MR_{0(n+1)}$ and $MR_{1(n+1)}$ their size being $N = 2^n - 1$ cells. In the summators $SUM_{0(n+1)}$ and $SUM_{1(n+1)}$, there are calculated the sums of $u_{00i} = y_{0i} + y_{0(i-N)}$ and $u_{10i} = y_{1i} + y_{1(i-N)}$ while in the subtractors $SUB_{0(n+1)}$ and $SUB_{1(n+1)}$ – the differences $u_{01i} = y_{0i} - y_{0(i-N)}$ and $u_{11i} = y_{1i} - y_{1(i-N)}$, respectively. Based on these values, in the quadratic blocks QT_0 and QT_1 the samples

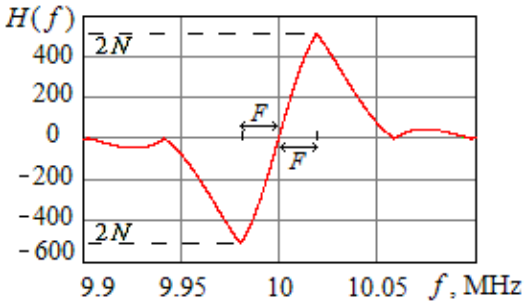

Fig. 20. The normalized amplitude-frequency characteristic of the FSK signal demodulator.

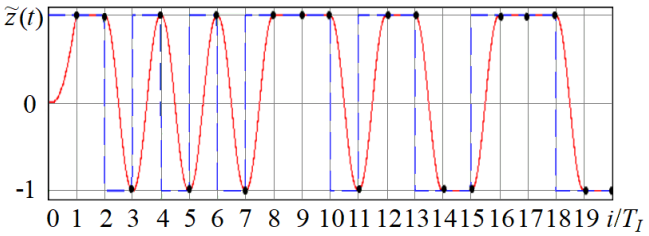

Fig. 21. The time diagram of the normalized response of the FSK signal demodulator.

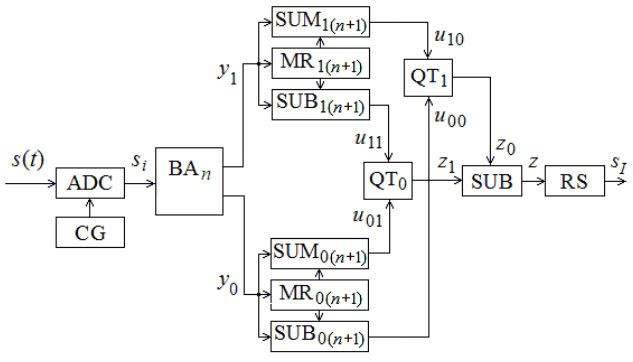

Fig. 22. The block diagram of the differential PSK demodulator.

$$\begin{cases} z_{0i} = \sqrt{u_{00i}^2 + u_{10i}^2}, \\ z_{1i} = \sqrt{u_{01i}^2 + u_{11i}^2} \end{cases} \quad (19)$$

are generated. They are moved to the subtractor, where the decision statistics

$$z_i = z_{0i} - z_{1i} \quad (20)$$

is determined.

By the sign of z_i (20), in the resolver RS the information symbol is determined at the end of the received element. In the absence of noises, if the phases of the neighboring elements coincide, then, at the decision time, the values (19) are $z_{0i} = 4NS$ and $z_{1i} = 0$, and vice versa, if the neighboring elements are antiphased, then $z_{0i} = 0$ and $z_{1i} = 4NS$.

In [11], it is shown that the probability of erroneous noncoherent demodulation of the differential PSK signals is determined in the following way:

$$p_e = \exp\left(-h^2\right)/2. \quad (21)$$

This dependence is shown by solid line in Fig. 23. Also here there are, by dots, the corresponding experimental values are drawn of the demodulation error probability obtained by means of statistical simulation. For comparison, the values of the error probability under coherent PSK signal demodulation calculated by the formula [3]

$$p_e = 1 - \Phi\left(\sqrt{2}h\right) \quad (22)$$

are presented by a dashed line. In (22), $\Phi(x) = \int_{-\infty}^{x} \exp\left(-z^2/2\right) dz / \sqrt{2\pi}$ is the probability integral.

The expression (21) coincides with one for the potential noise immunity of noncoherent PSK signal reception in Gaussian noises [3]. Thus, the introduced demodulator is optimal.

Noise immunity of the communication system can be significantly improved by applying the second-order binary differential PSK signals [12]. In this case, the received information signal is determined by the phase shift (0 or π) between the phase shifts (0 or π) of the neighboring pairs of the signal elements (E), as it is shown in Fig. 24. The block diagram of the demodulator of such the signals is shown in Fig. 25.

The results (4) of the signal sample processing in the basic algorithm are passed to the sample processing units SPU_0 and SPU_1 where they are stored in the two cascaded multi-bit shifters of N samples each by the capacity. Then for the last three received elements in SPU_0 there are formed the values

$$\begin{aligned} v_{000i} &= y_{0i} + y_{0(i-N)} + y_{0(i-2N)}, \\ v_{001i} &= y_{0i} + y_{0(i-N)} - y_{0(i-2N)}, \\ v_{010i} &= y_{0i} - y_{0(i-N)} + y_{0(i-2N)}, \\ v_{011i} &= y_{0i} - y_{0(i-N)} - y_{0(i-2N)}, \end{aligned} \quad (23)$$

while in SPU_1 –

$$\begin{aligned} v_{100i} &= y_{1i} + y_{1(i-N)} + y_{1(i-2N)}, \\ v_{101i} &= y_{1i} + y_{1(i-N)} - y_{1(i-2N)}, \\ v_{110i} &= y_{1i} - y_{1(i-N)} + y_{1(i-2N)}, \\ v_{111i} &= y_{1i} - y_{1(i-N)} - y_{1(i-2N)}, \end{aligned} \quad (24)$$

respectively.

Using (23), (24), in the decision-making unit (DMU) the quadrature transformations are implemented in the following way:

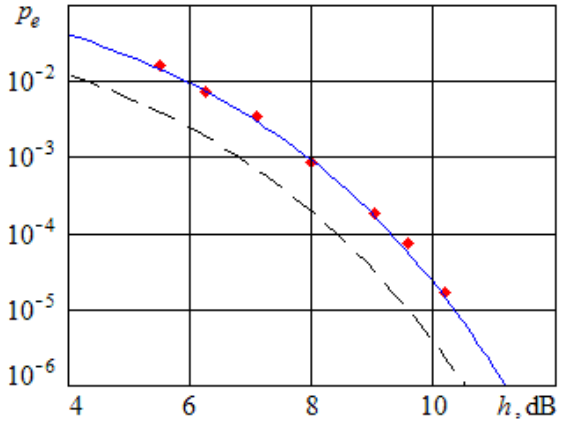

Fig. 23. The normalized amplitude-frequency characteristic of the FSK signal demodulator.

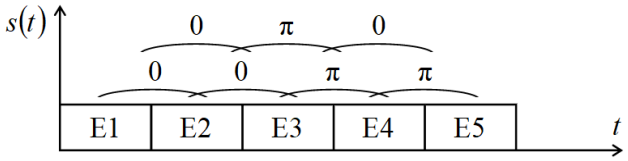

Fig. 24. The second-order binary differential PSK coding.

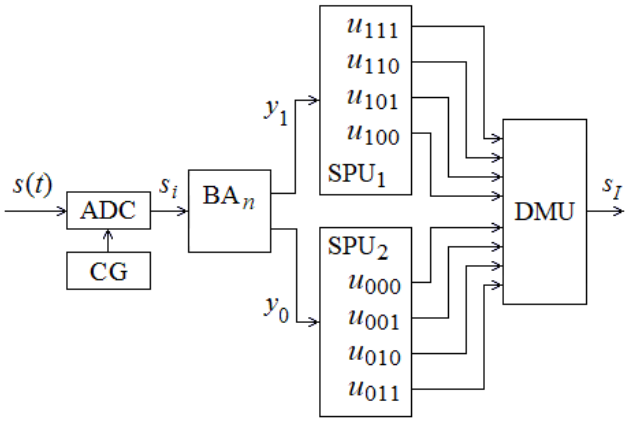

Fig. 25. The block diagram of the second-order binary differential PSK signal demodulator.

$$V_{0i} = \sqrt{v_{100i}^2 + v_{000i}^2}\,, \qquad V_{2i} = \sqrt{v_{110i}^2 + v_{010i}^2}\,, \tag{25}$$

$$V_{1i} = \sqrt{v_{101i}^2 + v_{001i}^2}\,, \qquad V_{3i} = \sqrt{v_{111i}^2 + v_{011i}^2} \tag{26}$$

and the highest values from both (25) and (26) are chosen:

$$A_i = \max(V_{0i}, V_{2i}), \qquad B_i = \max(V_{1i}, V_{3i}).$$

In [1], [2], [12], the estimates are obtained of the probability of the signal demodulation error against Gaussian white noise. In particular, in the case of noncoherent orthogonal signal reception, the probability of error is determined by the formula (18), in the case of noncoherent differential PSK signal reception – by the formula (21), in the case of coherent PSK signal reception – by the formula (22), in the case of coherent differential PSK signal reception – by the formula

$$p_e = 1 - \frac{1}{2}\left[1 + \left(\sqrt{\frac{2}{\pi}}\int_0^{\sqrt{2}h} \exp\left(-\frac{u^2}{2}\right) du\right)^2\right]. \tag{27}$$

In Fig. 26, there are shown the dependences of the specified estimates (18), (21), (22), (27) upon the SNR (10). Curve 1 corresponds to the probability of the demodulation error for the noncoherent orthogonal signal reception (18), curve 2 – for the noncoherent differential PSK signal reception (21), curve 3 – for the coherent differential PSK signal reception (27). The dashed line demonstrates the noise immunity of the coherent PSK signal reception described by the formula (22). By the crosses, the results are drawn of the statistical simulation of the digital demodulator of the second-order differential PSK signals against Gaussian white noise.

From Fig. 26, it follows that the noise immunity of the introduced second-order differential PSK signal demodulator almost coincides with the potential noise immunity of the coherent differential PSK signal demodulation, as stated in [12]. The gain in SNR compared to the noncoherent orthogonal signal demodulation and the ordinary differential PSK signal demodulation is approximately 3 and 0.5 dB, respectively, while retaining both the communications rate and the spectral characteristics.

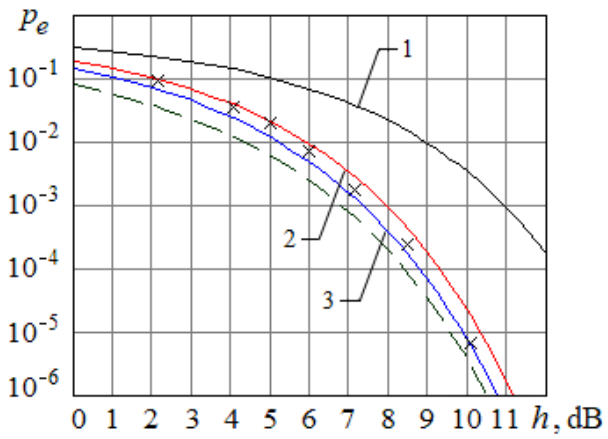

Fig. 26. The probability of the signal demodulation error.

VII. Digital Demodulator of the Signals That Are Phase-Shift Keyed in Toto

Based on the introduced basic algorithm of noncoherent processing of the radio signal, the demodulation of the signals that are phase-shift keyed in toto [3] can be implemented [13], [14]. The block diagram of such the demodulator, for the case when the signals are coded by Walsh sequences [15] with the length of binary symbols $M = 4$, is presented in Fig. 27.

The responses y_{0i} and y_{1i} of the quadrature channels of the basic algorithm (Fig. 3) are moved to the channel response shapers (CRSs) CRS_0 and CRS_1, their block diagrams are shown in Fig. 28. In these channels, the sums and differences of adjacent pairs y_{0i}, $y_{0(i-N)}$ and y_{1i}, $y_{1(i-N)}$ are calculated, and then the sums and the differences of these pairs separated by $2N$ periods are generated. The responses u_{0xxi} and u_{1xxi}, where symbols xx are equal to

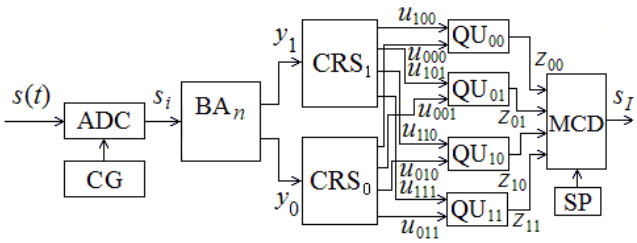

Fig. 27. The block diagram of the demodulator of the signals phase-shift keyed in toto and coded by Walsh sequences with the length of binary symbols $M = 4$.

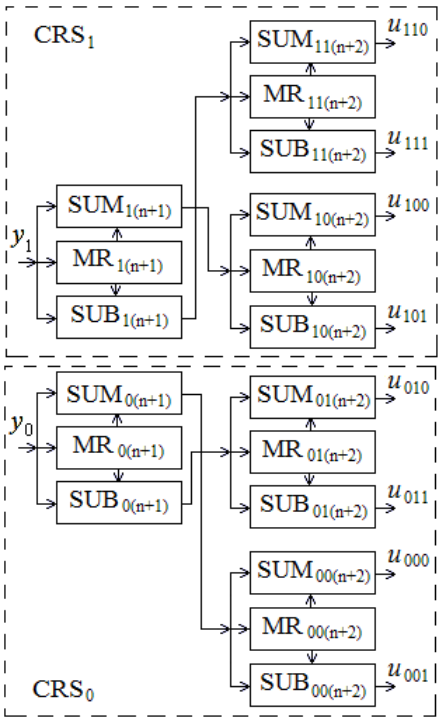

Fig. 28. The block diagram of the channel response shapers.

00, 10, 01 and 11, are presented in the Table I.

With the help of the values of u_{0xxi} and u_{1xxi} that are generated at the CRSs outputs in the quadratic units (QUs), the demodulator responses $z_{xx} = \sqrt{u_{0xxi}^2 + u_{1xxi}^2}$ to the corresponding Walsh codes are formed at the time of arrival of the framing clock pulses. And, depending on the greatest value the response z_{xx} takes, the decision on the received code combination is made by the maximum choice device (MCD). Thus, the estimated information symbol s_I is formed at the demodulator output at the time driven by the synchronizing pulse SP.

The calculation of the noise immunity of the demodulator of the binary signals that are phase-shift keyed in toto has been carried out in [13]. According to [13], the probability of erroneous reception of the code combination is

$$p_e = \sum_{k=1}^{M-1} \binom{M-1}{k} \frac{(-1)^{k-1}}{k+1} \exp\left(-\frac{Mkh_2^2}{k+1}\right) \qquad (28)$$

or approximately

$$p_e \approx (M-1)\exp\left(-Mh_2^2/4\right)/2\,, \qquad (29)$$

where h_2^2 is the SNR for the binary element and it is the same as in (10). For the demodulator presented in Fig. 27, in (28), (29), it should be taken that $M = 4$.

In Fig. 29, the dependences of the probability p_e (28) upon SNR h_2 determined according to (10) are shown by solid lines. By dotted lines, the similar dependences are drawn for the case of coherent signal processing when $M = 8$ (red dots) and $M = 16$ (blue dots). As it can be seen, the noncoherent reception of the signals that are phase-shift keyed in toto provides high noise immunity and loses less than 0.5 dB in comparison with the coherent reception.

It should be noted that, with the help of the considered basic algorithm for the noncoherent radio signal processing, the demodulator of four-position differential phase shift keyed signals [16] as well as the digital device for phase locking of the PSK signal demodulators [17] can also be

TABLE I
THE PROCEDURES TO FORM THE QUADRATURE CHANNELS RESPONSES

Walsh code	Channel response y_0	Channel response y_1
1 1 1 1	$u_{000i} = (y_{0i} + y_{0(i-N)}) + (y_{0(i-2N)} + y_{0(i-3N)})$	$u_{100i} = (y_{1i} + y_{1(i-N)}) + (y_{1(i-2N)} + y_{1(i-3N)})$
1 –1 1 –1	$u_{010i} = (y_{0i} - y_{0(i-N)}) + (y_{0(i-2N)} - y_{0(i-3N)})$	$u_{110i} = (y_{1i} - y_{1(i-N)}) + (y_{1(i-2N)} - y_{1(i-3N)})$
1 1 –1 –1	$u_{001i} = (y_{0i} + y_{0(i-N)}) - (y_{0(i-2N)} + y_{0(i-3N)})$	$u_{101i} = (y_{1i} + y_{1(i-N)}) - (y_{1(i-2N)} + y_{1(i-3N)})$
1 –1 –1 1	$u_{011i} = (y_{0i} - y_{0(i-N)}) - (y_{0(i-2N)} - y_{0(i-3N)})$	$u_{111i} = (y_{1i} - y_{1(i-N)}) - (y_{1(i-2N)} - y_{1(i-3N)})$

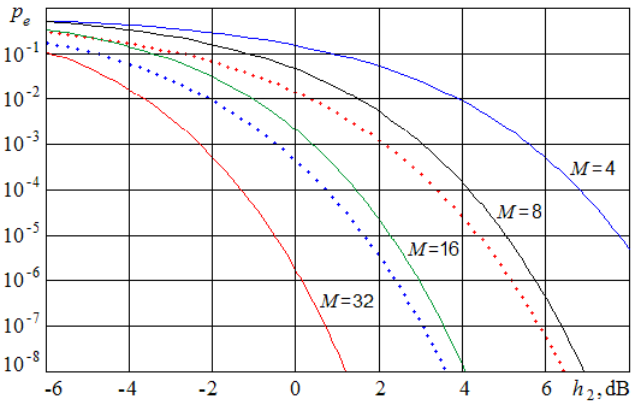

Fig. 29. The error probability when receiving the signals phase-shift keyed in toto and coded by Walsh sequences.

designed. The similar methods of accumulating signal samples are used in the design of digital measuring equipment as it is demonstrated in [18], for example. Thus, the introduced basic algorithm is a universal basis for designing various digital signal processing devices. The possibilities and the efficiency of the hardware implementation of the proposed devices by means of field-programmable gate arrays (FPGAs) are studied in [19], [20].

VIII. Conclusion

A unified approach to the development of the devices for digital radio signal processing is described based on the basic algorithm that is their major and most resource-intensive component. It is shown that this algorithm requires the minimum possible number of simple arithmetic operations for implementation.

It is demonstrated that the use of the presented approach makes it possible to design high-speed digital detectors of narrow-band and PSK signals including those that estimate the noise level and form the decision threshold adaptively. There are proposed the digital detectors and demodulators of ASK, FSK and differential PSK signals as well as the signals that are phase-shift keyed in toto. It is shown that the introduced devices have good frequency selective properties and provide potential immunity to Gaussian noises with independent samples. The greater possibilities for designing other digital signal processing devices are highlighted.

The hardware implementation of the devices specified above can be effectively implemented by means of FPGAs [21].

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