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Load-modulation technique without using quarter-wavelength transmission line

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Abstract: A proposed method for achieving active load-modulation technique without using a quarter-wavelength transmission line is discussed and evaluated. The theoretical analysis shows that the active load-modulation can be achieved without using a quarter-wavelength line, where the main amplifier sees a low impedance when the input signal level is low, and this impedance increases in proportion to the amount of current contributed from the peaking amplifier. The peaking amplifier sees an impedance decreasing from infinity to the normalized impedance. To validate the method, a circuit was designed, simulated and fabricated using two symmetrical gallium nitride (GaN) transistors (6 W) to achieve a peak power of 12 W and 6 dB output back-off efficiency. The design operates with 400 MHz bandwidth at 3.6 GHz and showed an average efficiency of 50% at 6 dB back-off and an efficiency of 75% at peak power. The designed circuit was tested with CW and modulated signals, the amplifier showed an Adjacent Channel Power Ratio (ACPR) of 31–35.5 dB when tested with a wideband code division multiple access signal of 6 dB peak-average-power ratio (PAPR) at 35.5 dBm average power. Additional 20 dB of linearity improvement was achieved after adding a linearisers.

1 Introduction

Complex modulation schemes are increasingly used in modern communication systems to increase high-speed data rates. As these schemes depend mainly on employing both amplitude and phase modulations, the generated signal will have an envelope with a high peak-to-average power ratio (PAPR), and as a result, the linearity required of the power amplifiers should be very stringent. On the other hand, high-power amplifiers are ideally designed to work in the saturation region to save energy, and the linearity in this region is very low. Consequently, the operating region of the power amplifier needs to be backed-off into a region that keeps the required linearity; however, the achieved average efficiency will be very low. Hence, the linearity and the efficiency of the power amplifier have become very challenging requirements in current and future communication systems. Several techniques are used to improve the efficiency of the power amplifier at the back off regions; among these are linear amplification using non-linear components, envelope tracking, envelope elimination and restoration, Chireix out-phasing and the Doherty power amplifier [1–4]. However, the Doherty technique is the simplest, where neither signal processing nor additional control circuits are required.

Doherty technique was first introduced in 1936 [5], and its main concept relies on the active load-modulation concept [6], where the apparent load impedance is modified by the effect of a current supplied from another source. There are at least two power amplifiers: the main amplifier, which that is operating all the time; and the peaking amplifier(s), which are working only at a high input power level as an additional current source(s). Many papers discuss the operation of the Doherty amplifier in detail [7–10]. In a classic Doherty amplifier, there are two peak efficiency points; the first peak is mainly dependent on the efficiency of the main amplifier because the peaking amplifier is off (in an ideal case), whereas the second peak efficiency is obtained when the two amplifiers are working at their full saturated power. Although there is a lower gain obtained from the Doherty amplifier compared to the single-ended form, the Doherty amplifier gain is nearly constant.

Moreover, the biasing of the main and peaking amplifiers depends mainly on the method of feeding the input signal to both amplifiers. If the amplifiers are fed independently (digitally controlled), both amplifiers can be biased as class AB; however, there will be a need to duplicate the radio frequency chains. Another solution is to use one input signal, then divide it between the two amplifiers, in which case the main amplifier will be biased as class AB whereas the peaking amplifier will be biased as class C. Nevertheless, class C [11] amplifier suffers from a low gain compared to class AB. To compensate for the gain difference between the two amplifiers, an unequal power splitter can be used.

Besides, there are some studies on replacing the quarter-wavelength lines with different architectures [12–15]. In [12], a coupled line was used as an all-pass section for achieving the load modulation and compensating the phase difference between the two amplifiers, whereas in [13], a lumped-element balun network was used for combining the output power and achieving the load modulation. In [14], a harmonic injection network allowed the second harmonic to be injected between the two amplifiers, which means the output power and the efficiency can be improved; however, there was a bandwidth limitation due to mismatch at the fundamental frequency [14]. An additional quarter wavelength was added to the peaking amplifier output matching network for compensating the carrier load reactance in [15].

The main advantage of the Doherty power amplifier is the circuit simplicity, whereas its well-known disadvantage is the limitation of the bandwidth due to the impedance inverter [16]; much research has been pursued to improve the achievable bandwidth [17–24]. Improving the bandwidth of the Doherty amplifier involved analysing the impedance transformer in detail [17], absorbing the parasitic effects of the Doherty amplifier [18, 19], or introducing a new post-matching network that can enhance the performance [25].

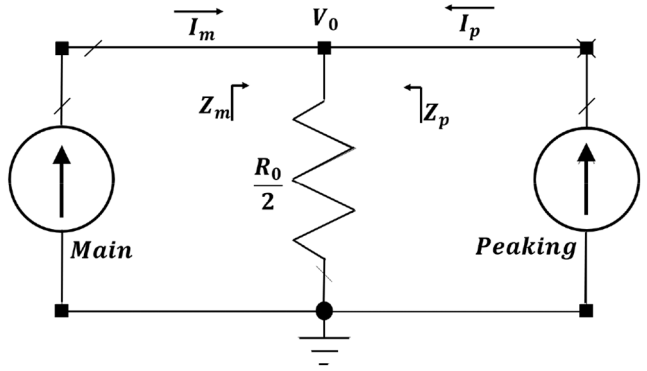

Fig. 1 *Suggested method operational diagram with equivalent amplifiers represented by current sources*

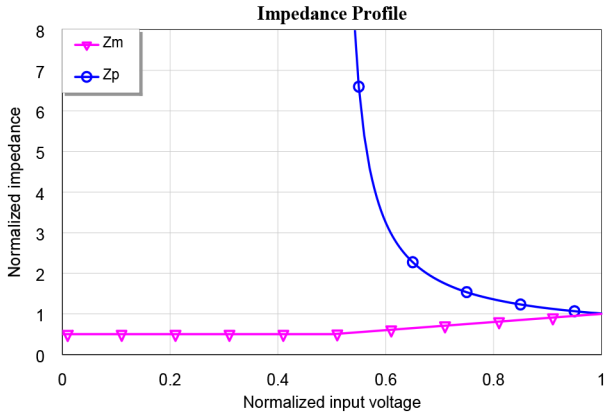

Fig. 2 *Impedance profiles for both amplifiers*

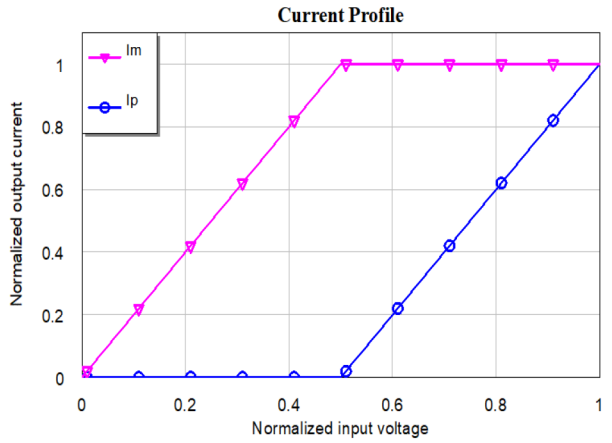

Fig. 3 *Main and peaking current profiles*

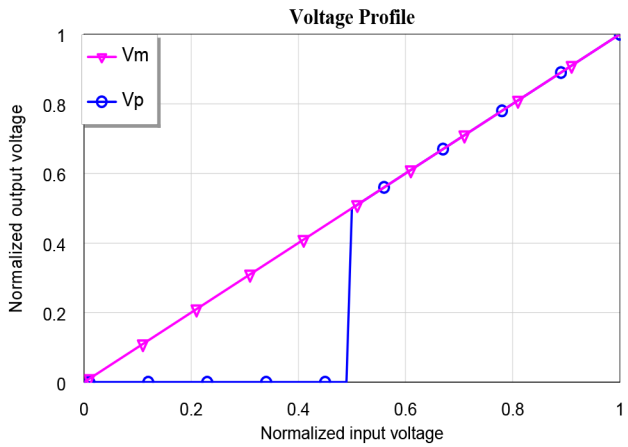

Fig. 4 *Main and peaking voltage profiles*

In this paper, a design methodology for a load-modulation technique without a quarter-wavelength transmission line will first be proved mathematically. This will be followed by a practical implementation, including all required assumptions and measurements, and finally conclusions will be drawn.

2 Proof of concept

The suggested method supposes that two power amplifiers (two current generators) are connected to each other into a load without a quarter-wavelength line as shown in Fig. 1.

The output load has an impedance of $R_0/2$, and is connected directly to both amplifiers, where both are matched at the peak power into R_0. At low input power, the peaking amplifier can be represented as an open circuit so that the main amplifier will see $R_0/2$ as load, and the impedance seen by the main amplifier will be varied according to the current amount of the peaking amplifier as shown in the following equations:

$$Z_{\mathrm{m}} = \frac{V_0}{I_{\mathrm{m}}} = \frac{(R_0/2)[I_{\mathrm{m}} + I_{\mathrm{p}}]}{I_{\mathrm{m}}} \tag{1}$$

where Z_{m} is the impedance seen by the main amplifier, V_0 is the voltage across the load, I_{m} is the main amplifier current, I_{p} is the peaking amplifier current and R_0 is the optimum matched impedance.

The current ratio between both amplifiers can be represented by the following equation:

$$\alpha = \frac{I_{\mathrm{p}}}{I_{\mathrm{m}}} \tag{2}$$

where α is the peaking to main current ratio.

By substituting (2) into (1), the impedance seen by the main amplifier will be

$$Z_{\mathrm{m}} = \frac{R_0}{2}(1 + \alpha) \tag{3}$$

The value of α varies from 0 to 1 assuming that the maximum peaking amplifier current is equal to the maximum main amplifier current. It can be noticed that impedance seen by the main amplifier is varying from $R_0/2$ to R_0. On the other hand, at the next phase of operation, when the peaking amplifier turns on, the peaking amplifier will act as an additional current source, where the impedance seen by the peaking amplifier will be varying from ∞ to R_0 according to the following equation:

$$Z_{\mathrm{p}} = \frac{V_0}{I_{\mathrm{p}}} = \frac{(R_0/2)[I_{\mathrm{m}} + I_{\mathrm{p}}]}{I_{\mathrm{p}}} \tag{4}$$

By substituting (2) into (4) the impedance seen by the peaking amplifier will be

$$Z_{\mathrm{p}} = \frac{R_0}{2}\left(1 + \frac{1}{\alpha}\right) \tag{5}$$

The load modulation of the suggested design is shown in Fig. 2, where it is clear that the impedance seen by the main amplifier is increased as the peaking amplifier current increases whereas the impedance seen by the peaking amplifier is changing from infinity to R_0, assuming a linear relation between the input voltage and output current of the transistors.

According to the suggested load modulation method, the current and voltage profiles of both amplifiers are shown in Figs. 3 and 4, respectively. The maximum currents of both amplifiers are assumed to be equal. However, the peaking amplifier starts injecting current at the mid-point, and in this case the transconductance of the peaking amplifier is assumed to be twice that of the main amplifier so that both amplifiers can reach the same peak current at the peak input voltage; nevertheless, only half of the peaking amplifier capability will be utilised. A solution for

this is to use an unequal input splitter. It can be noticed from Fig. 3 that the main amplifier current is increasing up to its maximum at the back-off point, after which it is constant, whereas, at the back-off point, the peaking amplifier starts injecting current to the summing point till the peak input power where it produces its maximum current.

The main amplifier current profile can be represented by the following equation:

$$I_{\mathrm{m}} = \begin{cases} I_{\max}\dfrac{V_{\mathrm{in}}}{\dfrac{V_{\mathrm{in,max}}}{2}}, & 0 < V_{\mathrm{in}} < \dfrac{V_{\mathrm{in,max}}}{2} \\ I_{\max}, & \dfrac{V_{\mathrm{in,max}}}{2} < V_{\mathrm{in}} < V_{\mathrm{in,max}} \end{cases} \tag{6}$$

where $I_{\max}$ is the maximum current, V_{in} is the input voltage level and $V_{\mathrm{in,max}}$ is the maximum input voltage level.

Whereas the peaking current profile is represented by the following equation:

$$I_{\mathrm{p}} = \begin{cases} 0, & 0 < V_{\mathrm{in}} < \dfrac{V_{\mathrm{in,max}}}{2} \\ I_{\max}\left[\dfrac{V_{\mathrm{in}} - \dfrac{V_{\mathrm{in,max}}}{2}}{\dfrac{V_{\mathrm{in,max}}}{2}}\right], & \dfrac{V_{\mathrm{in,max}}}{2} < V_{\mathrm{in}} < V_{\mathrm{in,max}} \end{cases} \tag{7}$$

It can be seen from Fig. 4 that the voltage of the main amplifier is increasing as the input power level increases; on the other hand, the peaking amplifier voltage will be equal to the main amplifier voltage once the peaking amplifier starts injecting the current. The main and peaking voltage profiles can be calculated using the following equations depending on the impedance and current equations:

$$V_{\mathrm{m}} = V_{\max}\left[\frac{V_{\mathrm{in}}}{V_{\mathrm{in,max}}}\right], \quad 0 < V_{\mathrm{in}} < V_{\mathrm{in,max}} \tag{8}$$

$$V_{\mathrm{p}} = \begin{cases} 0 & 0 < V_{\mathrm{in}} < \dfrac{V_{\mathrm{in,max}}}{2} \\ V_{\max}\left[\dfrac{V_{\mathrm{in}}}{V_{\mathrm{in,max}}}\right], & \dfrac{V_{\mathrm{in,max}}}{2} < V_{\mathrm{in}} < V_{\mathrm{in,max}} \end{cases} \tag{9}$$

In addition, the impedance profile of the main amplifier can be represented by the following equation:

$$Z_{\mathrm{m}} = \begin{cases} \dfrac{V_{\max}}{2 * I_{\max}}, & 0 < V_{\mathrm{in}} < \dfrac{V_{\mathrm{in,max}}}{2} \\ \dfrac{V_{\max}}{I_{\max}}\left[\dfrac{V_{\mathrm{in}}}{V_{\mathrm{in,max}}}\right], & \dfrac{V_{\mathrm{in,max}}}{2} < V_{\mathrm{in}} < V_{\mathrm{in,max}} \end{cases} \tag{10}$$

whereas the impedance seen by the peaking amplifier can be represented by the following equation:

$$Z_{\mathrm{p}} = \begin{cases} \infty, & 0 < V_{\mathrm{in}} < \dfrac{V_{\mathrm{in,max}}}{2} \\ \dfrac{V_{\max}}{2 * I_{\max}}\left[\dfrac{V_{\mathrm{in}}}{V_{\mathrm{in}} - \dfrac{V_{\mathrm{in,max}}}{2}}\right], & \dfrac{V_{\mathrm{in,max}}}{2} < V_{\mathrm{in}} < V_{\mathrm{in,max}} \end{cases} \tag{11}$$

Equations (10) and (11) can be rewritten in terms of load impedance as illustrated in the next equations:

$$Z_{\mathrm{m}} = \begin{cases} \dfrac{R_0}{2}, & 0 < V_{\mathrm{in}} < \dfrac{V_{\mathrm{in,max}}}{2} \\ \dfrac{R_0}{2}(1+\alpha), & \dfrac{V_{\mathrm{in,max}}}{2} < V_{\mathrm{in}} < V_{\mathrm{in,max}} \end{cases} \tag{12}$$

$$Z_{\mathrm{p}} = \begin{cases} \infty, & 0 < V_{\mathrm{in}} < \dfrac{V_{\mathrm{in,max}}}{2} \\ \dfrac{R_0}{2}\left(1 + \dfrac{1}{\alpha}\right), & \dfrac{V_{\mathrm{in,max}}}{2} < V_{\mathrm{in}} < V_{\mathrm{in,max}} \end{cases} \tag{13}$$

where

$$\alpha = \frac{I_{\mathrm{p}}}{I_{\mathrm{m}}} = \frac{I_{\max}[(V_{\mathrm{in}} - (V_{\mathrm{in,max}}/2)/(V_{\mathrm{in,max}}/2))]}{I_{\max}} = \frac{V_{\mathrm{in}} - (V_{\mathrm{in,max}}/2)}{(V_{\mathrm{in,max}}/2)} \tag{14}$$

It should be clarified that the analysis above is suitable at low frequency; however, as the operating frequency increases, the effect of the transistor parasitic will dominate the transistor performance, where the parasitic effect is mainly depending on the transistor structure and manufacturing process. The transistor parasitic can be modelled as a complex network consists of inductors, capacitors and very small resistors; however, the drain–source capacitance (C_{ds}) can be assumed as the most effective parasitic component that dominates the amplifier performance especially at high-frequency bands in terms of transistor current phase, output power, efficiency, and even amplifier linearity. Several techniques are used for neutralising the C_{ds} such as adding a shunt inductor. However, the additional reactive component would result in an asymmetrical transistor frequency response. For a specific frequency band, the parasitic effects can also be compensated using the matching network and the line offsets.

Depending on the mathematical proof above, the load modulation can be implemented without using a quarter-wavelength transmission line. However, there are some assumptions and procedures that should be followed. All these issues will be discussed in the following section.

3 Design of load-modulation technique

The design of any power amplifier starts by defining the architecture that needs to be implemented for the given design requirements. The main difference between the main and peaking amplifiers in the load modulation technique is the biasing condition. In addition, there are some practical considerations in designing a load-modulation power amplifier without a quarter-wavelength section. These are the impedance seen from the summing point (S) towards the peaking amplifier as shown in Fig. 5 should be high to prevent any leakage current when the peaking amplifier is off. In addition, this impedance should not load and affect the impedance seen by the main amplifier at both the back-off and peaking region. An offset line can be used for maintaining this condition after designing the output matching network. Moreover, an offset line is used after the output matching network of the main amplifier to compensate for the parasitic effects of the amplifier due to the change of the impedance seen at the back-off. However, the implemented circuit has a minimum length of offset lines for practical circuit fabrication, in addition to the reasons mentioned above.

A 3.6 GHz GaN load-modulation amplifier was designed and simulated using microwave office (MWO) with 400 MHz bandwidth to achieve a peak power of 12 W and a back-off power of 6 dB. Fig. 5 shows the schematic circuit diagram for the load-modulation technique without a quarter wavelength. It can be observed that the designed circuit started with a Wilkinson power divider to split the input signal between the two amplifiers. This was followed by the design of the main and peaking amplifiers, including the stability circuits, the input matching networks, the output matching networks and the biasing circuits. The stability circuit prevents the designed amplifier from oscillating. Moreover, the input matching network is mostly responsible for controlling the gain of the amplifier whereas the output matching network is used to provide a trade-off between the output power and the achieved efficiency. At the same time, there are interactions between the input and output matching networks which should be considered. Each amplifier is matched to 50 Ω at the output side,

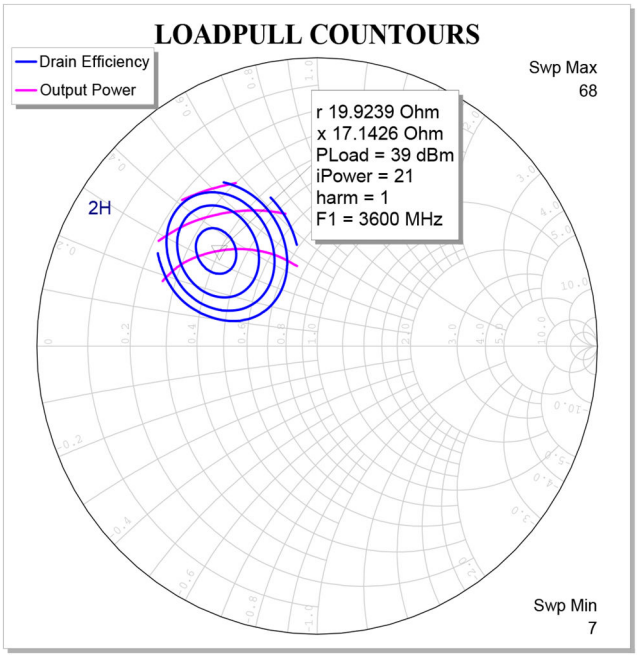

Fig. 5 *Amplifier output power and efficiency contours*

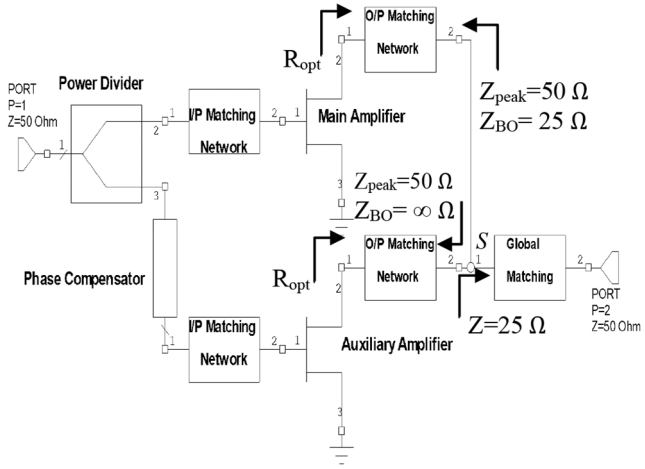

Fig. 6 *Schematic circuit diagram for load modulation technique without a quarter-wavelength section*

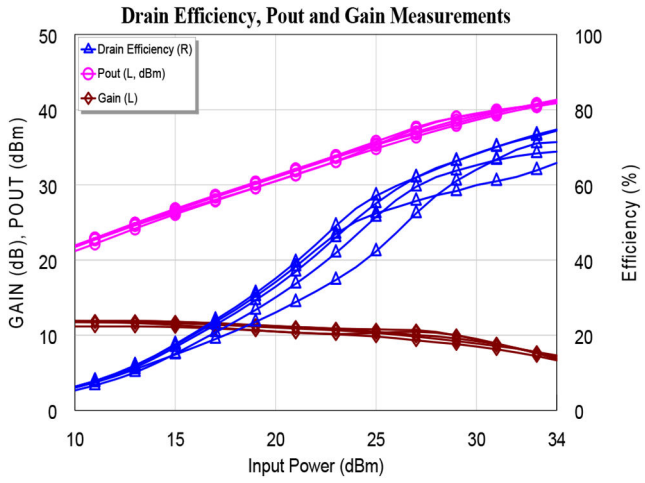

Fig. 7 *Simulated results of the designed amplifier*

where the amplifier would see the optimum impedance looking from the transistor side. In addition, the global matching network is used as a transformer for transferring the output port impedance (50 Ω) into the 25 Ω at the summing point. So that the main amplifier would see a 25 Ω at the back-off, where the load modulation would occur according to the theory that discussed in the last section where the impedance seen will be modulated and increased from 25 to 50 Ω for the main amplifier side. On the other side, the peaking amplifier is matched to 50 Ω at the peak power, at the same time, the output matching network is designed to produce a high impedance looking from the summing point towards the peaking amplifier when the peaking amplifier is off. In this case, the load impedance will be modulated according to the peaking contributed current as discussed previously.

To specify the impedances that the transistor needs to see at both input and output sides to achieve a certain amount of gain, output power and efficiency, load-pull data can be used as an indication as shown in Fig. 6, where the transistor needs to see, at the output side, $(20 + j17\,\Omega)$ for the fundamental frequency and about $(0 + j15\,\Omega)$ for the second harmonic matching in order to produce a 39 dBm peak power with 78% peak efficiency.

At the input side, the power amplifier has both a stability circuit and the input matching network that interact with each other to stabilise the amplifier in addition to determining the gain, input reflection etc. by adjusting the impedance seen from the gate side. All these steps were applied in the design procedure for both main and peaking amplifiers.

MWO was used to perform both linear and non-linear simulations, including electromagnetic simulation. Fig. 7 illustrates the simulated performance of the designed amplifier; there is an obvious peak efficiency averaging 50% at the back-off power and about 70% peak efficiency at the peak power for the designed frequency band. On the other hand, the simulated gain was 12 dB and the peak power is 41.5 dBm.

At the same time, waveform engineering techniques [2, 3] were used to utilise the devices most effectively by controlling the current and voltage waveforms. Fig. 8 illustrates the voltage and current waveforms at the current generator plane using the available voltage and current ports from the non-linear model. The results of Fig. 8 are obtained after designing the output matching network which makes the amplifier see the required impedances for the fundamental and harmonic frequencies depending on the load-pull data.

Figs. 9 and 10 show the prototype circuit layout of the designed amplifier using the MWO and the fabricated circuit, respectively, where both the main and peaking amplifiers have the same input matching network. However, the output matching networks of both amplifiers are different. Here the output matching network of the peaking amplifier was used to achieve the two purposes of providing the impedance that the transistor needs to see, in addition to providing a high impedance seen from the summing point towards the peaking amplifier at low input power levels.

In addition, six ports are provided in the prototype design which are used for testing the designed amplifiers individually or in combination. Ports 1 and 2 are used to test the complete load-modulation amplifier (the two amplifiers working together) whereas ports 3 and 4 are used for testing the main amplifier alone. Likewise, ports 5 and 6 are used for testing the peaking amplifier alone. At the same time, ports 1, 3 and 5 can be used for testing the operation of the Wilkinson divider. The dc blocking capacitors (C1–C4) at the input and output sides can be repositioned during testing for changing the signal paths as shown in Fig. 9.

Fig. 11 shows the practical measurement setup for the fabricated circuit. The circuit was tested in continuous wave (CW) signal mode for the designed frequency bands. Moreover, each amplifier was tested alone, where ports 3 and 4 are used to test the main amplifier which achieved a peak power of 38 dBm with peak efficiency of 70%, whereas the peaking amplifier was tested using ports 5 and 6. The achieved peak power for the peaking amplifier was also 38 dBm, with 62% peak efficiency. The reduction of the efficiency in the peaking amplifier is due to the difference of the designed output matching network.

Furthermore, with an input at port 1 and the output taken from port 2, the performance of the complete load-modulation amplifier was tested after changing the signal directions using the dc blocking capacitors. Fig. 12 shows the CW test for the load-modulation amplifier, where the amplifier was able to achieve a peak power of 41.5 dBm with an average efficiency of 73%. At the

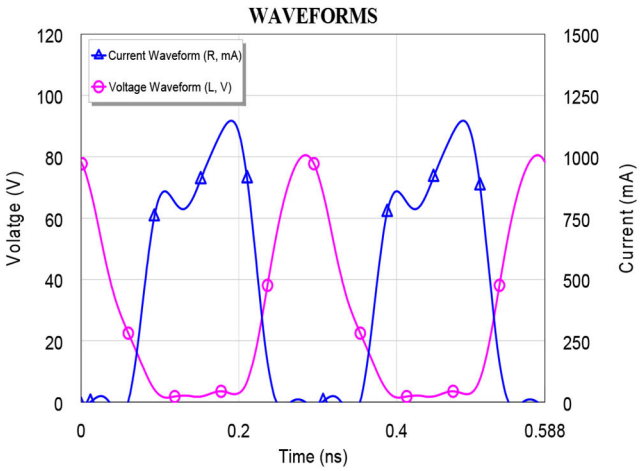

Fig. 8 *Simulated current and voltage waveforms*

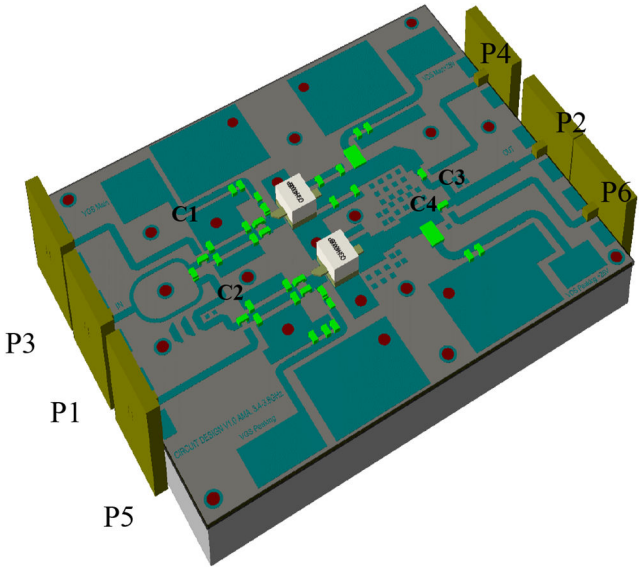

Fig. 9 *Prototype of the designed circuit using MWO*

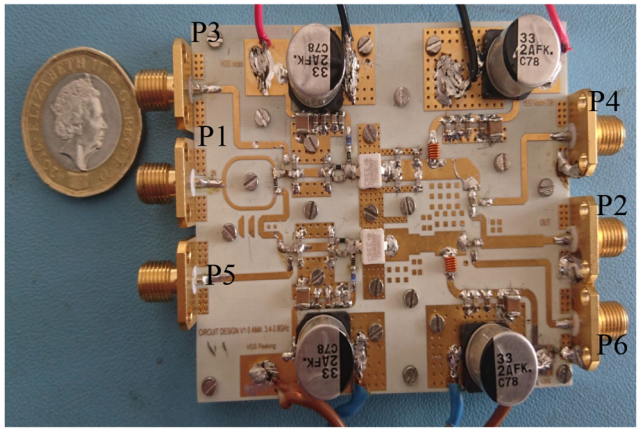

Fig. 10 *Fabricated prototype of load-modulation technique without a quarter wavelength*

same time, the amplifier was able to deliver an average efficiency of 50% at 6 dB back-off from the peak power. It should be noted that these results were achieved without any tunings. In addition, Fig. 13 shows the amplifier performance versus the design frequency band.

Moreover, the fabricated circuit was tested using a wideband code division multiple access (WCDMA) signal with 6 dB PAPR, when the amplifier is working at the back-off power of 35.5 dBm. Fig. 14 is a sample of the measured performance at 3.6 GHz. The amplifier was able to achieve 35.5−31 dB ACPR for the designed

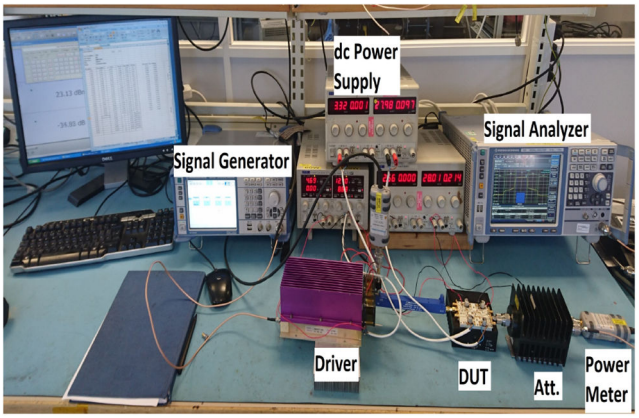

Fig. 11 *Practical measurements setup for the designed amplifier*

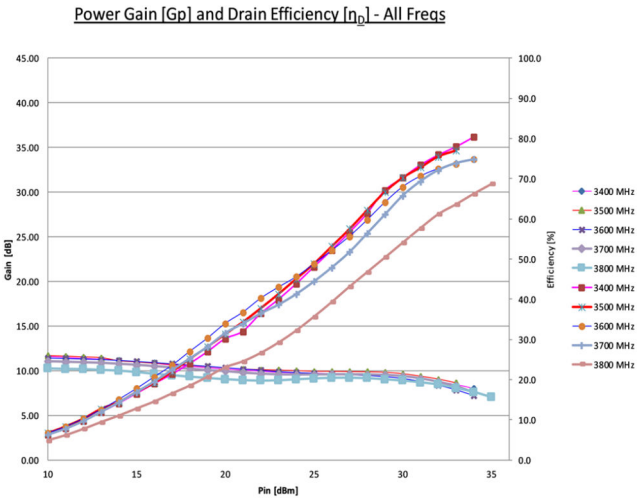

Fig. 12 *Practical large-signal measurements of the designed amplifier*

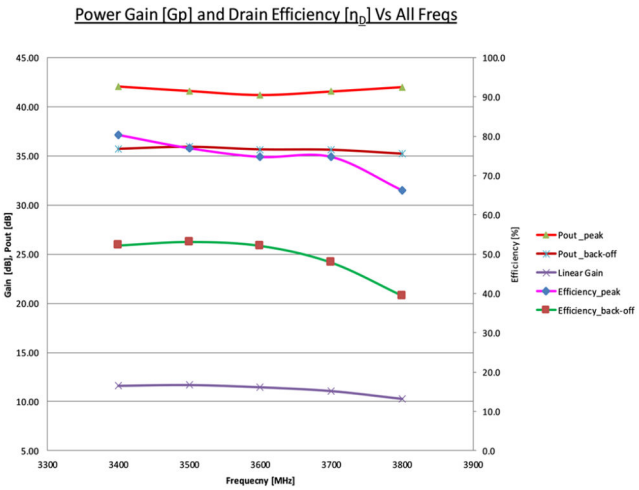

Fig. 13 *Practical large-signal measurements versus the designed frequency*

band without any lineariser. After that, a lineariser (Maxim integrated SC1894) has been added to improve the linearity of the designed amplifier, where about 20 dB improvement has been achieved for the ACPR performance as shown in Fig. 14.

Finally, Table 1 shows the performance summary of the state-of-the-art of load-modulation amplifiers within the same frequency band. It can be seen that the suggested technique can achieve higher linearity comparing to the performances in other work, with/without using digital pre-distortion (DPD).

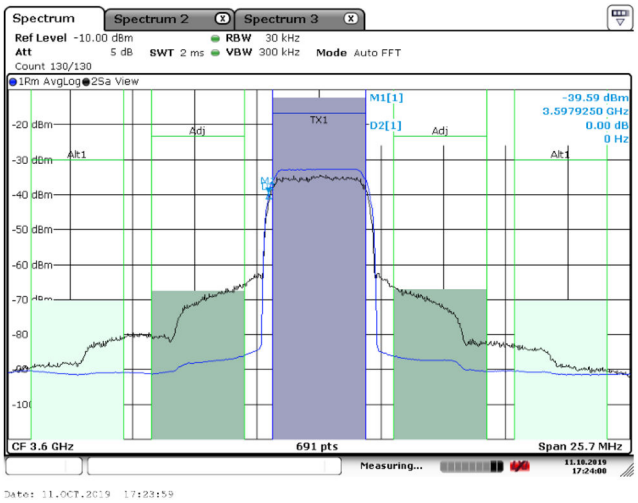

Fig. 14 *ACPR measurements at 3.6 GHz*

Table 1 Performance comparison of load-modulation amplifiers

REF	Frequency, GHz	P_{sat}, dBm	DE (%) @P_{sat}	P_{av} (dBm)	DE (%) @P_{av}	Gain, dB	BO, dB	Signal type	ACPR, dB	
									Without DPD	With DPD
[26]	3.4–3.8	44.5	48	36.5	40–42	25	8	LTE	−29	−50
[27]	3.3–3.6	44.3	64	36.3	52	28.5	8	LTE	NA	NA
[28]	3.3–3.6	49	55–70	41	41–55	14.7	8	LTE	−30	NA
[29]	3.3–3.55	47.5	53–60	40	47–58	12–15.5	7.5	LTE	−27.5	−46.7
[30]	3.3–3.5	48	50	40	48–52	11–12.5	8	WCDMA	−31.8	NA
this work	3.4–3.8	41.5	75	35.5	50	12	6	WCDMA	−33	−53

P_{sat}: amplifier output power at the saturation.

DE: drain efficiency.

P_{av}: amplifier average power (amplifier output power at the back-off).

4 Conclusions

The active load-modulation technique without a quarter-wavelength transmission line has first been verified mathematically and then practically using a fabricated prototype. The active load modulation is mainly depending on the contributed current from the peaking amplifier, whereby the impedance seen by the main and the peaking amplifier will be changed. In the case where the load modulation is achieved without a quarter-wavelength transmission line and with equal capabilities for both amplifiers, the impedance seen by the main amplifier will be increased from $R_0/2$ to R_0 depending on the peaking current whereas the impedance seen by the peaking amplifier will be changed from infinity (ideally) to R_0. The load modulation can be realised with/without a quarter-wavelength transmission line after considering all required assumptions; although the designed amplifier is narrowband, we can assume that the Doherty bandwidth limitation is not mainly restricted by the quarter-wavelength transmission line. The output matching network can be designed to provide a high impedance seen from the summing point towards the peaking amplifier and to transform 50 Ω into the optimum impedance that the transistor needs to see. Designing a load-modulation amplifier without a quarter wavelength can help in reducing the required area for the power amplifier in addition to realising a peak efficiency at the back-off. This technique can be used in mobile handsets when lumped elements are used instead of microstrip elements. Additional ports in the prototype design were useful in testing the amplifiers individually or when combined. The fabricated circuit was able to achieve a peak power of 41.5 dBm and an efficiency of 75%. At the same time, the designed amplifier achieved an average back-off efficiency of 50% at 6 dB output power back-off from the peak power. The amplifier was able to achieve 35.5−31 dB ACPR at 35.5 dBm average power when the amplifier is fed with a WCDMA signal of 6 dB PAPR. A 20 dB improvement on the ACPR was achieved after using the linearisers.

5 References

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