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Design and implementation of a series switching SPSI for PV cell to use in carrier based grid synchronous system

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ABSTRACT

A carrier-based grid synchronous method is proposed to develop the system efficiency, phase and power quality of the inverter output waves. The operating principle of a single-phase phase synchronous inverter (SPSI) is introduced, with proper synchronous paid to the switching-frequency synchronizing voltage made by the interleaved process, as well as actual mitigation approaches. In the construction of the SPSI, input and output filters are electrically coupled with the two sides of an inverter. The inverter power electronic switches and other electrical components are operated by carrier-based grid synchronous controller (CBGSC) with PWM regulator. The SPSI is designed and implemented with the Toshiba 40WR21 IGBT, Digital Microcontroller pulse controller (DMPC) and 4N35 Optocoupler with a fundamental frequency of 50Hz. The other parameters are considered as load resistance, R_L=11Ω, duty cycle, 85%, carrier frequency, 2.5kHz and input DC voltage, ± 340V. In addition, LCL lowpass grid filters are used to convert squire wave to sine wave with required phase and frequency. Finally, the simulated and experimental results obtained with a carrier-based grid synchronous SPSI experimental prototype are exposed for justification, showing the phase error of 55% improvement, reduced 11% of THD and the conversion efficiency of 97.02% highly predicted by the proposed design technique to improve the microgrid system.

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1. INTRODUCTION

SPSI active carrier-based pulse width modulation (PWM) DC to AC inverters is generally utilized as a means of improving efficiency and developing the power quality of the source current, as the characteristic a higher effective performance compared to their multi-carrier PWM based DC to AC inverter counterparts. In consequence, traditional carrier-based PWM inverters have become dominant in the grid synchronize system, a high-quality further maintained by their characteristic simplicity. Nevertheless, if superior performance is sought, carrier-based PWM inverters denote a better solution to operate lower switching frequency [1]. This type of control mechanism is gradually being implemented in these systems, a trend that is built easier by the current availability of combined power electronic semiconductor switching modules in different control DC to AC inverter configurations.

Single phase inverters can be operated in discrete, continuous and phasor power flow methods. Among discrete methods, one of the standard methods is the single-phase midpoint source voltage source inverter which uses discretization of the electrical power system for a solution at fixed time steps [2]. On the hand, the configuration of the solver depends on the option which is selected discrete mode to perform a discretization of the model and specify the sample time in the sample time parameter. A multi-carrier based

PWM phase terminal implementation with two switches the input DC source voltage and two devices in AC-switches arrangement half the input DC source voltage [3]. Continuous and phasor methods are used to perform a continuous and phase solution of the inverter, at the specified by the phasor frequency parameter. If the power inverter switching blocks utilizing ideal switches. This parameter can be visible only when the type of the parameter is set to continuous. By default, this selection is not designated, a large amount of switching ripple current is amplified in the output side that can be affected by the DC bus voltage. In this case, current ripple can be generated low frequency and degrade the power density and quality. For instance, ripple current is degrading the regulator in the solar system [4]; it will be reduced the power quality and lifetime of fuel cells in Gencell [5]; it may be boosted battery storage uninterrupted power systems. Conventionally, the solar power is an unlimited power source that is produced by a PV cell must convention instantaneously and required the bulky size of battery cells. It is a high cost and complexed maintaining issue. To overcome this problem, several cells of the PV modules are connected through common local networks knowing as the grid system [6]. These systems have some limitation. The main drawback is required to take steps to ignore the low-frequency current ripple flowing in the input DC supply, phase synchronization, high preliminary cost, and a large area. Therefore, carrier-based grid synchronous PSI using renewable power system is superior performance and economical.

To illustrate multifunction topology of the single-phase inverter low-frequency supply distorted current has been introduced in the earlier publications [7]. However, the grid filter circuit can be involved to decrease the low-frequency distorted current. For example, DC bus capacitance is improved in [8], and grid filter is injected to DC bus in [9]. Besides, it is more complexed to maximize the weight and size of the DC bus capacitor. An alternative realization of the latter is the S-PSI topology is included a suitable switching circuit and logic controller are diverted to added storage mechanism [10]: traditional buck-boost DC to DC converter is connected to DC bus and process as an input LC filter of active power in [11]; The discussion [12] carried out an exceptional low-frequency distorted compensator that can be sequenced with the novel inverter; A secondary phase terminal is involved in [13], and the total power from DC bus can retain constant by properly monitoring the existing of further phase terminal. Whereas these methods can be successfully overpowering the input frequency ripple current, the additional switches circuit may be led to an increase in cost, power losses and regulator effort.

A switching technique to further develop the system efficiency and increase a power inverter is to utilize series switches. In the latter case, unknown gate signals of the equivalent switches of each phase terminal are interleaved, both the inverter power quality and efficiency are improved [14]. Precisely, the higher harmonic frequency cancellation gain between the interleaved of the half phase terminals consents for the utilize of lower switching frequencies, whereas simultaneously falling the input power quality size and electromagnetic interference filters [15]. It is then expected that an interleaved n-channel Vienna-type rectifier [16] would feature even higher efficiency and power density than its single-channel embodiment. In search of a topology with an efficiency exceeding 99% that could eliminate the need for active cooling, this work adopted a two-channel interleaved Vienna-type rectifier. It is predictable than that a carrier base synchronous series switching DC to AC inverter depends on switching logic operation would feature even higher overall system performance and power quality than its conventional DC to AC inverter embodiment. In an exploration of a switching topology with a control, the approach is very complicated when since the electromechanical concert, and not appropriate for the power supply systems. Authors in [17] studied that single-phase inverter can be boosted along with incontrollable low-frequency ripple. In this case, the constant duty factor is assumed for the boost stage that is primarily an open-loop voltage regulator. The effect of DC ripple current reduction, fully depends on the DC bus capacitors; thus, filter components of the bus capacitance must comparatively large [18, 19].

This paper presents the design and implementation of a carrier-based grid synchronous controller, series switching S-PSI with proper grid synchronous less than lower phase angle. This is more essential to reduction ripple, reduce switching loss and higher efficiency. The inverter operation is maximized for phase voltage of 230V AC, 45-55 Hz of a fundamental frequency, line frequency around of 250Hz to 500 Hz, DC bus voltage ± 340V DC and 85% of duty factor. In addition, grid LCL filter is utilized to couple inverter, convert the signal and reduce the harmonic. This paper is systematized as follows: Section II shows the operating principles of the series switching S-PSI; Section III presents the model configuration and analysis; Section IV presents a design procedure of a switching gate controller; Section V presents grid couple lowpass LCL filter design; Section V presents the grid synchronous method; Section VI presents simulated result and discussion; Section VII presents the experimental results and discusses; and lastly, Section VIII introduces the conclusions drawn from this work.

2. OPERATION PRINCIPLES OF THE SERIES SWITCHING S-PSI

Figure 1 shows the switching topology of the series switching S-PSI configuration. In this system, upper switches (IGBT1, IGBT1a), lower switching (IGBT2, IGBT2a) and flywheel diode connected to the IGBT switch D_1 and D_2 from a half phase sub-inverter which can operate simultaneously. The remaining switching pairs upper switches IGBT3, IGBT3a, lower switching (IGBT4, IGBT4a) and their corresponding diodes D_3 and D_4 from a second-half sub-inverter. The inverter output phase legs are connected utilizing the grid LCL filter input side inductor of L_{inv_o} and output side inductor of L_{MG_o} is coupled to grid load as seen in Figure 1.

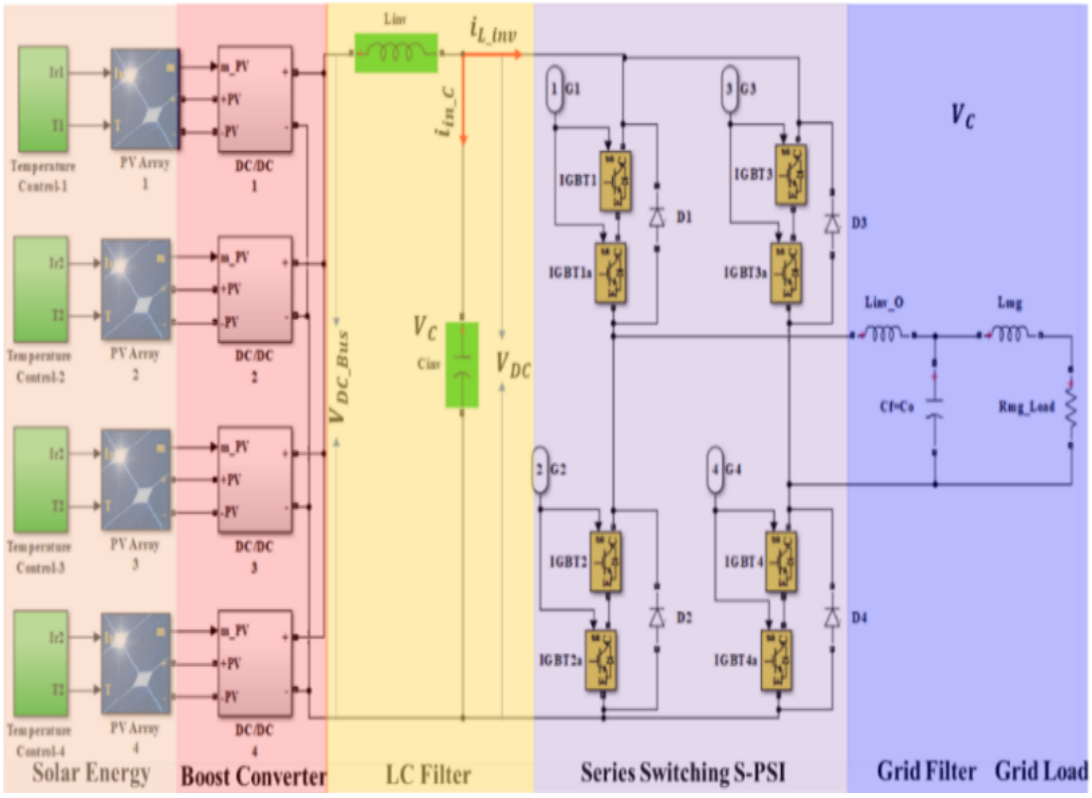
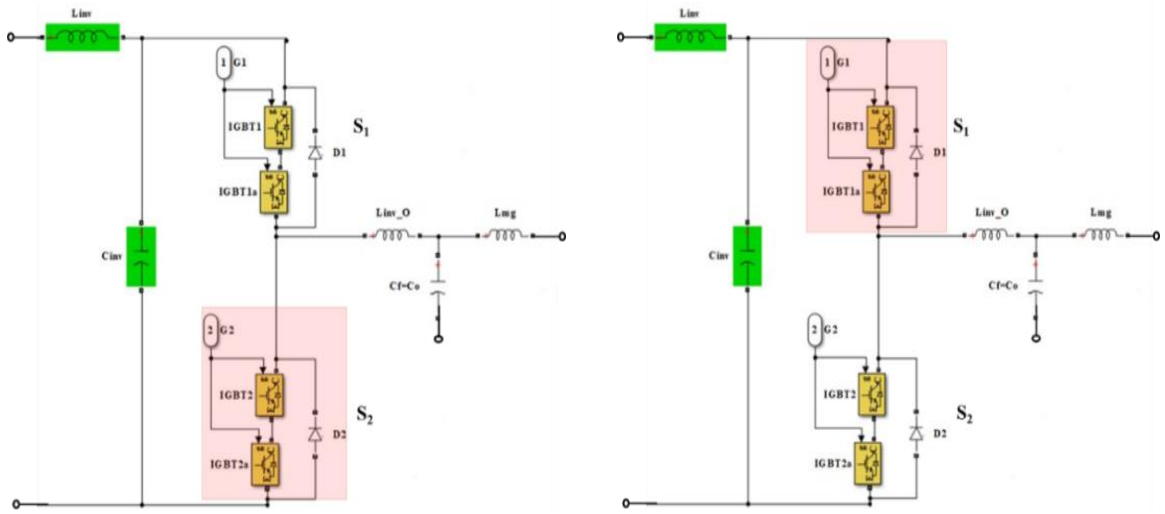


Figure 1. Proposed series switching SPSI circuit configuration [1]

The series switching S-PSI is a voltage source current-commutated inverter, which can be, the devices which commutate at any upper switching or lower switching instant are measured by the instantaneous direction of flow load current. If the load current flow in Figure 2 is positive, the computation will take place between upper switch of S_1, lower switch of S_4 and $D_1 - D_4$ whereas the lower switch of S_2 *and upper switch* S_3 are turned OFF. Therefore, the voltage potential at point of phase leg V_{ao} with reference to the center point of the input DC source will be either half of the DC bus voltage, when S_1-S_4 or S_3-S_2 are turned ON or OFF.



(a) (b)

Figure 2. MATLAB circuit for switching mechanism

3. MODEL CONFIGURATION AND ANALYSIS

To work the inverter in series switching method, a phase angle shift is offered between the carriers based PWM of the two-half phase inverter that compound it [20]. This working approach forces odd harmonic components to circulate between the consistent output terminal of the half phase inverter, which can be reduced higher frequency harmonic drawn from the input DC source. DC voltage source of V_{DC} gaining a midpoint 'o'. L_{in_inv} and I_{in} are the DC bus component of inductor and current through it. $C_{in_inv}$and v_{in} are represents the DC bus capacitor and the capacitive voltage on it. V_{O_MG} and $i_{the\ O\_MG}$ are the grid voltage and current form the grid LCL lowpass filter. i_{L_inv} is the current flowing through the grid inductor of I_{O_MG}. The phase terminal of a sub-inverter leg formed by S_1 and S_2 complete input side of the inverter is multi-connection to the DC to DC boost converter [21]. Whereas, the one sub-inverter leg formed by S_3 and S_4 are connected to the inverter output grid filter that can be converted DC to AC power with the DC to DC terminal cooperation. The inverter output current and voltage are expected by the following (1) and (2) [19].

$$v_{O\_MG} = V_{DC} \times sin(\omega t) \tag{1}$$

$$i_{O\_MG} = I_{O\_MG} \times sin(\omega t - \varphi) \tag{2}$$

In these equations above, the power factor of the inverter is $\cos\varphi$and the fundamental grid frequency is ω_f. Then i_{L_inv} and V_{ab} is determined by following (3).

$$V_{ab} = V_a - V_b \tag{3}$$

(3) recommends that only $V_a - V_b$ requirements to be determined, where the values of V_a and V_b are unconstrained. If the DC bus distorted ripple current is ripple free, at that point the inverter input source should only be proposed the continuous power, and the grid lowpass filter of the capacitor must be twisted all the vibrating power. Reliable with the change power of the S-PSI, the determination of $I_{in_inv}, i_C$and V_C can be measured as the following equation.

$$I_{in\_inv} = \frac{V_{o\_MG} I_{O\_MG} cos(\varphi)}{2V_{DC}} \tag{4}$$

$$V_C = V_{in\_C\_O} + \frac{V_{ab} I_{L\_inv}}{4\omega C_{in} V_{in\_C\_O}} sin(2\omega t - \alpha + \beta) \tag{5}$$

$$i_{in\_C} = \frac{V_{ab} I_{L\_inv}}{2V_{in\_C\_O}} \times cos(2\omega t - \alpha + \beta) \tag{6}$$

In these equations above, $V_{in\_C\_O}$ is the input source DC bus component in V_C. In the letter case, the cancellation distortion harmonic frequency depends on the add number of interleaving angle and interleaved phases are utilized [1, 20]. Therefore, the carrier frequency of each switch's half phase inverter in the interleaved switching mechanism is lower whereas keeping the equal input current quality that can be developed reduce to switching loss of the inverter. The inverter DC bus inductor of L_{in_inv} is almost to zero when avoiding the cancellation distortion frequency in I_{in}. where, V_a and V_b are gained as the following equations.

$$V_a = V_a - V_{ab} \text{ and } V_b = V_{DC} \tag{7}$$

$$V_a = V_{DC} + V_{ab} \times sin(\omega t + \beta) \tag{8}$$

Figure 3 demonstrates the main waveforms of the S-PSI based on as shown in (1), (5), (7) and (8). The inverter DC ripple voltage is kept insignificant by correctly designing the inverter input DC bus capacitance.

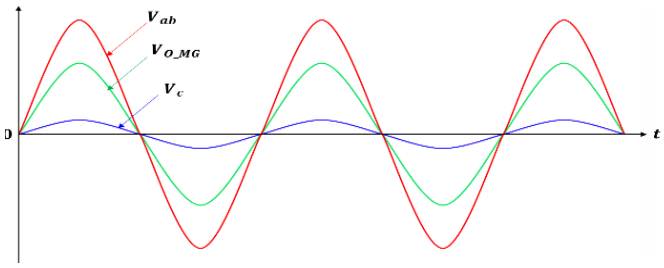


Figure 3. Main voltage waveforms of the S-PSI [1]

The predictable illustrates of the duty cycles of inverter upper switches which are S_1 and S_3 as shown in Figure 2 (a). Hence, the flywheel diodes like D_1 and D_3 expressed by the following (9) and (10).

$$D_1 = \frac{V_{DC}}{V_{in\_C\_O}} \tag{9}$$

$$D_3 = \frac{V_{DC}}{V_{in\_c\,O}} + \frac{V_{ab}}{V_{in\_C\_O}} \sin(\omega t + \beta) \tag{10}$$

Based on the duty factor of the half phase inverter upper switch of S_3, the currents flowing through each switch is assumed as the following Equations. When avoiding the even frequency harmonics distortion. The current reference directions are calculated in Figure 2.

$$i_{S_3} = D_3 \times i_{L\_inv} = \frac{V_{o\_MG}\, I_{O\_MG}\, cos(\varphi)}{2V_{in\_C\_O}} + \frac{V_{DC} I_{L\_inv}}{V_{in\_C\_O}} \sin(\omega t - \alpha) - \frac{V_{ab} I_{L\_inv}}{2V_{in\_C\_O}} \cos(2\omega t - \alpha + \beta) \tag{11}$$

$$i_{S_4} = (1 - D_3) \times i_{L\_inv} = -\frac{V_{o\_MG} I_{O\_MG}\, cos(\varphi)}{2V_{in\_C\_O}} + \frac{\left(V_{in_{C_O}} - V_{DC}\right) I_{L_i nv}}{V_{in\_C\_O}} \sin(\omega t - \alpha) + \frac{V_{ab} I_{L\_inv}}{2V_{in\_C\_O}} \cos(2\omega t - \alpha + \beta) \tag{12}$$

$$i_{S_1} = i_C + i_{S_3} = \frac{V_{o\_MG} I_{O\_MG}\, cos(\varphi)}{2V_{in\_C\_O}} + \frac{V_{DC}\, I_{L\_inv}}{V_{in\_C\_O}} \sin(\omega t - \alpha) \tag{13}$$

$$i_{S_2} = i_{S_4} - i_C + I_{in\_inv} = \frac{V_{o\_MG} I_{O\_MG}\, cos(\varphi)}{2} \left(\frac{1}{V_{DC}} - \frac{1}{V_{in\_C\_O}}\right) + \frac{(V_{in\_C\_O} - V_{DC}) I_{L\_inv}}{V_{in\_C\_O}} \sin(\omega t - \alpha) \tag{14}$$

In the above mention (11) and (12), the currents flowing through switches like S_3 and S_4 mainly comprehend DC bus voltage, critical and even harmonic elements as shown in Figure 2 (b). In the later case, (13) and (14) are represented that the currents flowing through S_1 and S_2 as shown in Figure 2 (a) only consist of the inverter input source of DC bus voltage and grid frequency elements. As a result, a CBGSC switches consents to gain the transfers functions vital for the proposed design of the S-PSI control of the different parameter of the grid-connected power system [14, 19]. The consideration parameters of the inverter

with switching controls are set that the dynamic model is same to a circuit voltage source inverter, enchanting into justification the point of the process is operated periodic signals modifications in the time of 50 Hz as exposed in Table 1.

Table 1. Considered parameters of the S-PSI under literature

Parameters	Unit	Value
Solar Panel Voltage (v_{PV})	V	170
DC Bus Voltage (v_{DC})	V	342
Output Grid Voltage (v_{o_MG})	Vrms	220
Fundamental Grid Frequency (f_g)	Hz	50
DC Bus Inductance (L_{inv})	H	$4e^{-3}$
DC Bus Capacitor (C_{in})	F	$570e^{-4}$
Inverter Side Filter Inductance (L_{inv_O})	H	$6e^{-4}$
Grid Filter Inductance (L_{MG})	H	$4.3e^{-4}$
Grid Capacitor (C_f)	F	$20.25e^{-4}$
Switching Frequency (f_c)	kHz	2.5
The resistance of damping (R_d)	Ω	$2e^{-3}$
Duty Cycle (D)	%	85

4. DESIGN PROCEDURE OF A SWITCHING GATE CONTROLLER

All switching modulation topologies applicable to S-PSI can be utilized in CBGSC with PWM system because switches pulse synchronizes half phase inverter make their outputs independently. In order to reach high efficiency, however, synchronous unpredicting PWM, which combine one phase in every switching interval period, is desirable in this case. This PWM system may be avoided inverter switching the phase terminal with the optimum current magnitude, then also eliminates switching the phase terminal going over zero crossing thus eliminates commutation disappointments. An evaluation between CBGSC with PWM system and other PWM methods, which is a sinusoidal carrier pulse with modulation and space vector modulation for single-phase two-level switching inverter was familiar in [9]. The author [15] described that CBGSC with PWM system not only decreases switching frequency loss, but also the input DC current ripple for series switching type of SPSI.

Figure 4 denotes the CBGSC with PWM for S-PSI that is divided into two steps. The step one upper part is te inverter switches control that switches the inverter power modification, and the other step lower is converter control that is in control of the inverter source voltage boosting. Whereas according to Figure 4, $G_{\mathrm{PI}(s)\ \mathrm{and}\ G_{\mathrm{MAF}(s)}}$ are the proportion-integral (PI) and the moving average filter. The inner current loop regulator is complicated to accomplish the DC bus current waveform. The PI controllers are expected by two loops such as $G_{\mathrm{PI-V}(s)}$ and $G_{\mathrm{PI-I}\,(s)}$, respectively. The outer loop regulator of the output signal is the reference of the inner loop which is defined as I'_{in_inv}.

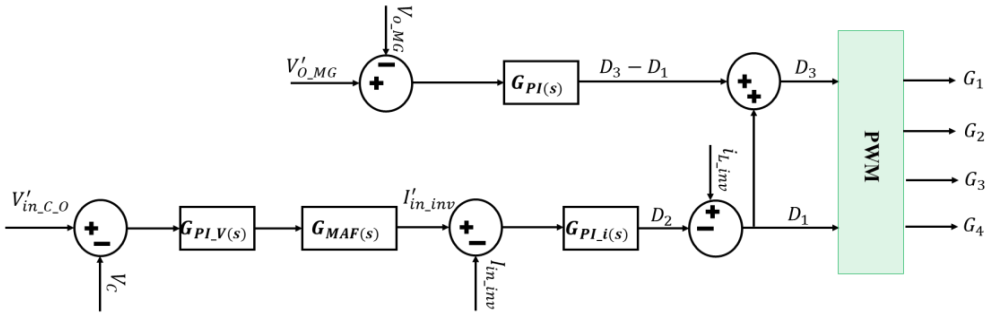


Figure 4. CBGSC scheme of an S-PSI [13]

As mentioned earlier, a few numbers of higher frequency harmonics in the DC bus capacitor voltage of V_C. The even frequencies harmonic elements are fed into the PI regulator of $G_{\mathrm{PI-V}(s)}$, and better-quality by it. Then a large amount of even harmonic frequency distortion element is seemed in I'_{in_inv}. Finally, over the inner loop regulator, there is happen an abundance of low add harmonic frequency distorted in the inverter source current of I_{in_inv} whereas no stages are employed. To reduce the low frequency harmonic distortion

components such as $I'_{in_inv}$and I_{in_inv}, the open-loop rise of outer loop current at $2f$ is decreased. A moving average filter is utilized for eliminating harmonic frequency distortion and its various harmonics in DC bus current reference I'_{in_inv}. Additionally, it is applied to the outer voltage loop regulator which can be defined as shown in (15) in s-domain [14]:

$$G_{\mathrm{MAF}(s)} = \frac{1-e^{-s\,N_S T_S}}{s\,N_S T_S} \tag{15}$$

Where, f_s is the sampling frequency, T_s=10μs, is the sampling time of switching, and N_s is the samples number are expected by the filter in a fundamental period. The small-signal similarity circuit and control block diagram of S-PSI is represented in Figure 5. The open loop transfer functions that relay the grid filter inductor current with the duty cycle of $G_{i_{O\_}d(s)}$ and the inverter output voltage with the duty cycle $G_{\mathrm{Vo}\_d(s)}$ are kept from the S-PSI dynamic models denoted.

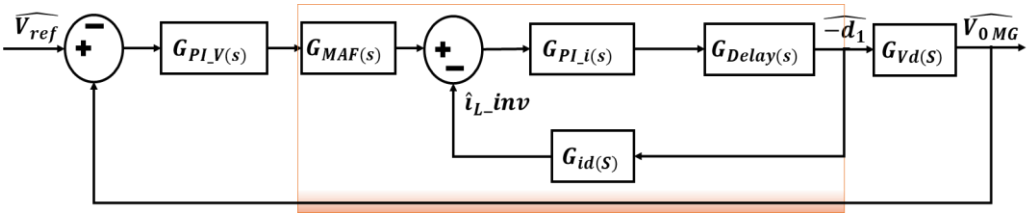


Figure 5. Input boost DC to DC converter control scheme [1]

According to Figure 5, D_1 is the duty cycle of the two-level switch of S_1; $R_{L\_inv\_D}$ means the equivalent load on DC bus voltage that can be known as $R_{L\_D} = V^2_{in\_C\_O} \div V_{O\_MG} I_{O\_MG} \cos(\varphi)$; the input filter equivalent series resistors (ESRs) are signified such as R_{L_in} and R_{C_in}. The variables with '^' is the small trepidations from their steady-state stabilities. Then the transfer functions are offered in (16) and (17) [20]. The $\frac{\widehat{V_C}}{\widehat{d_1}}$ is represented the duty factor of the input DC bus current transfer function are calculated as:

$$G_{VO\_d(s)} = \frac{\widehat{V_C}}{\widehat{d_1}} = \frac{V_{DC}(1+sR_{C\_in}C_{inv})[1-(sL_{inv}+R_{L\_inv})/(D_1^2 R_{L\_D})]}{G(s)} \tag{16}$$

$$G_{i_{O\_}d(s)} = \frac{\widehat{i_{L\_inv}}}{\widehat{d_1}} = \frac{V_{in\_C\_O}[s(1+2R_{C\_in}/R_{L\_D})C_{inv}+2/R_{L\_inv}]}{G(s)} \tag{17}$$

In the mention above Equations, $G_{Delay}(s)$ is the digital CBGSC delay effect and it is determined as $G_{Delay}(s) = e^{-0.1T_S s}$. The open-loop transfer functions of the outer and inner loops are defined as following (18) and (19).

$$G_{V\,OP}(s) = G_{PI-V(s)} G_{MAF\,(s)} \frac{G_{PI-I(s)} G_{Delay\,(s)} G_{VO\_d\,(s)}}{1+G_{PI-I(s)} G_{Delay\,(s)} G_{iO\_d\,(s)}} \tag{18}$$

$$G_{i\,OP}(s) = G_{PI-I(s)} \times G_{Delay\,(s)} \times G_{iO\_d(s)} \tag{19}$$

Firstly, the switching frequency is selected at almost 2.5kHz to keep the open loop gain at $2f$ higher enough for the inner loop while the phase margin is expected to higher than 60° to sustain this loop stable.

5. GRID COUPLE LOWPASS LCL FILTER DESIGN

The conventional topological construction is illustrated in Figure 6. This method can be utilized in single-phase PV grid-connected PSI. Where input DC bus voltage is V_{DC}, DC bus current is I_{DC}, S_1~S_4 four switches made up S-PSI, L_{inv_O}, C_f and L_{MG} are the grid coupled third-order LCL output filter [15].

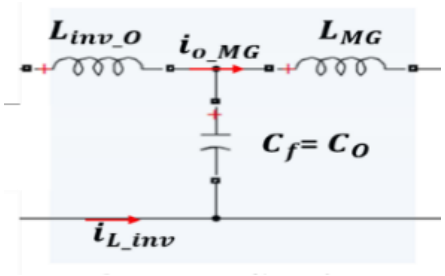


Figure 6. Equivalent circuit of grid couple lowpass LCL filter [1]

The plastic internal resistances of the LCL filter are negligible. The transfer function of the grid coupled inductor current to DC bus voltage is assumed as;

$$G_{M(s)} = \frac{G_{i(s)}}{G_{i(v)}} = \frac{1}{Ls} \times \frac{(s^2 + R_d C_f Z_{LC}^2 + Z_{LC}^2)}{(s^2 + R_d C_f \omega_{RES}^2 s + \omega_{RES}^2)} \quad (20)$$

$$P_{Loss} = 3 \times R_d \times \sum_h \left[i_{inv\_o}(h) - i_{MG}(h) \right]^2 \quad (21)$$

Then, the resonance grid lowpass LCL filter is made with a higher ripple current. One damping method, a series resistor relates to the shunt capacitor. Where the skin effect is neglected. The grid filter is additional to reduce higher harmonic frequency, then a convention filter quality depends on small reduction associated with what is expected because of oscillation effects. In this case, the DC bus ripple can cause an excess of the filter resonance. Hence, the inductors are correctly designed as DC bus ripple and damped to avoid resonances. However, the damping level is measured by the degradation of the filter efficiency, losses, and cost. Substantial the value of the filter is determined as a percentage of the filter base value by the following (22) and (23).

$$Z_{Base} = \frac{E_{p-p}^2}{P_{a\_p}} \quad (22)$$

$$C_{Base} = \frac{1}{Z_{base} \times \omega_{gf}} \quad (23)$$

Where, E_{p-p}^2 is the phase to phase voltage, ω_{gf} is the fundamental grid frequency and P_{p_p} is the active power of the S-PSI. The filter resonant frequency is shown to the switching frequency value calculated as the given (24).

$$\omega_{RES} = k \times \omega_{SW} \quad (24)$$

Where, the resonant frequency of ω_{RES}, the factor expresses of k and the switching frequency of ω_{SW}. Consequently, at the switching frequency of the S-PSI output side harmonic voltage is $V_{inv_{sw}}(h) \neq 0$ and at the switching frequency of the grid harmonic voltage is $V_{MG_{sw}}(h) = 0$. The DC bus current ripple flowing through the inverter output side into the microgrid side are calculated by the following (25).

$$\frac{i_{MG}}{i_{inv\_o}} = \frac{Z_{LC}^2}{|\omega_{RES}^2 - \omega_{SW}^2|} \quad (25)$$

Hence, $\omega_{SW}^2 = 4\pi^2 f_{sw}^2$, $\omega_{RES}^2 = L_T Z_{LC}^2 / L_{inv}$, f_{sw} is the switching frequency and $h_{sw} = {}^{\omega_{sw}}/_{\omega_n}$ is the witching harmonic order. The ripple current presented by the third-order filter is actual only if the LCL is correctly damped.

Finally, the first order, low order, and the higher order frequency harmonic currents get in decomposing the inverter output current. The ripple current is reduced because of inverter side coupled inductor which the flow through current. In the latter case, the filter capacitance is structuring a small amount of resistance to high order frequency harmonic, but the filter inductance is structuring high resistance, therefore the highe order frequency harmonic through of the filter capacitance

$$THD = \frac{\sqrt{\sum_{h=2}^{50} i^2(h)}}{i(1)} \quad (26)$$

At that point the port current of the first order and low order frequency harmonic flow through grid side filter inductance into a power grid. The resulting concert issues are utilized to validate the output microgrid filter efficiency, whereas the first three are low switching frequency pointers and the last two are high switching frequency pointers [3].

6. S-PSI GRID SYNCHRONOUS METHOD

To find out the proper phase angle of grid and inverter circuit, zero crossing-based circuits has been designed, with the required fundamental frequency, as shown in Figure 7. In the first step, grid reference signal such as voltage (v_a' and v_b') and current (i_a' and i_b') and DC bus reference signal such as v_{dc} and i_{dc} are taken to the sample circuit. Then, this sample circuit makes two types of signals such as DC sample voltage which are operated the DC component circuits and sample signals which are controlled the zero-crossing circuit [22]. The zero-crossing circuit has been designed in such a way that it can detect the zero-crossing point of phase angle and generate zero-crossing samples which are Z_a and Z_b.

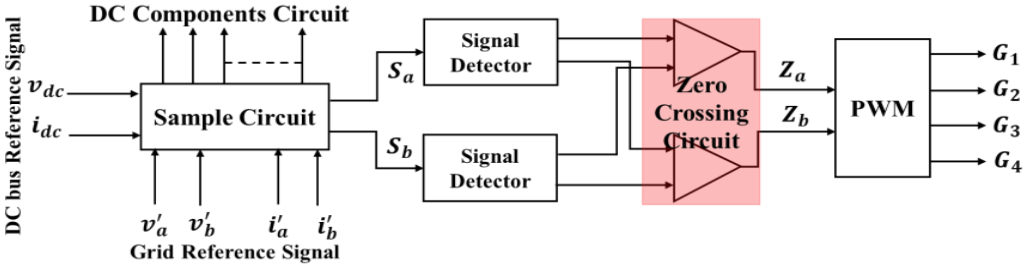


Figure 7. Zero crossing block diagram

Finally, these signals are passed through the PWM generator that can generate four pulses such as G_1, G_2, G_3 and G_4 by utilizing two zero-crossing sample signals [18]. Zero crossing is utilized to identify the phase angle as shown in Figure 8.

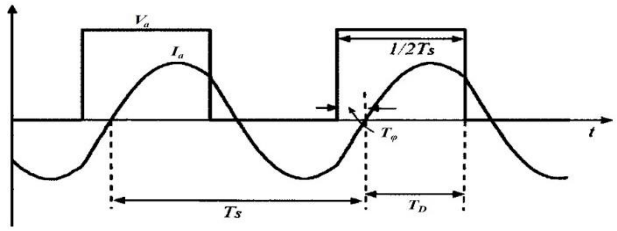


Figure 8. Half phase PSI voltage and current [22]

In the zero-crossing circuit, IGBT switching pulse has changed from the turn OFF to the turn ON state, which means changing to a high state from the low state to detect the desired phase. (27) shows that a sinusoid is a consideration under the signal.

$$V(t) = Vsin(\omega_o t) = Vsin(2\pi f_o t) \quad (27)$$

Then, the phase current has been swept from 0° to 90°.

$$T_D + T_\varphi = \frac{T_S}{2} \quad (28)$$

$$T_D = \frac{T_S}{2} - \varphi_{ref} \times \frac{T_S}{360^0} \quad (29)$$

Where T_D is the control variable, the phase angle command to current phase is φ_{res} and time response of currenthe t phase is T_φ.

$$\alpha = \frac{\varphi_{ref}}{90^0}$$

$$T_D = \frac{T_S}{2}(2\text{-}\alpha) \quad (30)$$

$$T_D\,[n] = \frac{T_S\,[n-1]}{4}(2\text{-}\alpha\,[n]) \quad (31)$$

Again,

$$\alpha\,[n] = \frac{\varphi_{ref}\,[n]}{90^0} \text{ When, } 0 \leq \alpha\,[n] \leq 1$$

$$T_D\,[n] = \frac{T_S\,[n-1]}{4}\left[\frac{(2^S-1)+(2^S-1-\alpha_1[n]}{2^S}\right] \quad (32)$$

Where S is the number of samples in the zero-crossing phase command and $\alpha_1[n]=0$ parallels to 0º, while $\alpha_1[n]=2^{S-1}$ parallels to 90º. For a large n, this error can be avoided.

7. SIMULATION AND RESULTS AND DISCUSSION

For the S-PSI, CBGSC with PWM method is used to synchronize the phase and frequency and reduce the switching loss. At first, reference sinusoidal signals are created utilizing a sinusoidal oscillator circuit. Therefore, the phase difference is 120° to the signal among the sinusoidal waves is created utilizing the phase shifter circuits. In this case, the triangular carrier wave is produced by a triangular wave circuit as shown in Figure 9. At that point, separate comparator circuits are made to utilize two switching signals such as G_1 & G_3 and utilizing two inverting circuit signals which are G_2 & G_4 are produced and these pulses switching signal are operated to IGBT of the S-PSI. If the control signal is greater than zero, switch S_1 is turned "ON" as a selection switching polarity in the grid cycle switching gate signals, IGBTs switches S_1 and S_4 are switched concurrently in this synchronous control mode, also S_3 and S_2 is inactive. Therefore, the synchronous gate pulse signals G_1 and G_3 are low. In the negative half cycle, if the reference control signal is higher than zero, S_3 is turned "ON" as a selection switching polarity in the half cycle of the grid synchronous gate pulse signals and IGBTs switches S_3 and S_2 switched simultaneously in this synchronous control mode.

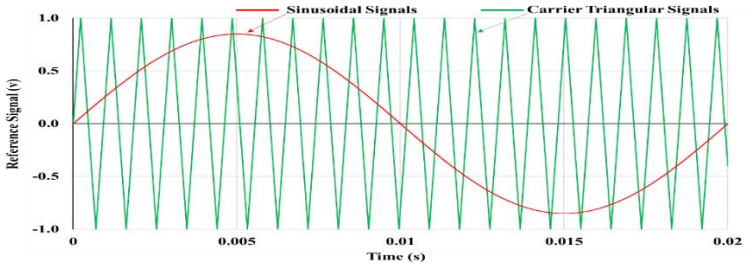


Figure 9. Reference sinusoidal and carrier triangular signal waveforms

So, the other switches S_1 and S_4 are inactive and G_3 and G_2 are low. The synchronous pulse signals produced, and its pattern is illustrated in Figure 10 that provide an idea switching of S-PSI.

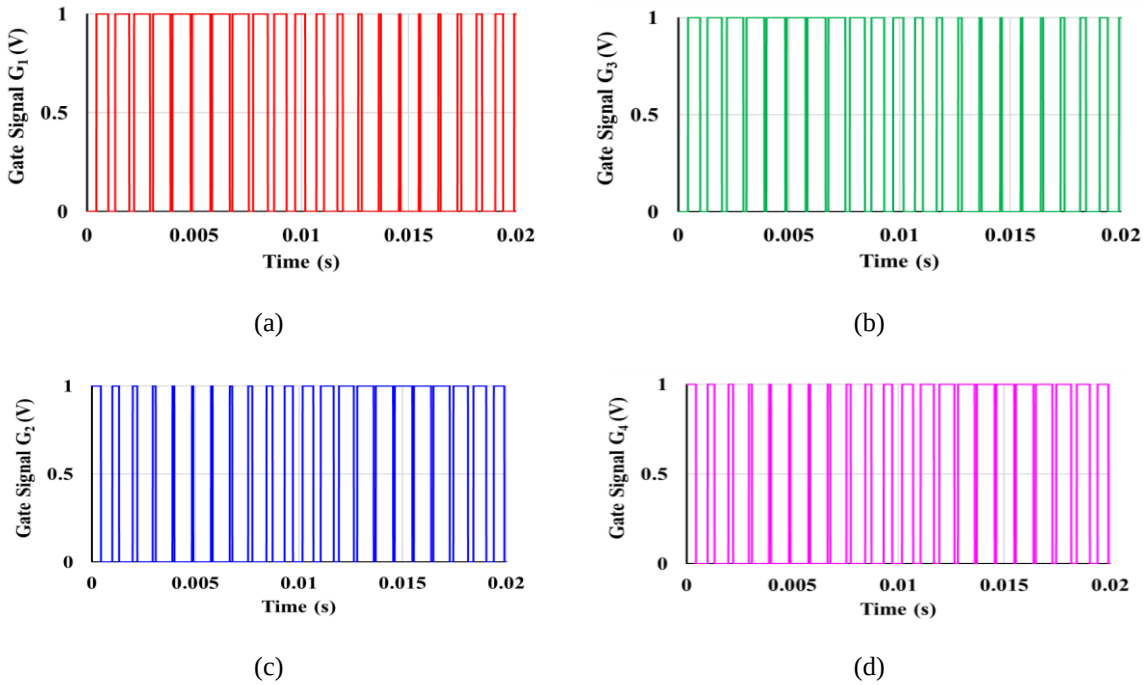


Figure 10. Separate comparator circuits signals (G_1, G_3, G_2 and G_4) for SPSI

The simulated results are compared with the concert of the S-PSI utilizing a CBGSC which is turned to give the maximum grid voltage. The grid rated line to line RMS voltage is 230V, the DC to DC output source voltage is ± 342V, the modulation index is 85%, the delay is 20µs, the sample is 4k/cycle and other parameters are considered. The outer voltage loop parameters of the DC to DC converter are k_{iu_1s} of 1.35, k_{pu_1s} of 0.3 and the MAF is denoted as (15) whereas N_s is 159. The inner loop current parameters are k_{ii_1s} of 0.99 and k_{pi_1s} of 0.007. in addition, the synchronous control parameters of the voltage loop are $k_{i\_1s}V_{C\_O\_inv(1s)}$ of 1 and k_{p_1s} $V_{C\_O\_inv(1s)}$ of 0.4.

Figure 11 demonstrations that the IGBT step response waveform for the initial condition of the S-PSI when only CBGSC is assumed for the dual control loop without outer loop voltage. From Figure 8, it is found that the switching delay of 10µs scheming to a positive response makes a loss development to the switching delay in 20µs. Figure 12 depicted that the DC to DC output waveform of the input DC bus voltage is around 342V using dual converters.

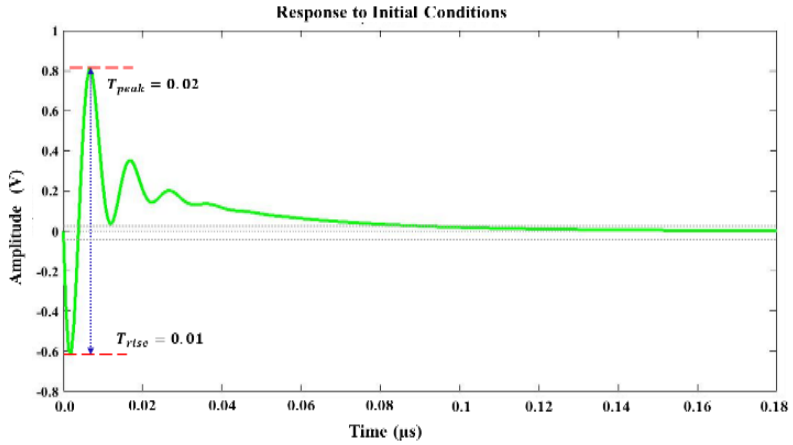


Figure 11. The step response waveform of the IGBT switch to the initial condition

The parameters for switching power loss of the S-PSI is close to but slightly greater than half of the one in the traditional inverter. The inverter has a high input DC bus ripple current which may lead to a larger switching loss of the IGBTs. The power losses are, individually, considered such as the DC bus inductor ESR of 0.54 Ω, DC bus capacitor ESR of 0.216 Ω, the input DC side inductor of 4mH and the input DC bus capacitor of $578e^{-4}$F. S-PSI without filtering condition, the control parameters of the switches in simulated which are operated to verify the theoretical equations and deliver the determined signal as represented in Figure 13 and Figure 14.

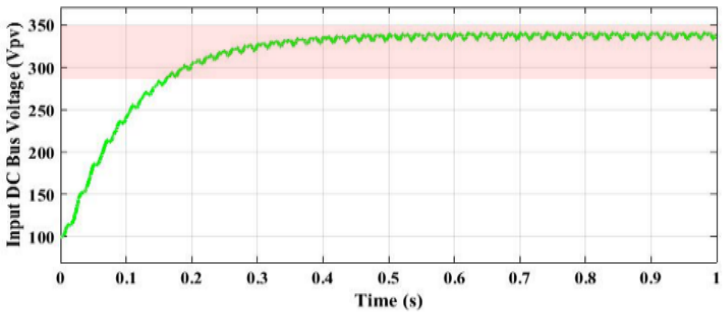


Figure 12. DC to DC converter output DC bus voltage waveform

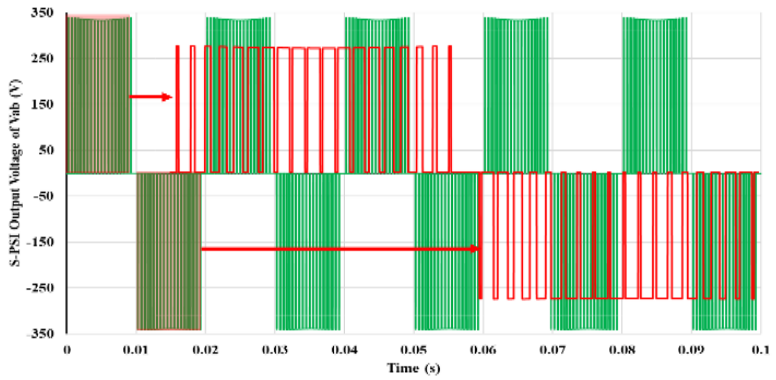


Figure 13. SPSI output voltage waveform without filtering condition [1]

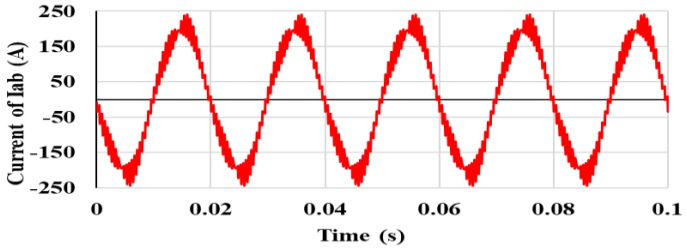


Figure 14. S-PSI output distorted current waveform without filtering condition [1]

From Figure 13 and Figure 14 the steady-state analysis of the S-PSI output voltage waveforms, it is noticed that the output voltage is a carrier-based synchronous PWM signal that pulse amplitude is almost 680V $_{pp}$ and the current is almost 400A peak to peak. As a result, the simulated results have a great agreement with the achieved results utilizing theoretical and simulated. In the latter case, the dynamic analysis is evaluated by utilizing a step response in the voltage and current reference during the filtering

condition mode. The inverter output distorted squire wave signals are passed through a grid lowpass LCL filter that can be converted to square wave into pure sine wave as represented in Figure 15 and Figure 16.

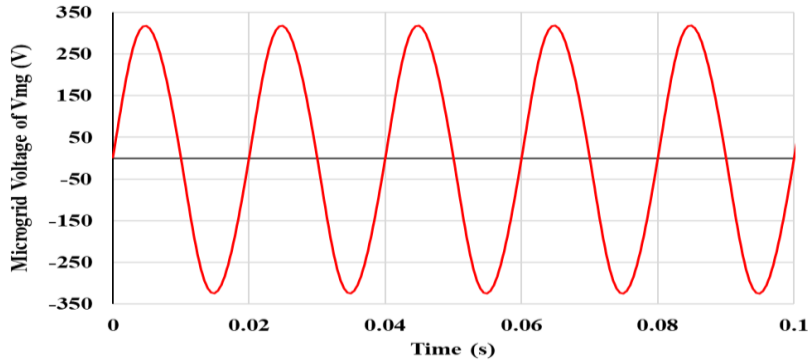


Figure 15. Harmonic free 50Hz grid voltage waveform with filtering condition [1]

S-PSI output with filtering condition, it is observed that the grid magnitude is almost 220V_{RMS} peak to peak, whereas 11Ω of the load resistance. Additionally, the grid current waveform is almost 20.18A_{RMS} peak to peak, whereas 85% of the duty cycle, at t=0.1s and 4000 of the sample per cycle.

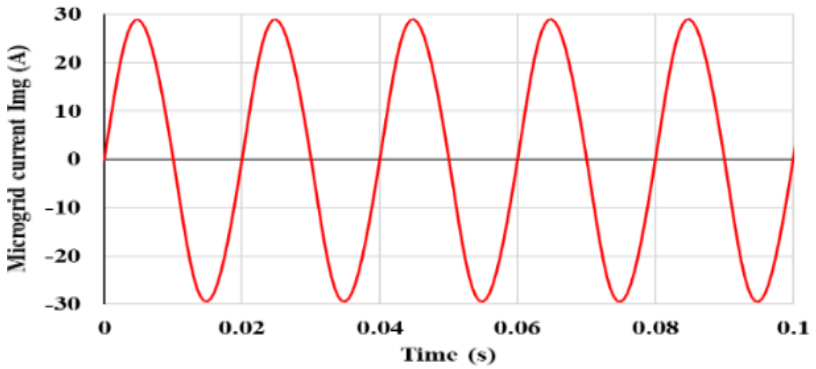
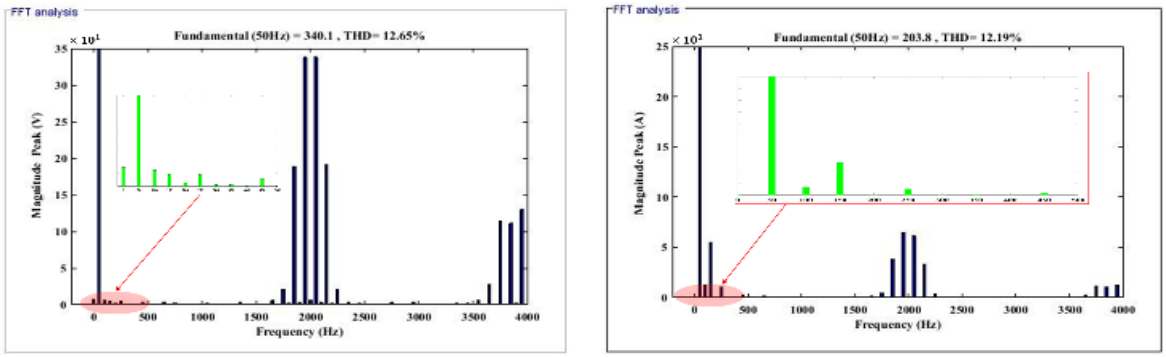


Figure 16. Harmonic free 50Hz grid current waveform with filtering condition [1]

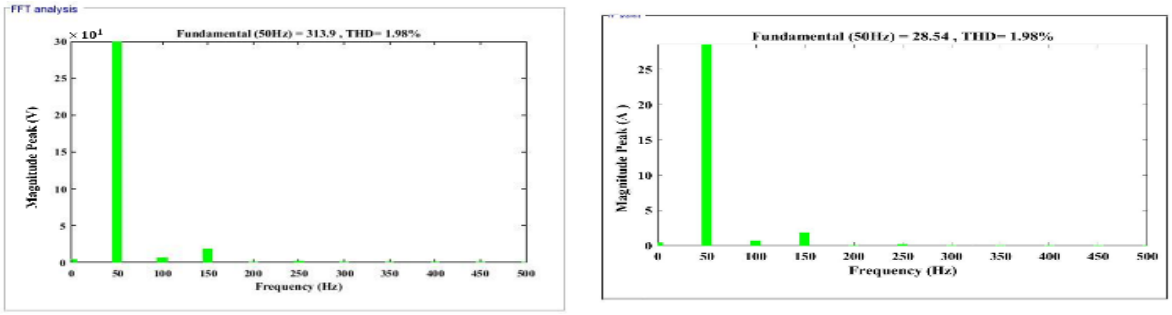
Figure 17 demonstrations the FFT for S-PSI output voltage and current waveforms attained by utilizing without filtering signals. The measured THD is represented in Figure 17 (a), without filtering the output voltage THD is around 12.65% while output current THD is around 12.19%. However, the determined SPSI voltage and current have some low-frequency harmonics distortion, with about a 12.4% amplitude relative to the fundamental.

With the filtering condition, the FFT of grid magnitudes is very close such as a voltage of 1.98% and current of 1.98%, respectively, as shown in Figure 17. It is clearly renowned that utilizing grid coupled LCL lowpass filter to reduce THD which is more than 11% of THD error.



(a) (b)

Figure 17. FFT analysis of the S-PSI, (a) voltage, (b) current THD waveforms without filtering [1]



(a) (b)

Figure 18. FFT analysis of the grid, (a) voltage, (b) current THD waveforms with filtering [1]

The sinusoidal signal is the angle of Φ in degrees that the waveform can be shifted from a positive reference signal point along the zero axes of the horizontal. Generally, the phase shift is the adjacent difference between two or more signals along a sinusoidal waveform and the mutual axis of the same frequency. When grid load resistor of 11Ω is coupled to a filtering sinusoidal grid voltage supply, whereas the current flowing through the grid load resistor can fluctuate in proportion to the grid voltage which is the voltage and current waveforms are the same phase with each other synchronized. Figure 19 shows the output signal frequency and phase analysis. From the frequency analysis, it is seen that the inverter phase angle is almost synchronized as grid phase, which is approximately 4.67° lagging of phase angle error whereas the frequency is 52Hz.

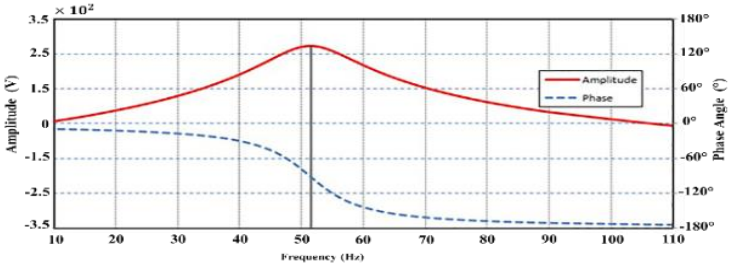


Figure 19. Frequency vs phase analysis of the S-PSI amplitude [1]

The S-PSI phase error is almost the same as microgrid phase due to carrier-based synchronous control in which the phase error is 55% improvement of the system. Figure 20 shows the Nyquist plot for a second-order system of the S-PSI stability analysis. It is found that the closed loop or open loop transfer function has two zeros in the right half plane which equivalently has two poles.

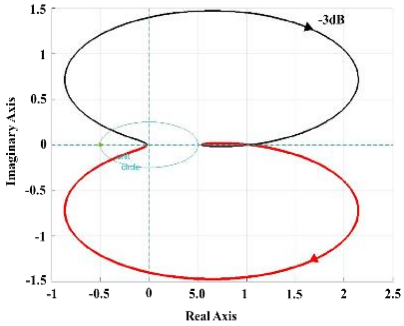


Figure 20. Nyquist plots of the S-PSI [1]

8. EXPERIMENTAL RESULT VERIFICATIONS

To establish the analysis above, some experiments are performed on the S-PSI and the experimental results evaluation showed with the S-PSI prototype made, including voltage waveform, THD, and efficiency. The prototype printer circuit bode of the S-PSI is illustrated in Figure 21. The circuit bode dimensions are $12^{"} \times 10^{"} \times 1.5^{"}$, board thickness of $1.55\text{mm} \times 50\mu m$ and clearance are 10mm of top and 1mm of the bottom.

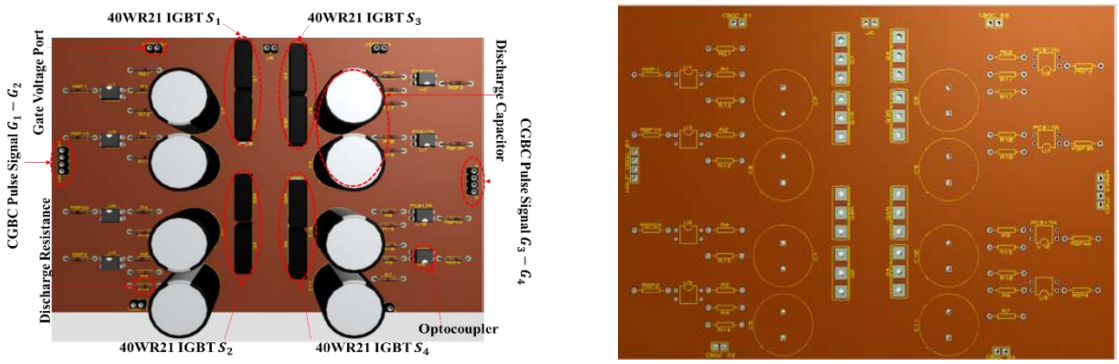
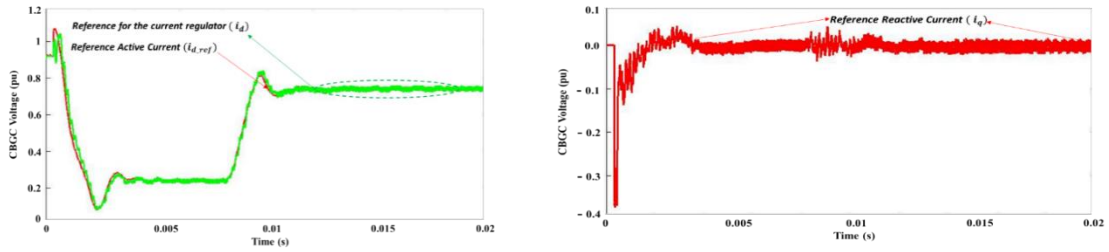


Figure 21. 3D PCB for S-PSI

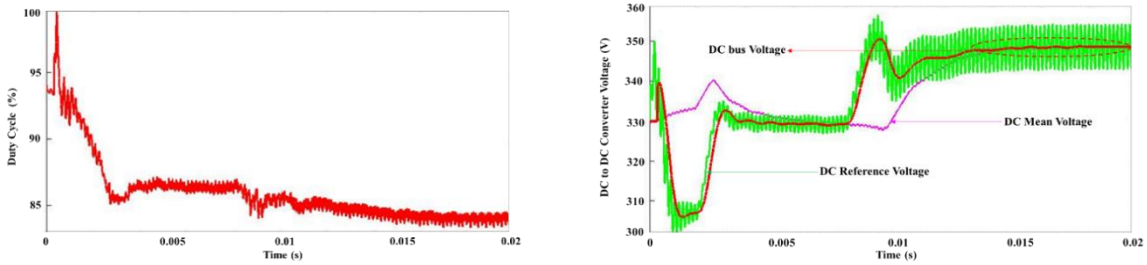
Experimental waveforms of the inverter controller found at reference active and reactive current are depicted in Figure 20, where i_d, i_{d_ref} and i_q are the regulator reference current, reference active current and reference reactive current. From Figure 22 (a), the reference active current is closed to reference for the current regulator after 0.01s. While, the reference reactive current is close to zero at 0.001s. Therefore, the power supply of the reactive from inverter regulator is predictable to increase the voltage lebel of the grid. It occurs in the grid synchronizing after the reference reactive current is needed higher than the making due to the instantaneous influences of an inductive load in the system. If the reference reactive current to the point of interconnection is the likely way of falling the effect of the reference reactive current imbalance.



(a) (b)

Figure 22. The controller of the CBGSC reference, (a) active, (b) reactive currents

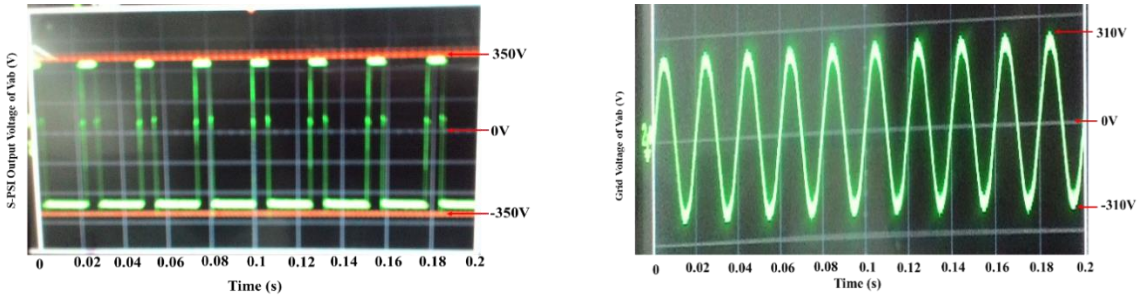
Duty Cycle is the time during percentage which that the inverter output signal is in an active state. Figure 23 represents the S-PSI duty cycle effect waveform and inverter input DC bus voltage. Consequently, in Figure 23 (a), it is clearly noticed that the initially the duty cycle is almost 100% because the output voltage is close to zero after that the time is increased the duty cycle decreased at 0.001s. The duty cycle is a little bit higher at the time of 0.005 to 0.01s. Finally, the duty cycle is 85%, whereas at the time of 0.015s. From Figure 23 (b), it is observed that the input DC bus voltage is almost balanced at the point of 0.01s which is around 342V and the sum of the reference and mean voltages are equivalent as bus voltage.



(a) (b)

Figure 23. S-PSI for, (a) duty cycle waveform, (b) DC bus voltage

Experimental output inverter voltage waveform obtained at nominal output voltage without filtering is demonstrated in Figure 24 (a), the parallel to the voltages of two half phase terminals with respect to the input DC bus center point which is induced the voltage difference between these voltages. It is seen that the prototype and simulated results are almost the same which is 350V peak voltage.



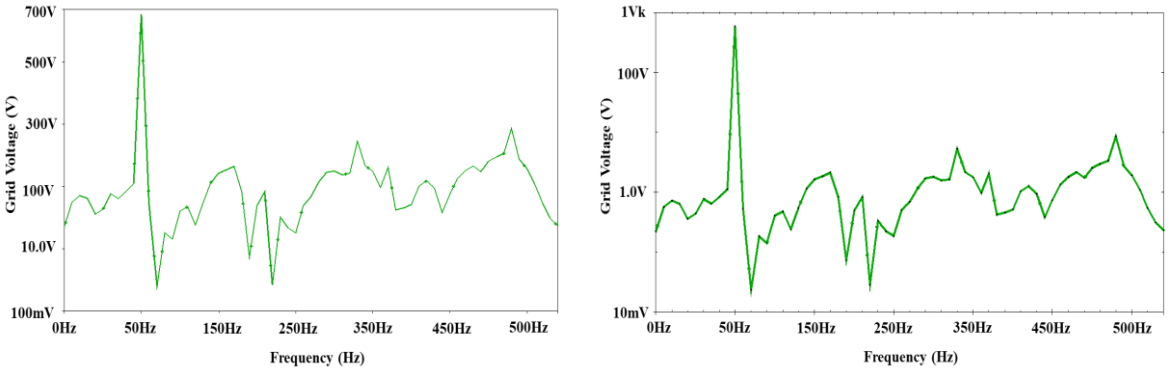
(a) (b)

Figure 24. The Experimental voltage waveform for, (a) without filtering S-PSI, (b) with filtering grid

As observed, Figure 24 (b) is represented by filtering condition, while the grid line to line voltage is around 310V peak which is almost equal as a simulated result. In addition, the grid inverter current is nearly sinusoidal and grid phase voltage is depicted to excellently clamp their process to the positive and negative input DC bus rails during the period after the corresponding grid phase currents are close to zero. However, the FFT analysis of the prototype S-PSI voltage waveforms without and with filtering condition is shown in Figure 25. The measure voltage THD at without filtering is about 14.6% and with filtering is 2.30% which are the same as simulated results.

Table 2 represents the sets of simulated and prototype results are established as produced from the point prediction and the goal of optimizing the overall system conversion efficiency with decreased higher frequency harmonic distortion and improved phase synchronize. It is clearly seen that the dynamic response of the SPSI system has been tested by the step of the altering grid resistive load from 87.58% to 100%. Moreover, is is also found that the SPSI phase angle is 4.67° lagging whereas the other parameters are

consideraded in this case. Consequently, the optimumized value is gained approxmetlly 97.02% of the overall system efficiency.



(a) (b)

Figure 25. FFT for S-PSI output voltage waveforms, (a) without filtering, (b) with filtering conditions

Table 2. Comparison between S-PSI and benchmark results

Switching Freq.	Duty Cycle	Input Voltage	Output Voltage	THD	Phase Angle	Efficiency	Reference
kHz	(%)	(V)	(Vrms)	(%)	(°)	(η)	
15.9	50	200	110	3.3	N/A	91.2	[19]
2.65	85	170	220	1.98	4.67	97.02	S-PSI

9. CONCLUSIONS

This paper represents the design and prototype implementation of series switching SPSI interleaved CBGSC with PV application, which performances with relations steady-state error, transient response, dynamic response and higher frequency harmonics. Form the analysis, it is noticied that the phase angle of the SPSI was developed at 4.67° lagging which is 55% lower than the maximum allowable angle (Phase angle 5°) as per IEEE standard due to the use of CBGSC. Moreover, the inverter output THD voltage and current waveforms were decreased from 12.42% of without filtering to 1.98% of with filtering condition. In the leater case, the proposed S-PSI system recommended that the design switching logic methods were more significant as the maximum acceptable THD is <5% as per IEEE standard. It is observed from the simulated and experimental results that the overall system efficiency of the S-PSI is 97%. Finally, the verified results exposed the CBGSC is higher in terms of sinusoidal voltage and current reference tracking with zero steady-state error, slightly slower transient response and very low total harmonic distortion.

ACKNOWLEDGEMENTS

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