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Design, modelling and simulation of controlled sepic DC-DC converter-based genetic algorithm

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ABSTRACT

This paper discusses various aspects of a single-ended primary inductance DC-DC converter (SEPIC). The focus is on design, modelling, and simulation results of a SEPIC converter. The study analyses the principle of SEPIC operation when operated in continuous conduction mode (CCM). Additionally, the mathematical equations for the design modules are calculated as per converter requirements. State-space equations are used to formulate the state-space model of the SEPIC converter. To satisfy the best-performance criterion of the system, the parameters for controller (K_p, K_i, K_d) should be tuned or optimized using the genetic algorithm (GA) optimization technique. Controller parameters are determined using an objective function that minimises the integral time absolute error (ITAE). Simulations performed on a closed-loop system reveal that the step response with a PID controlled based GA displayed superior performance. A closed-loop system has a substantially bigger stability region compared to an open-loop system. The simulation optimised performance metrics like maximum overshoot percentage (M_p), rise time (t_r), and settling time (t_s). MATLAB/Simulink R2018a® and m-file code are used for the system modelling, simulation, and optimization of the PID controller parameters based on the GA.

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1. INTRODUCTION

The power shortage relative to the cumulative demand for load is considered to be a major problem in many countries where it has become impossible to generate sufficient energy using traditional means. These difficult situations have led researchers to focus on finding alternative ways to generate energy [1, 2]. Power electronic converters such as DC-DC converters (sometimes called switching regulators) are primarily implemented to improve energy conversion efficiency when extracting electric power [3]. DC-DC converters are circuits which typically supply a constant output and convert DC voltage to a different voltage level. These are used for obtaining stabilized or changing DC voltage(s) by increasing, decreasing, or multiplexing from any DC source [4, 5].

There are two types of DC-DC converters, isolated and non-isolated. Flyback and forward converters are variants of isolated DC-DC converters [6]. These use a high-frequency transformer to place an electrical barrier and isolate both the input and output of these converters. A significant advantage of isolated converters is that they protect sensitive loads [7]. On the other hand, non-isolated DC-DC converters have no

such electrical barrier. Some examples of non-isolated converters are buck-boost converter, buck, boost, CUK, ZETA, and SEPIC converters [8, 9]. Non-isolated DC-DC converters are cost-effective and easy to design when compared to their isolated counterparts.

The converters have diverse applications in electric traction, electric vehicles, distributed-DC systems like space applications, ships, and airplanes [10, 11]. Solar photovoltaic and specialised electrical machine drives are other areas where the converters are useful [12, 13]. Different systems have specific requirements and the DC-DC converter used for the applications should be carefully chosen to have a high-efficiency system with excellent power quality [14]. This paper focuses on the single-ended primary-inductance DC-DC Converter (SEPIC). The SEPIC converter is able to reduce or raise the electrical potential (voltage) at the output and can be considered as a buck/boost converter [12]. Additionally, the SEPIC DC-DC converter is also capable of producing a regulated positive output voltage for any input voltage. This is in contrast to other converters like CUK or ZETA that provide a negative regulated output voltage [15–17]. The structure of the paper is specified as follows: introduction, principle of operation of the SEPIC converter, state-space modelling for the SEPIC converter, parameters and design components required for the converter, MATLAB simulations and modelling the SEPIC converter, genetic algorithm to optimise the PID parameters to control the SEPIC converter, results from the simulation, and discussion.

2. PRINCIPLE OF OPERATION OF SEPIC CONVERTER

The operating principle for a SEPIC DC-DC converter used in continuous conduction mode (CCM) is described in Figure 1. The diagram shows an input voltage source (V_S), a couple of inductors (L_1 and L_2), a coupling capacitor (C_1) that is connected to the inductors to ensure that a current path exists for the DC flow and to also provide insulation [14], power diode (D_1), output filter capacitor (C_2), and a switching device. Usually, the switching device is an insulated gate bipolar transistor (IGBT) labelled (S_1). The load resistance of the circuit (R) is also shown.

The SEPIC converter has two operating modes: one is the CCM, the other is the discontinuous conduction mode (DCM). In this paper, the first mode is considered to have two states, which can be described as follows.

2.1. SEPIC converter operating modes

2.1.1.State I (0 < t < D)

When S1 is switched ON, the current I_{L1} increases. Current flowing through the second inductor I_{L2} also increases but in the negative direction. The energy stored in the first inductor L_1 increases. Therefore, capacitor C_1 supplies energy to increase the current in I_{L2}. SEPIC converter operation mode with switch S_1 ON is shown in Figure 2.

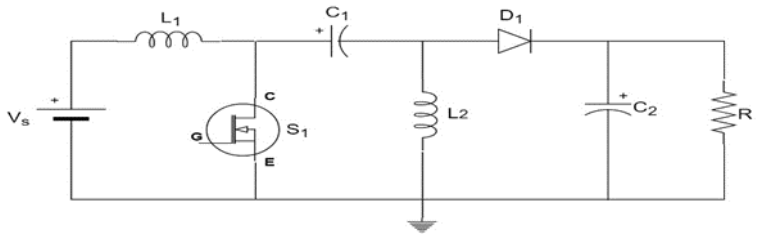


Figure 1. Circuit diagram of SEPIC DC-DC converter

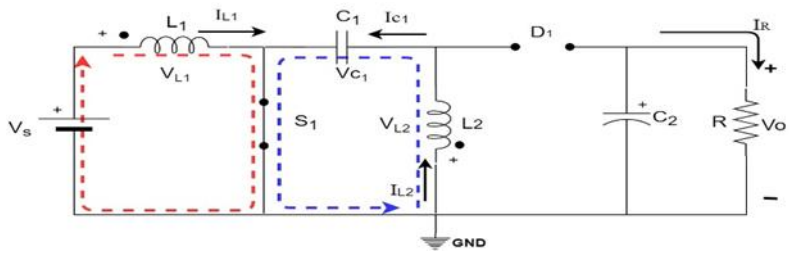


Figure 2. SEPIC converter operation mode when S1 is ON

The corresponding equations to **state I** of CCM using **KVL** and **KCL** are shown in (1), (2), (3), and (4).

$$V_S - L_1 \frac{d\,iL1}{dt} = 0 \quad (1)$$

$$C_1 \frac{d\,Vc1}{dt} + i_{L1} = 0 \quad (2)$$

$$L_2 \frac{d\,iL2}{dt} - V_{C1} = 0 \quad (3)$$

$$C_2 \frac{d\,Vc2}{dt} + \frac{Vc2}{R} = 0 \quad (4)$$

2.1.2.Stae I (0 < t < D)

When switch S_1 is turned off, the capacitor input current (I_{C1}) equals the current through the inductor (I_{L1}). Current I_{L2} remains in the negative direction and does not reverse its direction. Diode D_1 actively conducts. SEPIC converter operation mode with switch S_1 OFF is depicted in Figure 3.

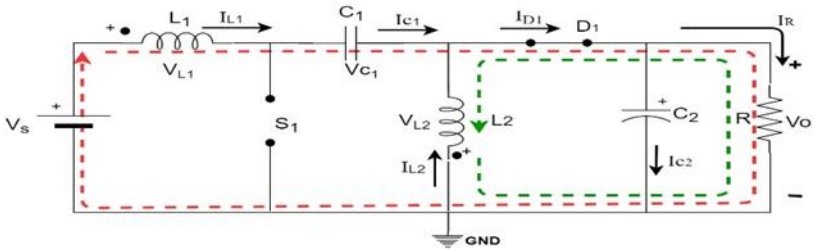


Figure 3. SEPIC converter operation mode when S_1 is OFF

The corresponding equations to state II of CCM using KVL and KCL are shown in (5), (6), (7), and (8).

$$V_S = L_1 \frac{di_{L1}}{dt} + v_{C1} + v_{C2} \quad (5)$$

$$L_2 \frac{di_{L2}}{dt} + V_{C2} = 0 \quad (6)$$

$$C_1 \frac{dv_{C1}}{dt} - i_{L1} = 0 \quad (7)$$

$$C_2 \frac{dv_{C2}}{dt} - i_{L1} - i_{L2} + \frac{v_{C2}}{R} = 0 \quad (8)$$

2.2. State space modelling of SEPIC DC-DC converter

The general state space equations for the SEPIC operating under state I of CCM can be given as in equations (9) and (10).

$$\dot{x}(t) = A_1\, x(t) + B_1\, u(t) \quad (9)$$

$$y(t) = C_1\, x(t) \quad (10)$$

Then, the state matrix for the SEPIC operating under **state I** is given in (11) and (12).

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{dv_{C1}}{dt} \\ \frac{dv_{C2}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L2} & 0 \\ 0 & \frac{-1}{C1} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{RC2} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_S \quad (11)$$

$$y(t) = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \end{bmatrix} \quad (12)$$

Similarly, the general state equations for the SEPIC converter operating under state II of CCM are given in (13) and (14).

$$\dot{x}(t)= A2\ x\ (t) + B2\ u(t) \quad (13)$$
$$y(t) = C_2\ x(t) \quad (14)$$

Then, the state matrix for the SEPIC converter operating under state II can be given as shown in (15) and (16).

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{dv_{C1}}{dt} \\ \frac{dv_{C2}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-1}{L1} & \frac{-1}{L1} \\ 0 & 0 & 0 & \frac{-1}{L2} \\ \frac{1}{C1} & 0 & 0 & 0 \\ \frac{1}{C2} & \frac{1}{C2} & 0 & \frac{-1}{RC2} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_S \quad (15)$$

$$y(t) = [0 \quad 0 \quad 0 \quad 1] \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \end{bmatrix} \quad (16)$$

The average form of the state matrix over a switching cycle for the SEPIC converter is as given in (17) and (18).

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{dv_{C1}}{dt} \\ \frac{dv_{C2}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{D-1}{L1} & \frac{D-1}{L1} \\ 0 & 0 & \frac{D}{L2} & \frac{D-1}{L2} \\ \frac{1-D}{C1} & \frac{-D}{C1} & 0 & 0 \\ \frac{1-D}{C2} & \frac{1-D}{C2} & 0 & \frac{-1}{RC2} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_S \quad (17)$$

$$y(t) = [0 \quad 0 \quad 0 \quad 1] \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \end{bmatrix} \quad (18)$$

Where A represents the system matrix, B represents the input matrix, C represents the output matrix, and D represents the duty cycle of the SEPIC converter within the range of (0–1).

2.3. Component design of SEPIC DC-DC converter

It is necessary that the selection of the main components in the converter design improve the output power efficiency without increasing cost, especially in high-volume power electronic applications. Based on the above, this section of paper focuses on choosing components and deriving their mathematical expressions when designing a SEPIC DC-DC converter to meet the requirements tabulated in 1.

2.3.1.Component design of SEPIC DC-DC converter

The principle of volt-second balance takes into account the voltage drops at diode (D_1), i.e. according states to the volt-second balance for a converter operating in a steady state, the average voltage during one switching cycle of the inductor must be zero [16]. Firstly, the voltage can be seen by L_1 during interval ($0 < t \leq D_T$) equals to ($V_{L1}=V_s$), while, during the interval ($D_T < t \leq T$), it equals ($V_{L1}=V_S-V_{C1}-V_D-V_O$). Taking the average over the entire interval and making it equal to zero, equation (19) can be obtained as:

$$\frac{1}{T}\left(\int_0^T V_{L1}dt\right) = \frac{1}{T}\left[\int_0^{DT} V_S\,dt + \int_{DT}^{T}(V_S - V_{C1} - V_D - V_O)dt\right] = 0 \quad (19)$$

Finding the integral and rearranging the above equations yields equation (20)

$$V_{C1} + V_D + V_O = \frac{V_S}{1-D} \quad (20)$$

Similarly, by taking the volt- second balance for L_2. Hence, the voltage can be seen by L_2 during interval ($0 < t \leq D_T$) is equal to ($V_{L2}=V_{C1}$), while during the interval ($D_T < t \leq T$), the voltage is equal to $V_{L2}=-V_O+V_D$ which gives (21).

$$\frac{1}{T}\left(\int_0^T V_{L1}dt\right) = \frac{1}{T}\left[\int_0^{DT} V_{C1}\,dt + \int_{DT}^{T}(-V_O - V_D)\,dt\right] = 0 \quad (21)$$

$$V_{C1} + V_O + V_D = \frac{V_O+V_D}{D} \quad (22)$$

By combining (20) and (22), the transfer ratio or voltage gain (G) of the SEPIC converter in terms of (D) can be obtained as shown in (23).

$$G = \frac{V_O+V_D}{V_S} = \frac{D}{1-D} \quad (23)$$

The value of (G) can be greater than or less than one, depending on the value of the duty cycle (D).

2.3.2.Calculation of minimum and maximum duty cycle

Depending on the voltage gain in equation (23), the minimum duty cycle (D_{min}) occurs when the input voltage is at a maximum value ($V_{S\,max}$) and it can be expressed as shown in (24).

$$D_{min} = \frac{V_O+V_D}{V_O+V_D+V_{S\,max}} \quad (24)$$

However, the maximum duty cycle (D_{max}) may occur when the input voltage is at a minimum value ($V_{S\,min}$), as given in (25).

$$D_{max} = \frac{V_O+V_D}{V_O+V_D+V_{S\,min}} \quad (25)$$

2.3.3.Inductor L_1 and L2 selection

In switch mode power supply (SMPS), the main function of the inductors is to store energy in their magnetic field and attempt to maintain a constant current, or equivalently, to limit the rate of change in current flow to the output. Selecting an inductor is necessary to the overall design of a converter. Normally, the inductance value of a converter should be set to limit the peak-to-peak ripple current flowing to the output. The inductance value that satisfied the requirements in the design of the SEPIC converter was estimated by rearranging (1), presented in the previous section, and substituting ($di_L = \Delta I_L,\ dt = DT,\ T = \frac{1}{f_s}$), to yield (26).

$$L_1 = L_2 = \frac{V_{S\,min}*D_{max}}{f_S*\Delta I_L} \quad (26)$$

2.3.4. Coupling capacitor C_1 selection

Capacitors have several functions in SMPS design, such as energy storage, filtering, compensation, etc. Typically, SMPS stages, the capacitance stores energy as an electric field due to the voltage applied and attempts to maintain a constant input and output voltage. To calculate the optimal value of (C_1) in the SEPIC converter circuit shown in Figure 1 with an acceptable level of voltage ripple to satisfy the requirements and stability of the converter, the capacitance formula shown in (27) was used.

$$C = \frac{\Delta Q}{\Delta V} \quad (27)$$

Equation (27) can then be rewritten, as the change in voltage is proportional to the change in charge over its capacitance, which yields (28).

$$\Delta V = \frac{\Delta Q}{C} \quad (28)$$

However,

$$\Delta Q = \int i(t)dt \quad (29)$$

Thus, (29) is substituted into (28) to determine the value of input capacitor (C_1) as shown in (30). Hence, it should be noted that (C_1) is charged by ($I_{L2} = I_{Omax}$) during the time interval ($0 < t \leq DT$).

$$C_1 = \frac{\int_0^{DT} I_o \, dt}{\Delta V_{C1}} \tag{30}$$

Solving the integration shown in (30) gives (31).

$$C_1 = \frac{I_{Omax} * D_{max}}{\Delta V_{C1} * f_s} \tag{31}$$

2.3.5. Output capacitor C_2 selection

Likewise, as in the coupling capacitor (C_1) calculation, the value of output capacitor (C_2) as obtained in (32) should supply the output current ($I_{o\,max}$) which is loaded during the ON state.

$$C_2 = \frac{I_{Omax} * D_{max}}{\Delta V_{C2} * f_s} \tag{32}$$

Where D_{min}, D_{max} are the maximum and minimum duty cycles respectively , $V_{s\,max}, V_{s\,min}$ are maximum and minimum input voltages respectively, V_O is the output voltage in volts, and ΔI_L is the same peak-to-peak ripple current in amperes for both inductors L_1 and L_2 when the minimum input voltage ($V_{s\,min}$) and switching frequency (f_s) are applied, it may be expressed as approximately (ΔI_L=20% $*I_{in\,max}$). ΔV_{C1}, ΔV_{C2} are the peak-to-peak voltage ripples in volts at capacitors C_1 and C_2, respectively. The acceptable percentage value of ripple voltage used in this paper is (ΔV_{C1}= 1% $*V_{S\,min}$ and ΔV_{C2}=1% $*V_O$).

2.4. Matlab simulation of SEPIC DC-DC converter

The open loop SEPIC DC-DC converter was implemented using the MATLAB® simulation platform R2018b Simulink [18]. For the purpose of simulation, the components of the SEPIC converter and their values tabulated in the Table 1 depend on the equations derived in pervious sections.

Table1. Component values of the designed SEPIC Converter

No	Parameter	Symbol	Value
1	Minimum input voltage	$V_{S\,min}$	100 V
2	Maximum input voltage	$V_{S\,max}$	120 V
3	Output voltage	V_O	311 V
4	Maximum output power	$P_{O\,max}$	2 Kw
5	Maximum load resistance	$R_{L\,max}$	~ 50 Ω
6	Maximum load current	$I_{O\,max}$	6.43 A
7	Switching frequency	f_S	25 kHz
8	Diode drop voltage	V_d	0.7 V
9	Minimum duty cycle	D_{min}	0.722
10	Maximum duty cycle	D_{max}	0.757
11	Current ripple at L_1 , L_1	ΔI_L	4.01 A
12	Voltage ripple at C_1	ΔV_{C1}	1 V
13	Voltage ripple at C_2	ΔV_{C2}	3.11 V
14	Coupling capacitor	C_1	195 µF
15	Output capacitor	C_2	63 µF
16	Inductor 1	L_1	755 µH
17	Inductor 2	L_2	755 µH

The output to the input voltage transfer function, $G_{(s)}$ can be derived from the average state (17) and (18) by using the formula to convert the state-space matrix to a transfer function, shown in (33), and substituting the values of the design parameters and components to obtain (34).

$$G(s) = C\,(SI-A)^{-1}\,B \tag{33}$$

$$\frac{V_o(s)}{V_{in}(s)} = \frac{5.135*10^8\,S^2 + 1.824*10^{-6}\,S + 2.642*10^{15}}{S^4 + 330.2*\,S^3 + 6.792*10^6\,S^2 + 1.419*10^9\,S + 8.478*10^{12}} \tag{34}$$

2.5. Genetic algorithm (GA)

GAs are stochastic global search engines that simulate the creation of natural processes. A GA starts with an initial population of chromosomes, each of which represents a possible solution to the problem, and the reliability of the chromosomes is evaluated by a fitness function (FF) [19, 20]. The GA consists of three main steps: mutation, crossover and selection [21]. GAs are used to determine the representation of the chromosomes that are created by three values corresponding to the gains or parameters of the PID controller (K_p, K_i, K_d) that have been modified to attain a desired behavior [22]–[24]. The (K_p, K_i, K_d) gains are real numbers, which are to be measured individually. The equation for the PID controller is shown as (35) [25]. In this study, the integral time absolute error (ITAE) is taken as the objective function, given as (36). The reciprocal of the objective function is called FF. The FF is the measurement of the chromosome's quality.

$$G_c(s) = K_p + \frac{K_i}{s} + K_d s \quad (35)$$

$$ITAE = \int_0^t t \mid e(t) \mid dt \quad (36)$$

Where K_p is the proportional gain, K_i is the integral time, K_d is the derivative time, e (t) is the error-controlling signal = 1− y(t) and y(t) is the tuned control system step response. Figure 4 shows a flowchart for GA. The parameters of the GA are listed in Table 2.

Table 2 Genetic algorithm parameters

No	*Parameter*	*Type / Value*
1	No. of iteration	100
2	Population size	50
3	Encoding	Binary
4	Selection scheme	Stochastic Uniform
5	Crossover probability (P_c)	0.8
6	Crossover type	Single Point
7	Mutation probability (P_m)	0.2
8	Recombination probability (P_r)	0.09
9	Fittness function	ITAE

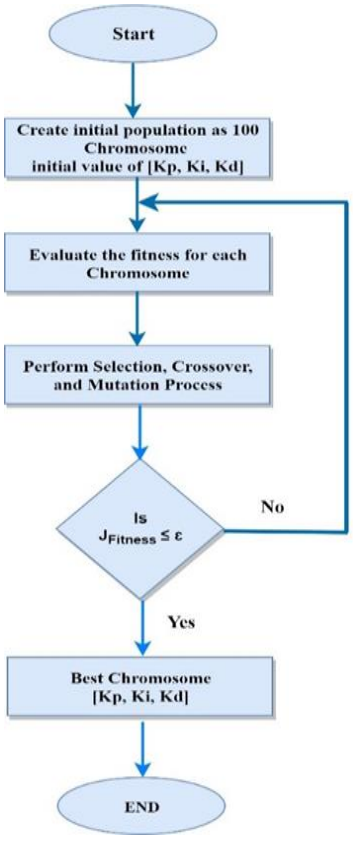


Figure 4. Flowchart for genetic algorithm (GA)

The block diagram for the GA-optimized or tuned PID controller parameters for the SEPIC DC-DC converter can be seen in Figure 5. The reference signal or set point R(s) is input as the desired voltage and is compared with the actual value of the output voltage Y(s) for the SEPIC converter. The error signal E(s) is given as the input signal to the PID controller after its parameters are tuned using GA technique. The output signal generated by the PID controller U(s) is used as the input signal to control the suitable range of duty cycle (D) in a suitable range for the SEPIC converter, and the required output voltage is then obtained [26].

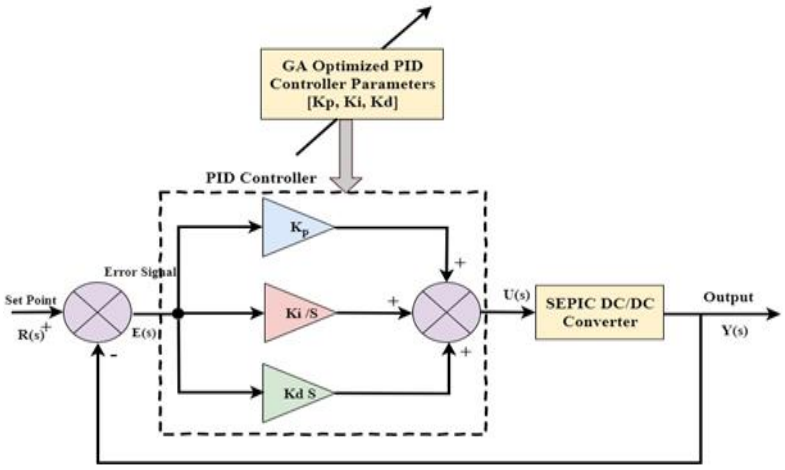
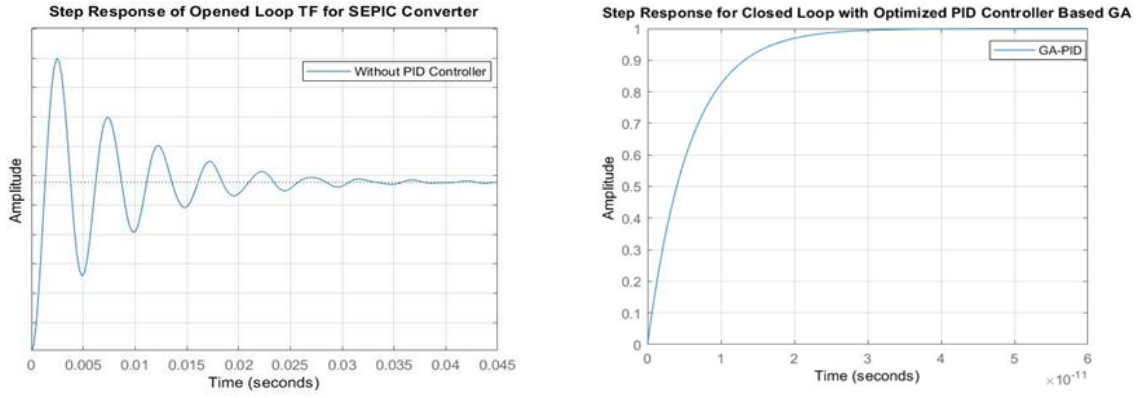


Figure 5. Block diagram of PID controller optimized by GA

3. RESULTS AND DISCUSSION

MATLAB® R2018b Simulink software was used to simulate the SEPIC DC-DC converter and verify its performance. Figure 6 (a) shows the step response of the open-loop transfer function for the SEPIC DC-DC converter without the PID controller. It is observed that the response matches the step response for a second-order system. However, the maximum overshoot percentage (close to 73%) is higher than that of the second-order system. Slow rise and settling times are also observed. Figure 6 (b) depicts the closed-loop step response for a GA optimised PID controller. The PID controller parameters (K_p, K_i, K_d) are set to their optimal value using the GA technique. This technique helps minimise the objective function (ITAE) and the optimisation process depends on the code specified in the MATLAB m-file. Table 3 specifies the optimisation criteria and the performance characteristics for the step response like (M_p, t_r, t_s).



(a) (b)

Figure 6. Simulation results, (a) Step response for SEPIC converter without controller, (b) Step response for SEPIC converter with GA-PID controller

Table 3 Performance Parameters for step response

Performance Parameters	Type of controller	
	Without PID controller	With GA-PID controller
K_p	N/A	69.805
K_i	N/A	290.779
K_d	N/A	339.306
% M_P	73	0
t_r (sec)	8.9246 e-04	1.2610 e-11
t_s (sec)	0.0301	2.2454 e-11
ITAE	N/A	2.7182 e-06

4. CONCLUSION

This paper presents design, modelling and simulation of controlled SEPIC DC-DC converter-based GA. The study comprised the mathematical model, state-space modelling, design components, simulation, and analysis of the SEPIC DC-DC converter. MATLAB R2018b SIMULINK was used to carry out the simulations. The SEPIC DC-DC converter is a time-invariant, linear system of the fourth order. A PID controller was utilised to change the output of the SEPIC converter to optimise the values of the performance parameters. PID controller parameters K_p, K_i, K_d were manipulated using the GA technique to determine their optimal values intelligently. Optimisation was performed with ITAE serving as the fitness function. The results of the simulation and the study indicate that the closed-loop step response system performed best in conjunction with a PID controller with optimised parameters. Maximum overshoot percentage rise and settling times were optimised. Additionally, the GA-PID controller was more accurate and better sensitivity against disturbances when compared to using it without the PID controller.

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