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Induction drive system with DSTATCOM based asymmetric twin converter

P Anusha, B V Rajanna
Department of Electrical and Electronics Engineering, Nalanda Institute of Engineering and Technology, India

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ABSTRACT

High power demands are usually met by advanced power electronics converters in several large utility and electric drives applications. Applications from high power drives commonly uses solution based multi pulse and multilevel converters. A common DC link with atleast one voltage source converter (VSC) working with almost fundamental switching frequency are used in converters of multipulse type, and each output module is connected with the multipulse transformer in series. When compared to that of solution with single-VSC, Several VSCs generating different triggering pulses are adjused in order to achieve current injected with low specified total harmonic distortion (THD) with losses of abridged switching. Huge structure in complexity and expensive cost expenditure of the multipulse transformer is the major limitation of this scheme. DC link split capacitors in addition are eliminated by modifying the topology of the circuit. Thus, the independent voltages of the DC capacitor are controlled and decreased in number and the flow of third harmonic current component in the transformer is eliminated. The scheme of the designed controller is depending on the derived mathematical system model. Simulaion observation is used to check the scheme performance and efficiency in a detailed way with drive control technique.

Corresponding Author:

B V Rajanna,
Department of Electrical and Electronics Engineering,
Nalanda Institute of Engineering and Technology,
Sattenapalli, Guntur-522438, Andhra Pradesh, India.
Email: rajannabv@ngi.ac.in

1. INTRODUCTION

Interconnection of many stations and centres of loads in contemporary power systems are done by the power networks of extended transmission and distribution which are complex in nature. Reliabilty of the power quality need not to be always better even if the reliability of generation of power is good [1]. Customers should get the energy flow with uninterruption with a fine level of sinusoidal voltage magnitude and frequency provided by the distribution system of power. Many loads in the power distribution systems which are particularly non-linear will considerably affect the power quality [2]. The Power Electronics devices eploying techniques of quick controlled force commutation are more useful and effective and mitigation of unfavourable impacts on the PQ in power industries during the past few decades were avoided by conventional means [3]. Compensators in PQ are classified mainly into two types. Prevention of harmonics is done effectively by the first type which is the shunt connected compensation device. The distorted voltages and voltage sags at the system side caused by the faults in the power transmission system are corrected by the second type which is the series connected device, which has an edge over the

shunt type [4], these qualities in quality of power might lead to irregular operations of amenities or even the devices with protection are tripped. Generation or Absorption of Reactive Power Control is done by the use of converters employing technology of FACTS device which is linked in parallel to the system of power known as static synchronous compensator (STATCOM) [5-7]. Injection of Reactive power to the power system makes the STATCOM works in the capacitive mode. A common DC link with atleast one voltage source converter (VSC) working with almost fundamental switching frequency are used in converters of multipulse type, and each output module is connected with the multipulse transformer in series [8-10]. When compared to that of solution with single-VSC, Several VSCs generating different triggering pulses are adjused in order to achieve current injected with low specified THD (total harmonic distortion) with losses of abridged switching. Huge structure in complexity and expensive cost expenditure of the multipulse transformer is the major limitation of this scheme [11-14].

In case of STATCOM with a multilevel converter, there is no source of power or any circuit in DC floating capacitor due to galvanical isolation and should be connected with each of the cascaded H-bridge converters [15]. In diode clamped topology there are eighteen switches controlled with diodes which are antiparallel in addition with eighteen diodes which leads to a greater number of components. This topology can be made with a smaller number of components which consists of 12 controlled switches with antiparallel diodes by the topology as shown in Figure 1 [16]. For simple, easy layout structure and for reducing circuit driver difficulty, Semiconductor switches are replaced by VSCs in this topology [17].

Conversion of AC Power into DC Power requires Power-Electronics technologies with managing skills. The structure and design of Component in the topology of Twin Converter topology is observed [2] which is like topology of open-ended transformer. In order to achieve only three-level operation, VSCs of both are maintained with equal voltages of DC-link in topology of twin converter. To ensure four-level operation with reduced THD with lesser filter requirements of the circuit [18], regulation of voltage at DC-link of VSC-2 made 1/2 of VSC-1 in the open-ended transformer topology that has not been observed in case of topology of three-level twin converter. Series connected capacitors in a string subdivide the single DC bus into number of voltage levels in the diode-clamped inverter topology. For switching each leg of the phase output to some of these levels of voltage [19], matrix of semiconductor switches and diodes are used.

Capacitor bank pairs in each VSC must require the balancing of the voltages, if the open-ended transformer- connected circuit equipped with a split-capacitor arrangement which therefore lead to the regulation of voltages in two pair of DC capacitors. To reduce the third-harmonic and DC current components, a complex controller is required [20].

Only pair of DC links in two VSCs is used without split-capacitor arrangement to overcome this drawback in proposed asymmetric twin converter topology which reduces the THD current components in the grid by choosing the two VSCs DC-link voltages with a convenient ratio [21-32] as shown in Figure 2.

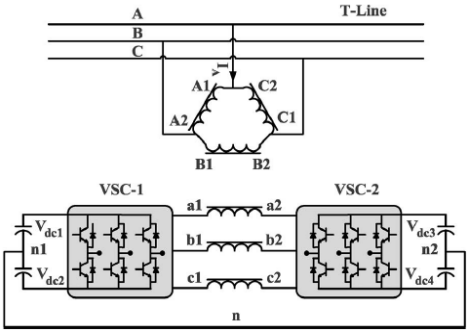

Figure 1. STATCOM having four level connected with an open-ended transformer

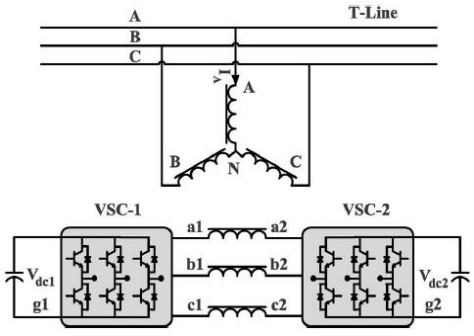

Figure 2. STATCOM with a twin-converter asymmetric topology

2. PROPOSED MULTILEVEL INVERTER TOPOLOGY

2.1. Principle of operation

Pair of VSCs contained in the proposed multilevel asymmetric-twin-converter topology as shown in Figure 2. The pair of 2-level VSCs will have the output voltage difference equal to LV side voltage by connecting differential transformer LV windings among them. Grid having three phases is connected through HV windings set in pattern of star. The STATCOM input filter inductances are governed by the transformers Leakage inductances. The two-level output individually provided by the operation of both VSCs with separate DC links. Transformer LV windings Voltages are expressed in VSCs voltage output as

$$E_a = E_{a1g1} - E_{a2g2} + E_{g1g2}$$
$$E_b = E_{b1g1} - E_{b2g2} + E_{g1g2} \quad (1)$$
$$E_c = E_{c1g1} - E_{c2g2} + E_{g1g2}$$

Where E_a is the LV winding phase-A voltage
E_{a1g1} is the VSC-1 pole voltage
E_{a2g2} is the VSC-2 pole voltage and
E_{g1g2} is the two VSCs terminals negative difference voltage respectively.

The summation of the currents in the LV phase winding will be zero as two VSCs have separate DC links.

$$I_a + I_b + I_c = 0 \quad (2)$$

Also, summation of voltages at particular instant values in grid is 0.

$$V_A + V_B + V_C = 0 \quad (3)$$

Addition of winding voltages at LV side expressed as

$$E_a + E_b + E_c = \frac{N_{LV}}{N_{HV}}(V_A + V_B + V_C) - R(I_a + I_b + I_c) - L\frac{d(I_a+I_b+I_c)}{dt} \quad (4)$$

where *R* is Resistance at LV Winding,
L is the LV Winding Leakage Inductance, *N*LV/*N*HV indicates ratio of turns.

Inserting (2) and (3) in (4) yields

$$E_a + E_b + E_c = 0 \quad (5)$$

Inserting winding voltages at LV side from equation (1) into equation (5) gives

$$E_{g1g2} = -\frac{1}{3}\left(E_{a1g1} - E_{a2g2}\right) - \frac{1}{3}\left(E_{b1g1} - E_{b2g2}\right) - \frac{1}{3}\left(E_{c1g1} - E_{c2g2}\right) \quad (6)$$

Inserting E_{g1g2} value in (1) gives

$$\begin{pmatrix} E_a \\ E_b \\ E_c \end{pmatrix} = \frac{1}{3}\begin{pmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{pmatrix}\begin{pmatrix} E_{a1g1} - E_{a2g2} \\ E_{b1g1} - E_{b2g2} \\ E_{c1g1} - E_{c2g2} \end{pmatrix} \quad (7)$$

The (7) gives the relation between voltages at the LV winding and pole. Based on the state of conduction of swiches in VSC-1 and VSC-2, the voltages occur at Pole are decided. A possible different switches states combination is equal to 2^6 = 64. The performance will be analyzed in a better way by choosing convenient ratio of VSCs DC link voltages, *V DC1: V DC2*=1:0.366 as observed in [24]. With repect to switching of unique states, the voltage plot of space vector is drawn by using proper DC link voltage ratio as shown in Figure 3. States of swiching totally consists of 64. Out of these states of switching, Voltages of the phase which are unique states of switching are 49 and Steps of voltages observed at the voltages of the LV side are 25.

LV side voltages of line are articulated in voltages of pole which gives *Eab*, *Ebc*, and *Eca* by (1)

$$E_{ab} = E_a - E_b = E_{a1g1} - E_{a2g2} - E_{b1g1} + E_{b2g2}$$
$$E_{bc} = E_b - E_c = E_{b1g1} - E_{b2g2} - E_{c1g1} + E_{c2g2}$$
$$E_{ca} = E_c - E_a = E_{c1g1} - E_{c2g2} - E_{a1g1} + E_{a2g2} \quad (8)$$

Voltage waveforms *Eab*, *Ebc* and *Eca* are having 7 different steps like the number of line voltage steps observed in the Diode clamped four level multilevel converter based on the states of switching for *V* DC1 = 2*V* DC2. Waveforms of the line voltages are having nine different steps like the number of line step

voltages observed in Diode clamped four level multilevel converter with ratio of voltage of capacitors having 100(*V* DC1: *V* DC2: *V* DC3) = 33:66:33 for 366*V* DC1 = 1000*V* DC2. Thus, the equivalent proposed scheme of a four-level converter is obtained.

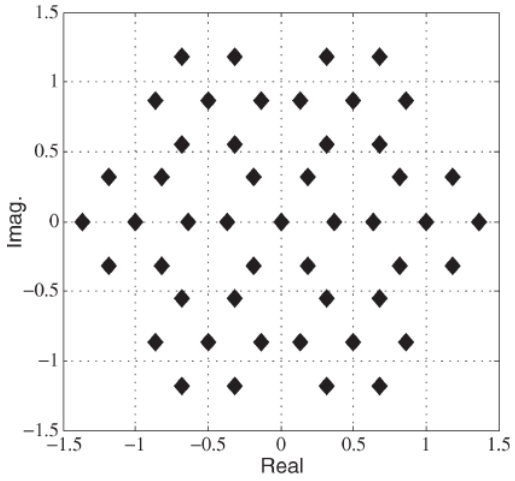

Figure 3. Proposed topology showing Space vector diagram with fourty nine unique states

2.2. PWM Strategy

Based on the 25 switching states given by equation (7), the voltage *Ea* at the LV side takes one of the switching states. The technique of PWM used and waveform of modulation decides the switching state. PWM techniques generally employed in high power applications are carrier-based PWM (CB-PWM) or space vector modulation (SVM) and Selective harmonic elimination method (SHEM). The dynamic response of the SHEM PWM technique is slow and thus its use is limited. Sector identification algorithm is required in the SVM multilevel converter realization. The implementation is multifaceted due to the presence of large number of sectors. Thus, the proposed topology uses the Phase-Shifed (PS) CB-PWM technique. Ouput voltages of *Ea*1*g*1, *Eb*1*g*1, *Ec*1*g*1, *Ea*2*g*2, *Eb*2*g*2, and *Ec*2*g*2 for every inverter are having the individual waveforms of modulation as expected by the controller of this PWM technique employed. States of switching are determined for the corresponding inverter devices by comparing each waveform of modulation with a waveform of carrier which is same as the technique of phase shifted carrier based PWM employed by H-bridge converters of cascaded type [15, 16]. Addition of voltages of individual converter gives resultant ac voltage waveform for two H-bridges per phase.

Thus, the waveforms of carrier are phase-shifted from each other by 180^0 to eliminate the frequency harmonics of carrier. Since the two ac voltages difference gives the resultant waveform, the phase shifting of carrier is not required in case of asymmetric twin converter topology. Modulation waveforms with carrier waveforms comparison for phase-A as shown in Figure 4. The technique of PWM employed in the operation eliminates the low-order harmonics. Harmonics which are dominant are twice the frequency of carrier located at its sideband. The magnitude of carrier sideband frequency is too there but smaller than frequency of carrier.

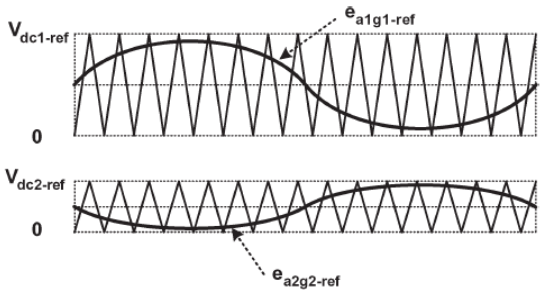

Figure 4. Phase-shifted carrier based PWM technique showing the comparison of modulation waveforms with carrier waveforms

3. PROPOSED STATCOM SYSTEM EQUIVALENT CIRCUIT

An Equivalent circuit is derived for the proposed STATCOM for analysis purpose as shown in Figure 5.

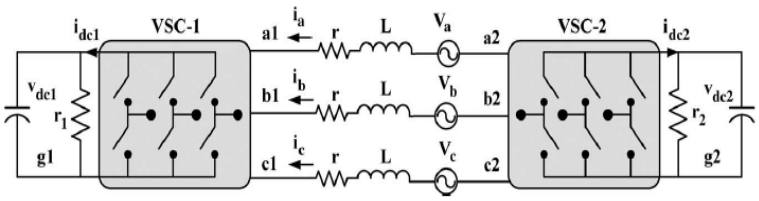

Figure 5. The proposed STATCOM having an equivalent circuit diagram

Sources of Voltage, Resistances and Inductances are used in the combination of series equivalent circuit which represents the transformer. Pair of resistances *R*1 and *R*2 located across pair of DC links for modelling losses in two VSCs. The system proposed has the derived governing equations as

$$S\begin{pmatrix} I_a \\ I_b \\ I_c \end{pmatrix} = \begin{pmatrix} -\frac{R\omega_b}{L} & 0 & 0 \\ 0 & -\frac{R\omega_b}{L} & 0 \\ 0 & 0 & -\frac{R\omega_b}{L} \end{pmatrix}\begin{pmatrix} I_a \\ I_b \\ I_c \end{pmatrix} + \frac{\omega_b}{L}\begin{pmatrix} -E_a + V_a \\ -E_b + V_b \\ -E_c + V_c \end{pmatrix} \quad (9)$$

where *L* is expressed in *ωbl/z*base.
l is the leakage inductance of STATCOM
ωb is base frequency of STATCOM and
and *z*base is impedance of base in STATCOM.

System values for all the variables and parameters are given in per-unit (p.u.). Information in the Appendix is given for *dq*0 reference frame transformation of (9). Frame of *dq*0 has variables of the system given as follows:

$$S\begin{pmatrix} I_d \\ I_q \end{pmatrix} = \begin{pmatrix} -\frac{R\omega_b}{L} & \omega \\ -\omega & -\frac{R\omega_b}{L} \end{pmatrix}\begin{pmatrix} I_d \\ I_q \end{pmatrix} + \frac{\omega_b}{L}\begin{pmatrix} -E_{d1} + E_{d2} + |V| \\ -E_{q1} + E_{q2} \end{pmatrix} \quad (10)$$

where I_d and I_q are *d* and *q*-axis current at side of LV. VSC-1 and VSC-2 are having components of voltages given by (E_{d1}, E_{q1}), (E_{d2}, E_{q2}). The ac parameters of the grid and STATCOM are interrelated by Equation (10). The equations of instantaneous power balance are used for deriving the reliance between the parameters of DC and ac of STATCOM. The condition of balance of power between the DC and ac links of VSC-1are given by the following (11):

$$V_{dc1} I_{dc1} = \frac{3}{2}\left(E_{d1} I_d + E_{q1} I_q\right) \quad (11)$$

The relation between the voltage *V* DC1 and current pssing through DC-link capacitor *c*1 is given as follows:

$$sV_{dc1} = \omega_b C_1 \left(I_{dc1} - \frac{V_{dc1}}{R_1}\right) \quad (12)$$

where *C*1 is expressed as 1*/*(*ωbc*1zbase).

Inserting *I* DC1from (11)

$$sV_{dc1} = \omega_b C_1 \left(\frac{3}{2V_{dc1}}\left(E_{d1} I_d + E_{q1} I_q\right) - \frac{V_{dc1}}{R_1}\right) \quad (13)$$

similarly, VSC-2 has the equation of governing given as

$$sV_{dc2} = \omega_b C_2 \left(\frac{3}{2V_{dc2}} \left(E_{d2} I_d + E_{q2} I_q \right) - \frac{V_{dc2}}{R_2} \right) \quad (14)$$

the system behaviour is given by the (10), (13), and (14).

4. MATLAB MODELING AND RESULTS OF SIMULATION

Three different scenarios are carried out in the simulation, 1). STATCOM of high power employed in planned converter of asymmetric type. 2). STATCOM of high power with control of reactive Power employed in planned converter of asymmetric type. 3). STATCOM of high power with induction machine drive employed in planned converter of asymmetric type.

4.1. STATCOM of high power employed in planned converter of asymmetric type

High Power STATCOM Employed in Asymmetric Twin Converter model in Matlab/Simulink as shown in Figure 6. Phase-A grid voltage at HV-side & Phase-A transformer current at LV-side as shown in Figure 7. Input side voltage of converter which is nothing but the voltages at the primary side to support the Asymmetric Converter with converter operations as shown in Figure 8.

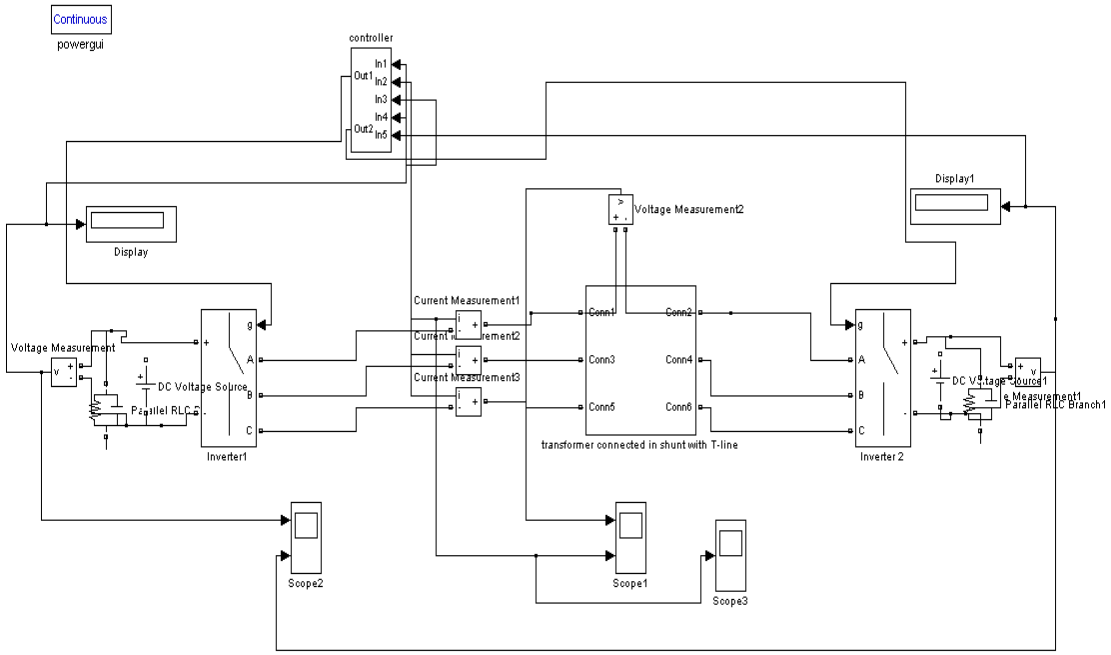

Figure 6. STATCOM of high power employed in converter of asymmetric type model in Matlab/Simulink

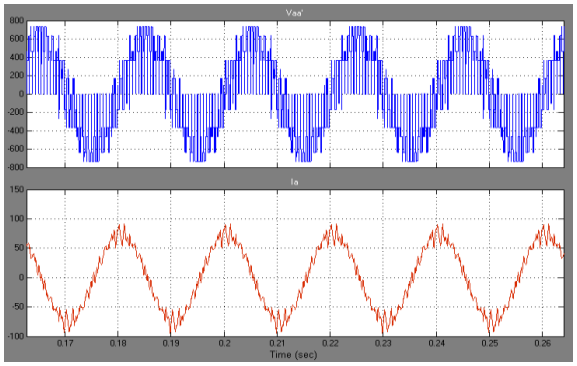

Figure 7. Phase-A grid voltage at HV-side & Phase-A transformer current at LV-side

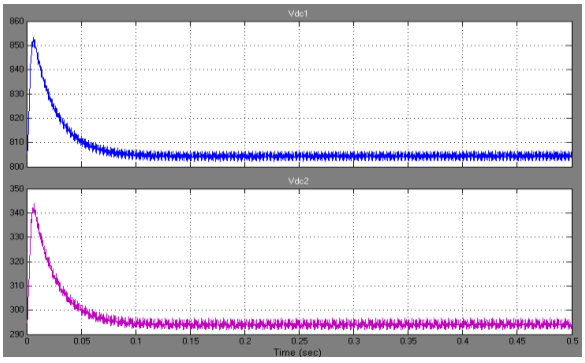

Figure 8. Input side voltage of converter

Analysis of FFT for Phase-A Current at LV Side with Asymmetric Converter is 13.34% as shown in Figure 9. Analysis of FFT for Voltage at the LV Side with Asymmetric Converter is 41.64% as shown in Figure 10.

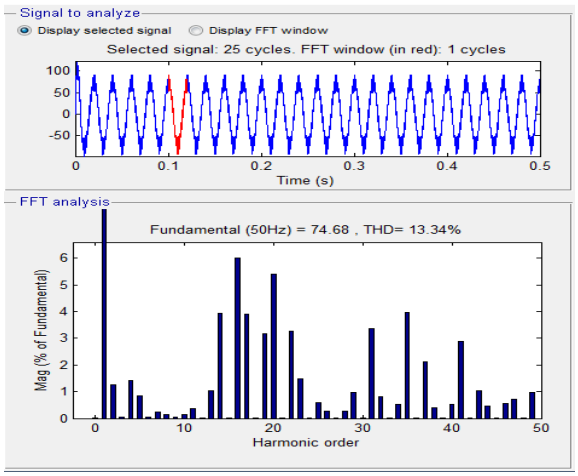

Figure 9. Analysis of FFT for Phase-A Current at LV Side

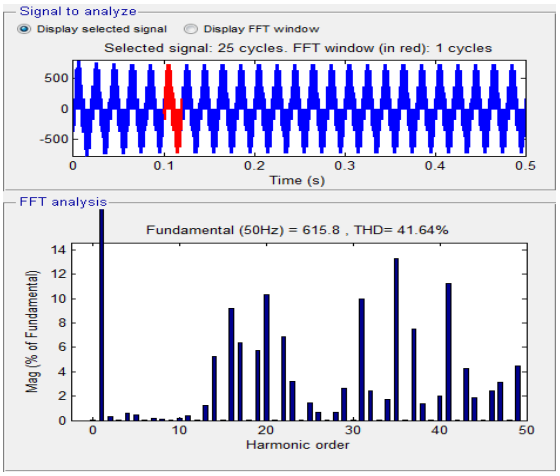

Figure 10. Analysis of FFT in voltage at LV Side

4.2. STATCOM of high power with control of reactive power employed in planned converter of asymmetric type

STATCOM of high power with control of reactive power employed in twin converter of asymmetric type model which has the Phase-A grid voltage at HV-side & Phase-A transformer current at LV-side as shown in Figure 11.

Input side voltage of converter which is nothing but the voltages at the primary side to support the Asymmetric Converter with control of reactive power with converter operations as shown in Figure 12.

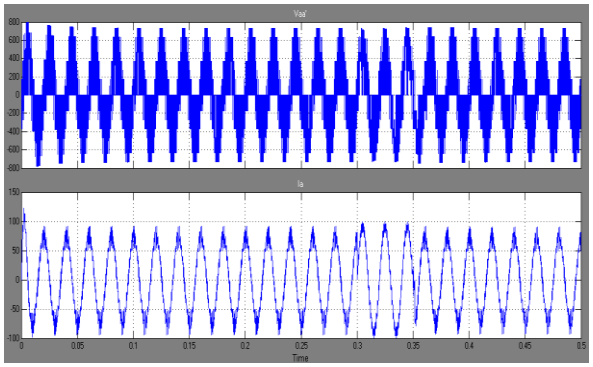

Figure 11. Phase-A grid voltage at HV-side & Phase-A transformer current at LV-side

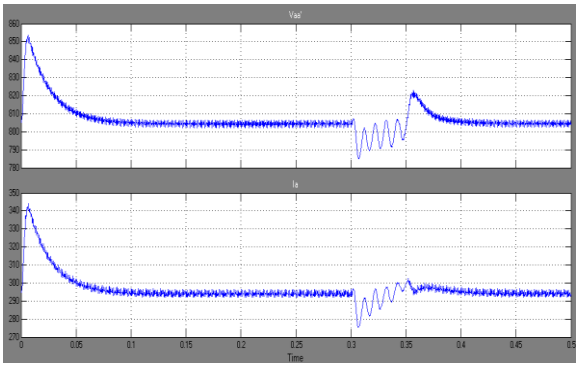

Figure 12. Input side voltage of converter

4.3. STATCOM of high power with induction machine drive employed in planned converter of asymmetric type

The Electromagnetic Torque, Speed and Stator Current of STATCOM of high power with induction machine drive employed in planned converter of asymmetric type as shown in Figure 13.

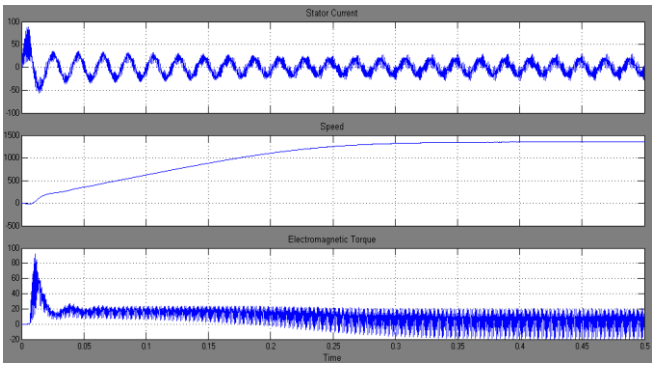

Figure 13. Electromagnetic torque, speed and stator current

5. CONCLUSION

Flexible AC TransmissionSystems *(*FACTS) devices are planned and implemented in systems of power by fast development in power electronics. FACTS devices are utilized for control power flow and enhance system stability. VSCs of two level employed with a high-power STATCOM with control of reactive power is proposed and induction machine drive performance is checked by the proposed system. The control of two DC link voltages of VSCs has been shown in the proposed topology. Also, the low current distortion is achieved by selecting the DC link voltages of the two VSCs with a convenient ratio. DC-link voltage regulation of two converters is done by controller voltage DC-link which is planned for extracting necessary active power of utility thereby transferring the power among pair of converters differentially. Design of planned converter improved in implementing the model in Matlab/Simulink system. Quick and better response and better values of THD are obtained which are well within the Standards of IEEE.

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