

Performance of three-phase three-wire cascaded H-bridge multilevel inverter-based shunt active power filter

Musa Yusup Lada¹, Mohd Amran Mohd Radzi², Jasronita Jasni³, Hashim Hizam⁴,
Auzani Jidin⁵, Syahrul Hisham Mohamad⁶

^{1,5,6}Power Electronic & Drive Laboratory, Center for Robotics and Industrial Automation,
Faculty of Electrical Engineering, Universiti Teknikal Malaysia Melaka (UTeM), Malaysia

^{2,3,4}Advanced Lightning, Power and Energy Research (ALPER) Centre, Faculty of Engineering,
Universiti Putra Malaysia (UPM), Malaysia

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ABSTRACT

Multilevel inverter (MLI) becomes more significant in Active Power Filter (APF) application due to capability to its produce low harmonic output current in which at the same time improving performance of APF. Among the topologies of MLI, Cascaded H-Bridge (CHB) is the most popular topology with less power devices requirement and simple design. MLI CHB is also capable to produce possible output voltage at twice of the number of DC source which in this case of APF is the best suited topology to replace with the conventional six -step inverter. This paper presents the performance of three- phase three-wire CHB MLI used in Shunt Active Power Filter (SAPF) based on Direct Current Control (DCC) and Indirect Current Control (ICC) schemes. Both schemes are developed and verified in MATLAB/Simulink. The simulation results show that both current control algorithms are capable to mitigate load current with Total Harmonic Distortion below than the permissible value based on IEEE 519 standard.

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Corresponding Author:

Musa Yusup Lada,

Faculty of Electrical Engineering,

Universiti Teknikal Malaysia Melaka,

Hang Tuah Jaya, 76100 Durian Tunggal, Melaka, Malaysia.

Email: musayl@utem.edu.my

1. INTRODUCTION

In the state of progression within the power electronic elements within the power system, applications of non-linear load are becoming more and more crucial. As those applications have exponentially increased, this phenomenon will generate a power quality issue in power system caused by the load current that drawing non-sinusoidal current form. The power quality distortion in power system can cause various problems such as high-power losses, extra current flow to neutral line, production of heat and implicit hazardous effect to the sensitive machine [1-6]. In the past decade, passive power filters such as series inductance, shunt capacitor and zigzag three-phase transformer are used to mitigate harmonic distortion at power system. However, those filters cannot work efficiently and furthermore they are unable to mitigate completely low frequency harmonics [7-9, 21-22]. Hence, Active Power Filter (APF) has been introduced to mitigate low and high harmonics distortion in the power system. In conjunction to that, APF can also be used for reactive power compensation, load balancing, voltage regulation and voltage flicker compensation [1, 3, 5, 6, 10, 24].

Multilevel Inverter (MLI) has gained much attention in high power system application due to its advantages such as produce common mode voltage, draw low distortion input current, operate in low and high switching frequency, and can reduce harmonic distortion using selective harmonic elimination technique. As the trend of increasing in research of renewable energy applications, researchers are progressively developing new topologies and algorithms in designing MLI in which the fruits of the research can also be applied in APF by replacing the conventional six-step three-phase inverter as shown in Figure 1(a). The advantage of using MLI compare to conventional six-step inverter is its capability to produce low harmonic output current which at the same time improving the performance of APF [5, 11-15]. Furthermore, MLI can produce high efficiency for fundamental frequency, is capable to work under high switching frequency, and can reduce voltage stresses across switches, which make it to even perform in medium and high voltage application [5, 11-13, 15]. There are three common types of MLI namely Cascaded H-Bridge (CHB), Neutral Point Diode Clamped (NPC) and Flying Capacitor (FC) [11, 12, 14, 15]. Among them, the CHB is the most popular due to its advantages such as less power devices requirement, Simple design and possible to produce output voltage level more than twice the number of DC source. Figure 1(b) shows the topology of CHB MLI in SAPF.

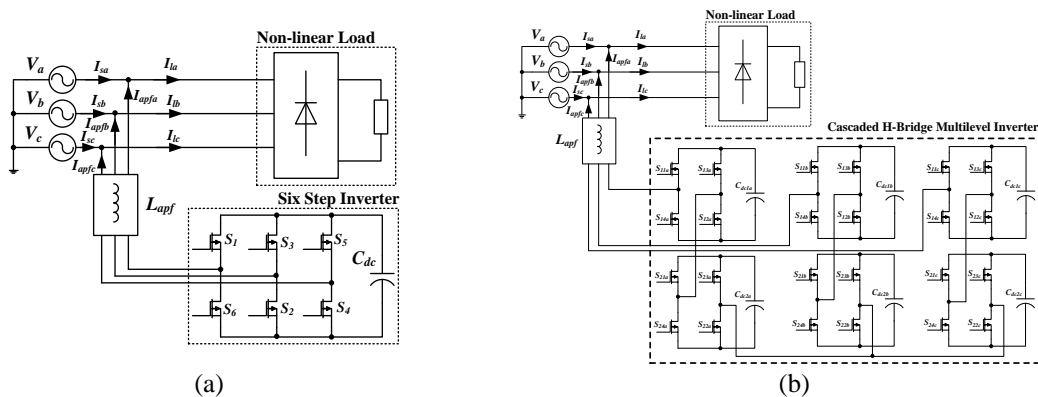


Figure 1. (a) Conventional six-step inverter based SAPF (b) Cascaded H-bridge Multilevel Inverter based SAPF

2. CURRENT CONTROL ALGORITHMS

A current control algorithm is used to generate switching signal for controlling turn ON and OFF switching device. It can be grouped into two major control schemes namely Direct Current Control (DCC) and Indirect Control Current (ICC) algorithms. The DCC algorithm will calculate the current injection reference of APF and compare with the actual current injection of APF as stated in Equation 1. Meanwhile, for ICC algorithm the source current reference needs to be calculated first before comparing it to the actual current source as stated in Equation 2. In term of complexity of the algorithm, ICC is more desirable compared to DCC. ICC uses less mathematical calculation and practically less number of sensors compared to DCC [16-19].

$$e_{current} = I_{APF} - I_{APF,ref} \tag{1}$$

$$e_{current} = I_{s,ref} - I_s \tag{2}$$

3. RESEARCH METHODOLOGY

The effective operation of current control algorithm is depending on instantaneous power theory that used in this simulation. The instantaneous power theory or p-q theory was introduced by Akagi in 1983 and this method uses algebra transformation, which is also known as Clarke transform, to be used in three-phase voltage and current [4, 9, 10, 12, 16]. This theory is the most popular harmonic extraction algorithm, which is usually used for three-phase three-wire SAPF. The illustration of this algorithm is shown in Figure 2, where *p* is instantaneous total energy flow per unit of time and *q* is energy exchanged between the phases without transferring energy.

The modification of filtering for the instantaneous parameter is done by replacing the conventional Low Pass Filter (LPF) or High Pass Filter (HPF) with a new filtering technique called as Self Turning Filter

(STF). This modification will improve the SAPF to work in more decent way of performing filtering in transient or steady state condition of the system [17, 18, 20, 23, 25]. The detailed principle of STF is described in Figure 3.

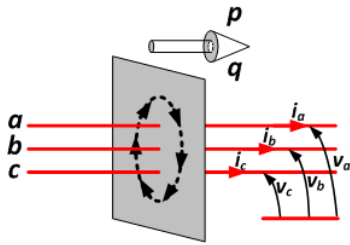


Figure 2. Instantaneous power theory

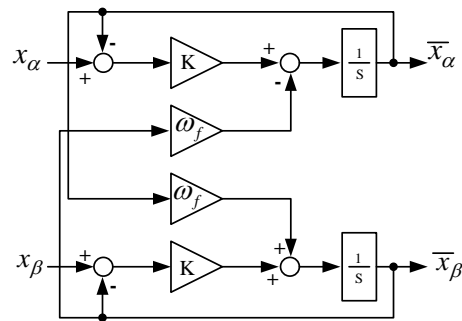


Figure 3. Self tuning filter (STF)

In mathematical equation, STF can be elaborated in Equations 3 and 4, where x_α and x_β are the input signals, \bar{x}_α and \bar{x}_β are the output filtering signals, K is the selectivity parameter, and ω_f is the fundamental pulsation. Since, the fundamental frequency is 50 Hz, the value of ω_f is set to 100π rad/sec and the value of K is set to 100 in order to decrease the STF selectivity process by mean to extract the fundamental component from the voltage or current signal that was distorted without phase delay and amplitude changing. This is because the smaller value of K will increase the filter selectivity in STF.

$$\bar{x}_\alpha = \frac{1}{s} [K(x_\alpha - \bar{x}_\alpha) - \omega_f \bar{x}_\beta] \tag{3}$$

$$\bar{x}_\beta = \frac{1}{s} [K(x_\beta - \bar{x}_\beta) + \omega_f \bar{x}_\alpha] \tag{4}$$

CHB MLI SAPF for three-phase three wire system uses six DC-link capacitors. DC-link capacitor regulation with PI controller is used to control each of DC-link capacitors connected in each of H-Bridge inverters. The values of K_p and K_i are set to 0.8 and 8, so that the transient and steady state voltage drops in each of capacitor can be controlled above than the reference value of average DC-link voltage. The easy way to get the actual DC-link capacitor voltage is by determining the average voltage as stated in Equation 5.

$$V_{dc,ave} = \frac{\sum_n V_{dcn}}{n} \quad n = 6 \tag{5}$$

3.1. Modification of direct current control algorithm

Figure 4 shows the modification of DCC algorithm for CHB MLI based SAPF. The load current and source voltage are transformed into $\alpha\beta$ axis as stated in Equations 6 and 7 respectively. Since the system only involves three-phase three-wire system, the zero sequence can be neglected.

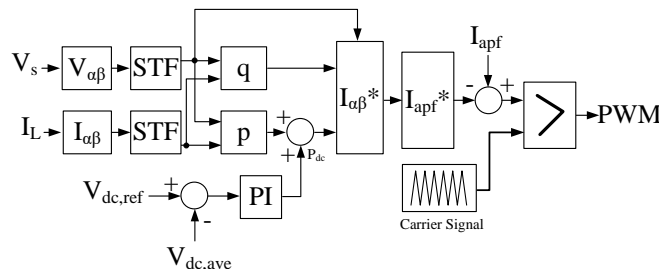


Figure 4. Modification of DCC algorithm for CHB MLI based SAPF

$$[V_{\alpha\beta}] = \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} [V_{abc}] \tag{6}$$

$$[I_{\alpha\beta}] = \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} [I_{abc}] \tag{7}$$

STF is used to filter $\alpha\beta$ axis for current and voltage to suppress harmonic component so that only fundamental component remains for computing instantaneous real power p and instantaneous reactive power q as stated in Equations 8 and 9.

$$p = i_{\alpha}v_{\alpha} + i_{\beta}v_{\beta} \tag{8}$$

$$q = i_{\beta}v_{\alpha} - i_{\alpha}v_{\beta} \tag{9}$$

From Equations 8 and 9, the reference current $\alpha\beta$ can be calculated as stated in Equation 10 before transforming it into active filter current reference as stated in Equation 11.

$$\begin{bmatrix} i_{apf,\alpha} \\ i_{apf,\beta} \end{bmatrix} = \frac{1}{v_{\alpha}^2 + v_{\beta}^2} \begin{bmatrix} v_{\alpha} & v_{-\beta} \\ v_{\beta} & v_{\alpha} \end{bmatrix} \begin{bmatrix} p + p_{dc} \\ q \end{bmatrix} \tag{10}$$

$$\begin{bmatrix} i_{apf,a} \\ i_{apf,b} \\ i_{apf,c} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ 1/2 & \sqrt{3}/2 \\ 1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_{apf,\alpha} \\ i_{apf,\beta} \end{bmatrix} \tag{11}$$

The DCC algorithm produces error current as stated early in Equation 1 and to be compared with the carrier signal. The comparison process used in this system is SPWM bipolar technique which is the error signal will be compared with four different signals that produce different PWM signal to create different levels of output voltage. The SPWM bipolar switching technique is shown in Figure 5.

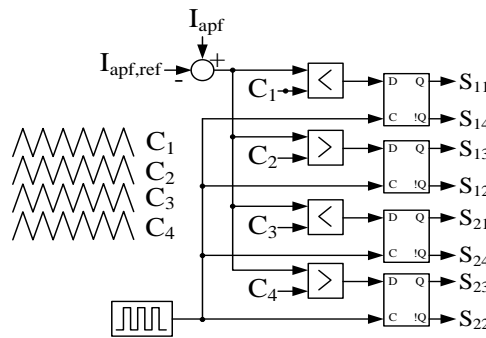


Figure 5. SPWM bipolar switching technique

3.2. Modification of Indirect Current Control algorithm

Figure 6 shows the modification of ICC algorithm for CHB MLI based SAPF. Most of the equations used in DCC algorithm are used in ICC algorithm. The only difference of using ICC over DCC algorithm is it only uses single STF for filtering $\alpha\beta$ voltage compare to DCC used two STF for filtering $\alpha\beta$ voltage and current. Other than that, ICC used current source for error computing as stated in (1).

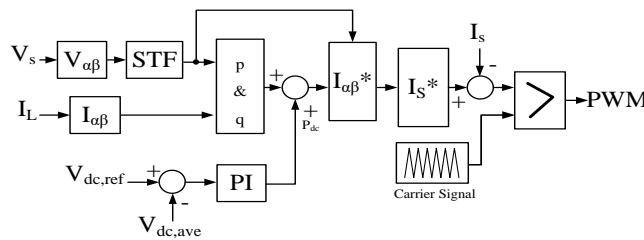


Figure 6. Modification of ICC algorithm for CHB MLI based SAPF

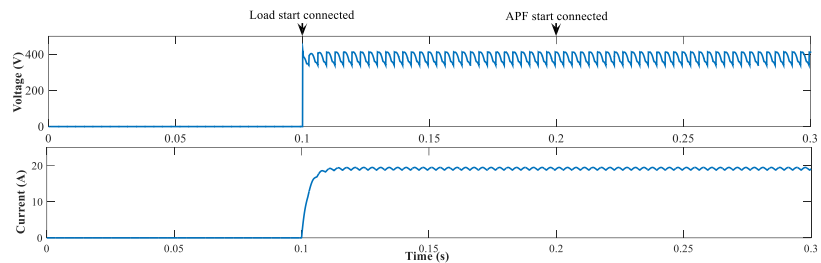
4. SIMULATION RESULT AND ANALYSIS

Simulation model for both algorithms is carried out using MATLAB/Simulink tools. Both of DCC and ICC simulation algorithms use same parameters as listed in Table 1.

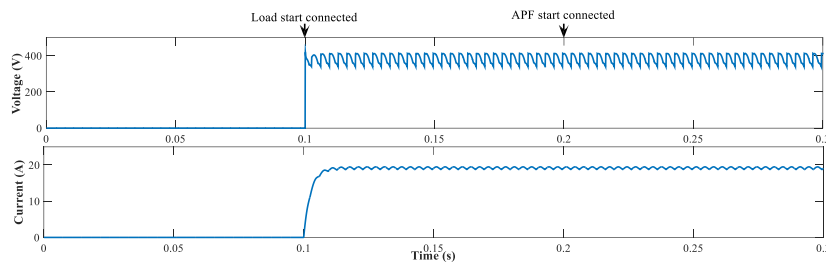
Figure 7 shows the non-linear voltage and current which are produced by combination of three-phase rectifier and RL load as stated early in Table 1. Based on this result, both algorithms produce similar pattern of voltage and current waveforms due to use of same value of non-linear load. The voltage and current at non-linear load also remain the same pattern before and after the APF is connect to the system. The results prove that the APF does not affect or disturb the performance of voltage and current at the non-linear load while sudden injection of the APF current to the system.

Table 1. Parameters of SAPF

Parameter	Value
Voltage source per phase	240 V _p 50 Hz
Smoothing Inductor, I_{apf}	2 mH
Capacitor Link, C_{dc}	3300 μ F 400V
Line Inductor, I_l	2 mH
Switching frequency	25 kHz
Non-linear load	Rectifier + 20 Ω 50mH



(a)



(b)

Figure 7. Non-linear load current and voltage for (a) DCC and (b) ICC algorithms

Figure 8 shows the three-phase source current, load current and active filter current for both DCC and ICC algorithms. The waveform shows the condition for both of DCC and ICC algorithms before and after connected to the APF. The clear detail of this changing condition shown in Figure 9, where only show the source current, load current, active filter current and active filter voltage at phase A for both DCC and ICC algorithms. The used of STF in this simulation prove that under transient condition which between in transition before and after connected to the APF, immediately the load current been mitigated to produced less harmonics in line current. Line current start to change into the sinusoidal waveform after the APF connected to the system. Since the system used MLI, the active filter voltage shows the staircase seven-level voltage for both algorithm DCC and ICC.

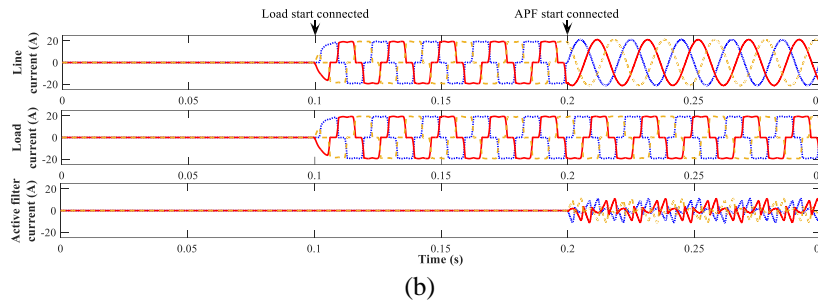
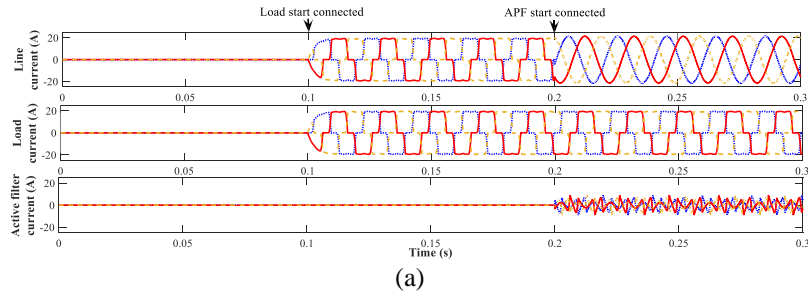


Figure 8. Three phase source current, load current and active filter current for (a) DCC and (b) ICC algorithms

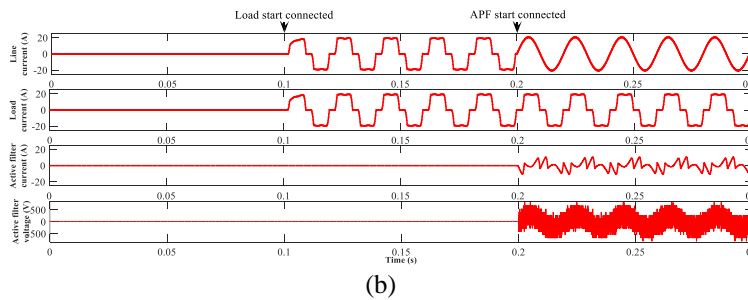
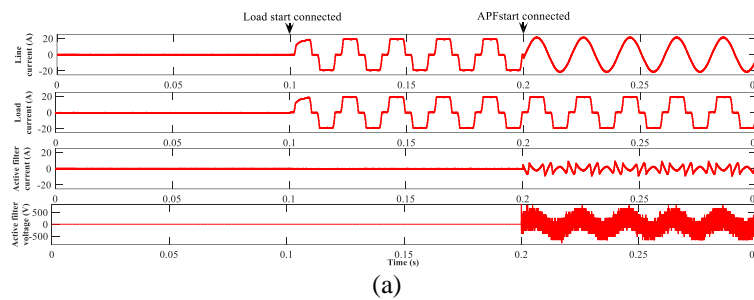


Figure 9. Source current, load current, active filter current and active filter voltage at Phase A for (a) DCC and (b) ICC algorithms

The total harmonic distortion load (THD) current spectrums at phase A for both DCC and ICC algorithms are shown in Figure 10. Since both DCC and ICC algorithms use the same value of non-linear load, the THDs of load current at all phases for both algorithms produce the same value of THD, which is 23.89%.

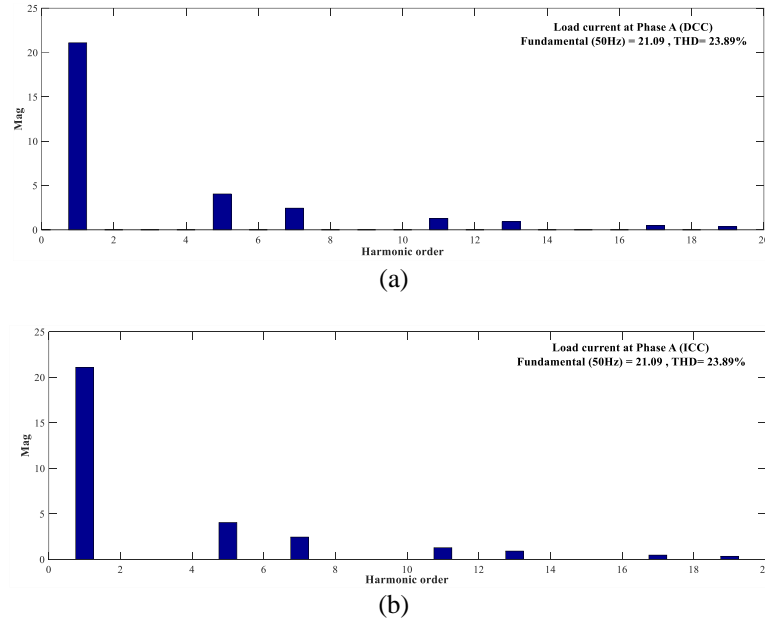


Figure 10. THD load current spectrums at phase A for (a) DCC and (b) ICC algorithms

Both DCC and ICC algorithms perform well in reducing the THD of load current so that the line current can produce less percentage value of THD and at the same time comply with 5% of THD in IEEE 519 Standard. Figure 11 shows the THD line current spectrums at phase A for both DCC and ICC algorithms. The THD value of line current at phase A for DCC algorithm is 1.00%, and meanwhile for ICC algorithm is 0.53%, which is less than DCC algorithm. The summary of THD values for load current and line current are listed in Table 2. Based on this result, ICC algorithm has a good performance in mitigation compared to DCC algorithm. In term of percentage reduction, DCC algorithm mitigates 95.8% of load current, and meanwhile ICC algorithm mitigates 97.8% of load current, which is higher than DCC algorithm.

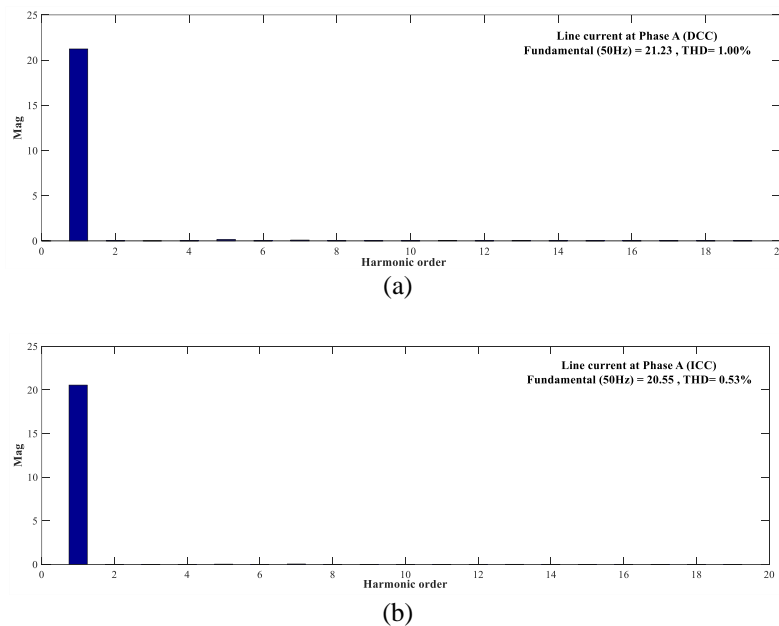


Figure 11. THD line current spectrums at phase A for (a) DCC and (b) ICC algorithms

Table 2. THDs of load and line current for both algorithms

Phase	DCC algorithms		ICC algorithms	
	Load (%)	Line (%)	Load (%)	Line (%)
Phase A	23.89	1.00	23.89	0.53
Phase B	23.89	1.00	23.89	0.53
Phase C	23.89	1.00	23.89	0.53

The real powers at source and load are shown in Figure 12 for both DCC and ICC algorithms. The result shows that, real power load at source has less ripple percentage as compared to load after the APFs start to perform in the system. This condition also happens to the reactive power at source and load for both DCC and ICC algorithms, as shown in Figure 13.

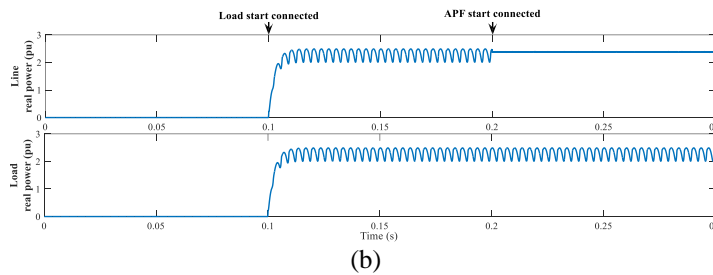
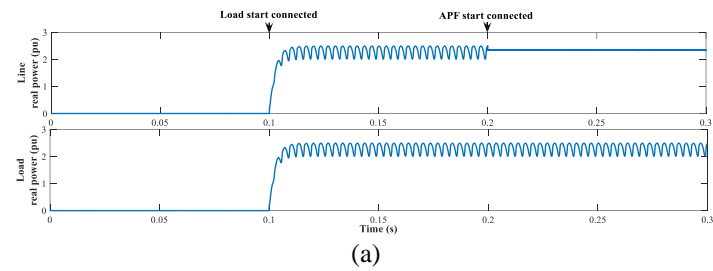


Figure 12. Real powers at source and load for (a) DCC and (b) ICC algorithms

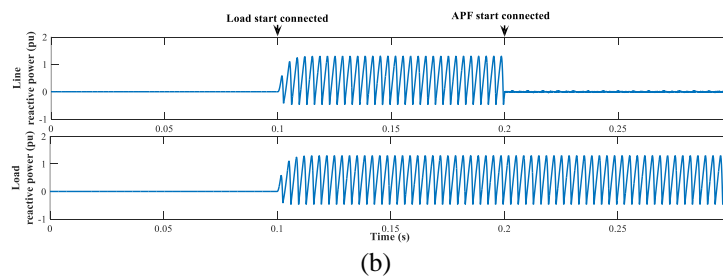
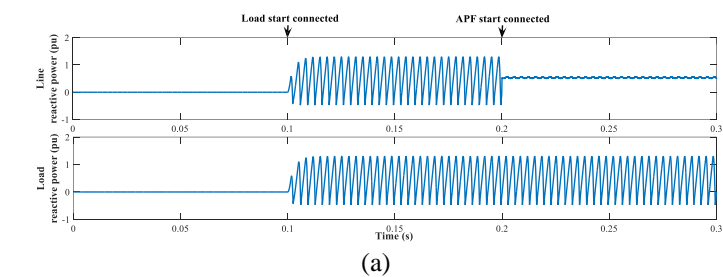


Figure 13. Reactive powers at source and load for (a) DCC and (b) ICC algorithms

Figure 14 shows the DC link capacitor voltages for each of capacitors connected to the CHB MLI. The PI controller will make sure that each of DC-link voltages are constantly at 400V and this will ensure that the CHB MLI work as APF by injecting the APF current to system. If the DC link voltages drop below than 400V the CHB MLI will not work as APF.

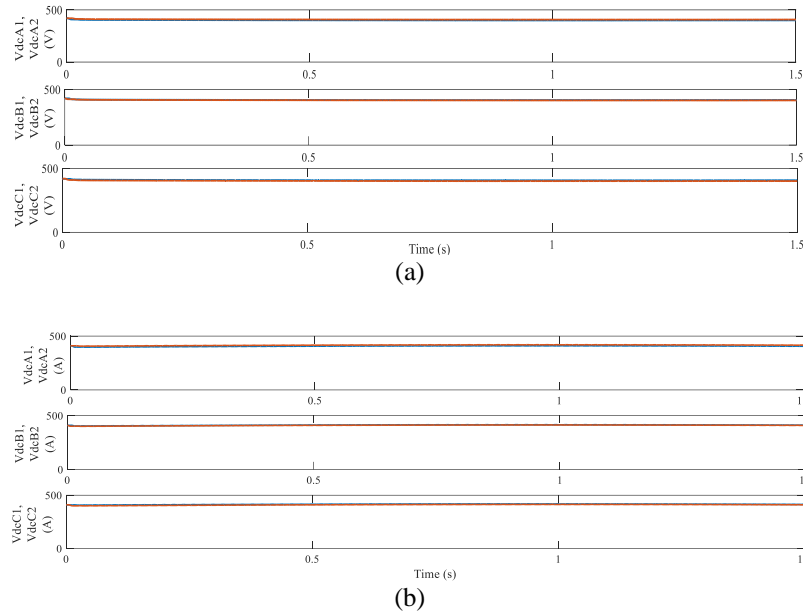


Figure 14: DC link capacitor voltage at Phase A, Phase B and Phase C for (a) DCC and (b) ICC algorithms

5. CONCLUSION

Based on the simulation result, both algorithms have performed well in mitigating the load current so that THD of line current reduces below than permissible value of IEEE 519 Standard, which is 5%. Modification of ICC and DCC algorithms by replacing the conventional low pass filter with STF shows that the line current waveform in each phase managed to immediately improve in transient and steady state condition, where the line current does not take long to become purely sinusoidal current and the waveform is constantly at the same amplitude. The key advantage of ICC algorithm with less calculation involved has made less THD of line current is obtained over DCC algorithm.

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BIOGRAPHIES OF AUTHORS

Musa Yusup Lada was born in Sabah, Malaysia, in 1984. He received his B.Eng. degree and M.Sc. in Power Electronics and Drive from the Universiti Teknikal Malaysia Melaka (UTeM) in 2008 and 2013, respectively. He is presently working towards his Ph.D. degree in Electrical Power Engineering in the Department of Electrical and Electronic Engineering, Faculty of Engineering, Universiti Putra Malaysia. His current research interests include power electronics converter, power quality, and renewable energy.



Mohd Amran Mohd Radzi was born in Kuala Lumpur, Malaysia, in 1978. He received his B.Eng. (Hons.) degree in Electrical and Electronics Engineering and his M.S. degree in Electrical Power Engineering from the Universiti Putra Malaysia (UPM), Serdang, Selangor, Malaysia, in 2000 and 2002, respectively; and his Ph.D. degree in Power Electronics from the University of Malaya (UM), Kuala Lumpur, Malaysia, in 2010. He is presently working as an Associate Professor in the Department of Electrical and Electronic Engineering, Faculty of Engineering, Universiti Putra Malaysia. His current research interests include power electronics, power quality, and renewable energy.



Jasronita Jasni received B. Eng degree in Electrical Engineering (1998) and M. Eng. in Electrical Engineering (2001) from Universiti Teknologi Malaysia. She received the PhD degree in Electrical Power Engineering from Universiti Putra Malaysia in 2010. Currently she is an Associate Professor in the Department of Electrical and Electronic Engineering, Universiti Putra Malaysia, Malaysia. She is an IEEE member. Her research interests include power system analysis for static and dynamics, load flow analysis, embedded generation and renewable energy.



Hashim Hizam graduated with a B.Sc. and M.Sc. in Electrical and Electronic Engineering from Polytechnic University, Brooklyn, New York in 1993 and 1994, respectively. In 2004, he obtained his Ph.D. from Queen University Belfast, Northern Ireland in the UK. He is now an Associate Professor at the Department of Electrical and Electronic Engineering, Faculty of Engineering, Universiti Putra Malaysia. His areas of research are in Power System Protection and Power System Analysis. He also a member of the IEEE.



Auzani Jidin received the B.Eng., M.Eng., and Ph.D. degrees in power electronics and drives from Universiti Teknologi Malaysia (UTM), Malaysia, in 2002, 2004, and 2011, respectively. He is currently a Senior Lecturer with the Department of Power Electronics and Drives, Faculty of Electrical Engineering, Universiti Teknikal Malaysia Melaka (UTeM), Malaysia. His research interests include the field of power electronics, motor drive systems, FPGA, and DSP applications.



Syahrul Hisham Bin Mohamad received his Bachelor Degree in Electrical and Electronics Engineering from Universiti Tenaga Nasional (UNITEN) in 2003 and Master of Engineering from Universiti Teknologi Malaysia (UTM) in 2013. He is currently working towards his Ph.D. degree in Electrical Power Engineering in the Department of Electrical and Electronic Engineering, Faculty of Engineering, Universiti Putra Malaysia. His current research interests include power electronics converter, power quality, and artificial intelligent.