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Implementation of SVM for five-level cascaded H-bridge multilevel inverters utilizing FPGA

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Article Info

ABSTRACT

The Space Vector Modulation SVM technique has won large acceptance for AC drive applications. However the utilization of multilevel inverters connected with SVM by Digital signal processor (DSP) raise the intricacy of control algorithm or computational load, increases of the obtaining distortions output voltage. The development of SVM in multilevel inverters may offer higher numbers of switching vectors for acquiring further enhancements of output voltage performances and implement by using Field Programmer Gate Array (FPGA), investigate lower Total Hormonic Distortion (THD). This paper reports the performance evaluation of SVM for five-level of Cascaded H-Bridge Multilevel Inverter CHMI using MATLAB/Simulink, which is sampled at the minimum sampling time, i.e. DT = 5 μs. The switching signals for driving insulated gate bipolar transistor (IGBTs) which are stored in MATLAB workspaces, are then used to be programmed in FPGA using a Quartus II software. Which can be stated the lower THD of the simulation result is about 14.48% for five-level CHMI and experiment result is about 14.31% for five-level CHMI at modulation index M_i=0.9. The error percentage between the simulation results and experimental results of the fundamental output voltage in SVM is small which is approximately less than 1 %.

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1.   INTRODUCTION

Many AC drive applications utilize Voltage Source Inverters (VSI) which have evolved as the most popular power conversion. The involvement of VSI is in line with the development of various Pulse Width Modulation (PWM) algorithms supported by the advent of solid-state switching device technologies, fast digital signal processors, Field Programmable Gate Arrays (FPGA) in order to create a PWM signal for the real-time and microcontroller system as means of a digital processing. Since a few decades ago, several PWM algorithms have been developed to improve some performances of VSI such as high-power efficiency [1–5]. Few studies indicated that they are not accounted for PWM control with high frequency and diversified techniques of sampling, produce greater output voltage with optimum fundamental value, keep total harmonic distortion (THD) lower within the critical range with lower ratio of switching frequency to fundamental frequency [6]. Apparently, the research about VSI, thus far, has not reached to the state of saturation, as novel or simplified PWM methods are still emerging for various topology inverter circuits and multilevel inverters [7]. Through various types of modulation strategies or PWM methods, a Space Vector

Modulation (SVM) technique has gained wide acceptance because of several advantages such as higher output voltages, lower THD, high-efficiency and flexibility to be implemented in vector control systems [8]–[13]. Besides that, this modulation scheme also offers in optimizing the used of dc voltage link utilization which means it can increase the ration of output magnitude voltage. In general, the implementation of SVM involve with the used of DSP board and required sector identification which brings into the formations of rotating space vector diagram. In the three phases system, there are six fractions in the space vector diagram spinning 360° which each has equally divided by 60°. This space vector diagram is a transformation from a balance of three phase quantities into two phase system of α-β reference frame. The SVM main operation is to use the nearest three vector recognition of the reference voltage and determined the corresponding on-time using the principles of volt second equivalent [14-17].

A multilevel inverter offers greater number of voltage vectors as compared to eight vectors for a two-level inverter. Figure 1 illustrates the space vector diagrams for Sector I, in a two-level inverter and three-level inverter. The space vector diagrams can be used to compare the implementation of SVM in two-level and three-level inverters. As compared to two-level space vector diagram, the sector in three-level inverter is divided into four identical smaller triangles (i.e. Δ_0, Δ_1, Δ_2 and Δ_3). To reduce THD (or dv/dt) and switching losses in multilevel inverter (i.e. three-level), it is necessary to switching vectors which are the nearest to the reference vector $\bar{v}\_s^*$. Hence, three-level SVM switch the vectors $\bar{v}\_2$, $\bar{v}\_7$ and $\bar{v}\_{14}$for a given reference vector. The calculation of on-duration in multilevel SVM is quite complicated and different for various triangles due to small triangles in the space vector diagram of three-level inverter in Fig.1 do not exactly imitate the geometry of a sector of two-level inverter. In two-level SVM, the calculation of on-duration is straightforward which is valid for every sector. However, the three-level SVM needs to modify the reference vector with new origin point to apply the two-level based SVM for calculating on-duration. As shown by Figure 1 (b), the modified reference vector $\bar{v}\_s^*$ with vector $\bar{v}\_2$ as origin point is determined such that the calculation of on-duration is like that of two-level based SVM. The calculation becomes complicated if the reference voltage vector $\bar{v}\_s^*$ lies in triangle Δ_2, where the orientation of triangle is different among others; as can be seen the triangles Δ_0, Δ_1 and Δ_3 have the same orientation with a single triangle or Sector I in two-level SVM, as shown in Fig.1. The complexity increases as number of levels of inverter becomes higher, e.g. in five-level inverter, there are six triangles among sixteen triangles, that have different orientation
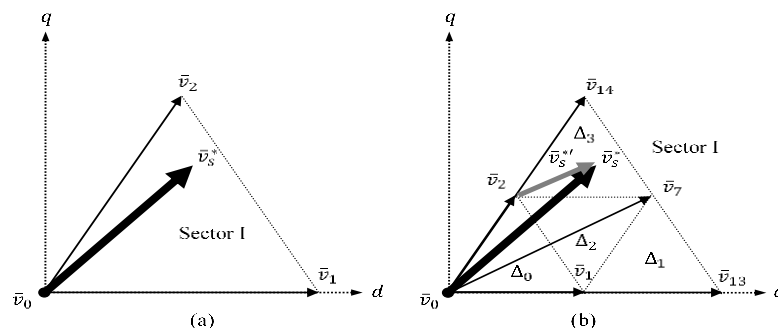

Figure 1. Comparison between (a) two-level space vector diagram and (b) three-level space vector diagram, e.g. for sector i

The implementation of SVM for multilevel inverters require some important parts which are as follows; (1) detection of sector si, (9) detection of triangle Δ_j, (10) calculation of on-duration for switching the nearest vectors, and (11) determination the switching sequence for every switching period. As found in literature, there are two common methods to calculate the on-durations. The first method is to detect the triangle and solve three simultaneous equations of the triangle to determine the on-times as suggested in [18]. The second method is to detect the triangle and use on-duration equations stored in a lookup table for this triangle, as proposed in [19, 20]. Both methods however require complex computations as the number of level increases. Alternatively, the calculation of on-duration can be obtained using general algorithms. Specifically, uses a Euclidean vector system with several matrix transformation, provided that it does not provide a systematic approach for real time SVM implementation. On the other way, calculated on-duration and obtained switching states by means of coordinate system, where the axes are 60 degrees apart. However, the 60 degrees transformation leads to the complexity since the voltage reference is commonly defined in the orthogonal coordinate system. Recently, a simple SVM algorithm for multilevel inverters based on

standard two-level SVM. The two-level based SVM concept is initiated by [21], however, the calculation of on-duration is based on origin modification and 60 degrees coordinate transformation, which cannot be extended in implementing SVM for higher levels, i.e. L greater than three. Unlike the former methods, the implementation of SVM that includes the detection of sector and triangle, and calculation of on-duration were derived geometrically and systematically which suitable for any level of inverter [22-24].

2.   RESEARCH METHOD

Based on the investigation in literature review about type of PWM, the SVM is preferable as it offers several advantages and recently known as the most popular technique for many electrical drive applications. This chapter discusses the development of space vector modulation (SVM) algorithm based on five-level cascaded H-bridge multilevel inverters as proposed by [18, 25]. It is necessary to describe the principle or formulation of the SVM algorithm with the aid of suitable diagrams and equations for every level of inverter is given to develop a proper modulator for evaluating its performances THD. The performances evaluation will be presented in results and discussion. Then, the simulation model of SVM for every level of inverter is developed using MATLAB-Simulink. The development of the simulation model uses same parameters values, e.g. sampling time, three-phase load, DC voltage, etc., as implemented in the hardware system. The verification and evaluation are also carried out via experimental. In the hardware system, the SVM algorithm is executed using a Field Programmable Gate Arrays (FPGA) DEO Controller. The implementation of the hardware system emphasizes on some important aspects for proper SVM operations, providing a blanking time generator to avoid short circuit conditions, ensuring the DC voltage supply for each H-Bridge inverter circuit has provides isolation and a constant DC voltage and applying gate driver circuits which have sufficient power amplifications and isolation to switch ON/OFF the IGBTs of VSI. Once the simulation and experimental results are obtained, all the recorded data is tabulated in tables, and graphs for comparison to performance evaluation. Then, based on suitable equations and theories, the analysis of performances is carried out to verify the improvements/advantages of using different type of levels of inverters which is five-level cascaded H-Bridge multilevel inverters. The development of hardware is used to obtain the experimental results which will be compared with the simulation results, validation of SVM algorithm as well as the advantages of SVM in multilevel inverters.

2.1.   Space vector modulation of five-level cascaded H-bridge multilevel inverter

This section briefly describes the principle of SVM for five-level CHMI based on two-level SVM. Since the SVM control algorithm is based on two-level SVM, it can be proven that most parts utilize same equations and approaches for implementing the switching modulations. Figure 2 depicts a five-level Cascaded H-Bridge Multilevel Inverter (CHMI) which consists of six isolated DC voltages. The CHMI shown in Figure 2 is referred to five-level inverter is due to the fact that the inverter can produce five levels of output voltages, which are $2V_{dc5}$, V_{dc5}, 0, $-V_{dc5}$ and $-2V_{dc5}$. The five output voltages can be obtained by providing possible switching state combinations on the simplified circuit of the five-level CHMI (i.e. for a single-phase) given in Figure 2. Hence a single-phase output voltage of the CHMI (i.e. x-phase where $x = a$-, b-, or c-phase) can be expressed as:

$$v_{xn} = (S_{x1} - S_{x2}).V_{dc5} + (S_{x3} - S_{x4}).V_{dc5} \tag{1}$$

The triangle for five-level CHMI as shown in Figure 4 is defined using (2) and (3). It can be shown that each sector will have 16 triangles (i.e. $\Delta_0, \Delta_1, \Delta_2,\ldots, \Delta_{15}$).

$$\Delta_j = k_1{}^2 + 2k_2 \tag{2}$$
$$\Delta_j = k_1{}^2 + 2k_2 + 1 \tag{3}$$

The discussion above shows the different parts utilized in five-level CHMI as compared to that of three-level, where the five-level CHMI involves greater numbers of triangles, level output voltages and voltage vectors. The rest parts will utilize same approaches and equations. For example, the on durations for switching vectors in five-level CHMI are calculated using (4), (5) and (6).

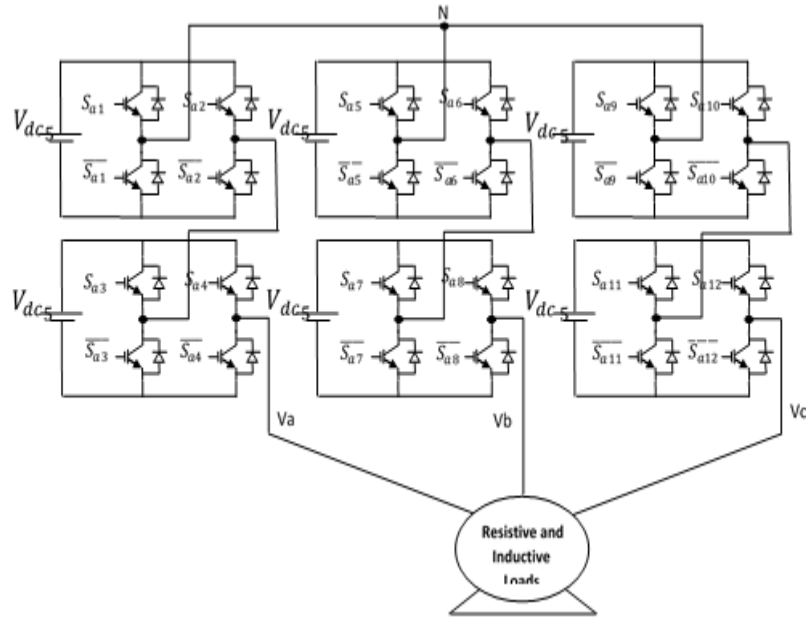$$t_{ao} = \frac{3T}{2V_{dc5}}\left(v_{\alpha o}{}^* - \frac{1}{\sqrt{3}}v_{\beta o}{}^*\right) \tag{4}$$

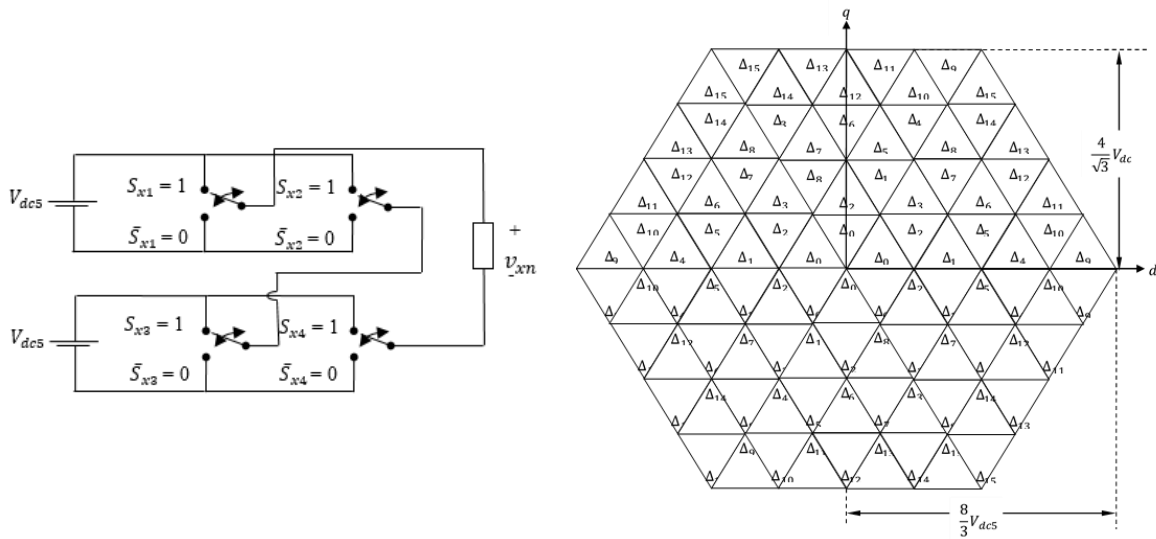Figure 2. The circuit of five-level CHMI

Figure 3. Simplified five-level H-bridge inverter
(for any Phase)

Figure 4. Definition of triangle ($\Delta_j = \Delta_0, \Delta_1, \Delta_2, \ldots,$
Δ_{15}) for every sector

2.2. Simulation model of space vector modulation

This section presents a simulation model of Space Vector Modulation (SVM) using MATLAB-Simulink. Figure 5 depicts the simulation model, specifically the control algorithm of SVM which generates switching status. The simulation model shown in this figure is used to generate switching states for driving IGBTs of five-level CHMI by modifying the number of inputs and DC voltage terms in some calculations. The simulation is performed using two sets of sampling times, such as $DT_1 = 200 \, \mu s$ for detecting sectors, triangles and computing on-duration, and $DT_2 = 5 \mu s$ for generating appropriate pulse width with highlinearity and accuracy. Generally, the simulation model is constructed using two types of programming approaches, namely the graphical programming approach using Simulink blocks and the c-programming approach written in MATLAB function blocks. There are two inputs required in the simulation model which are the demands of magnitude and frequency. These two inputs will produce a reference of three-phase

voltage. The Simulink blocks inside the Subsystem1 for generating the reference of three-phase are presented in Figure 6. It can be seen that the reference is constructed using (7).

$$v_a^* = A.sin(2\pi ft) \tag{5}$$

$$v_b^* = A.sin\left(2\pi ft - \frac{2}{3}\pi\right) \tag{6}$$

$$v_c^* = A.sin\left(2\pi ft + \frac{2}{3}\pi\right) \tag{7}$$

where A is the magnitude of reference voltage. By considering the limitation of the possible output voltage produced in the SVM for five-level CHMI, the magnitude A can be calculated as follows:
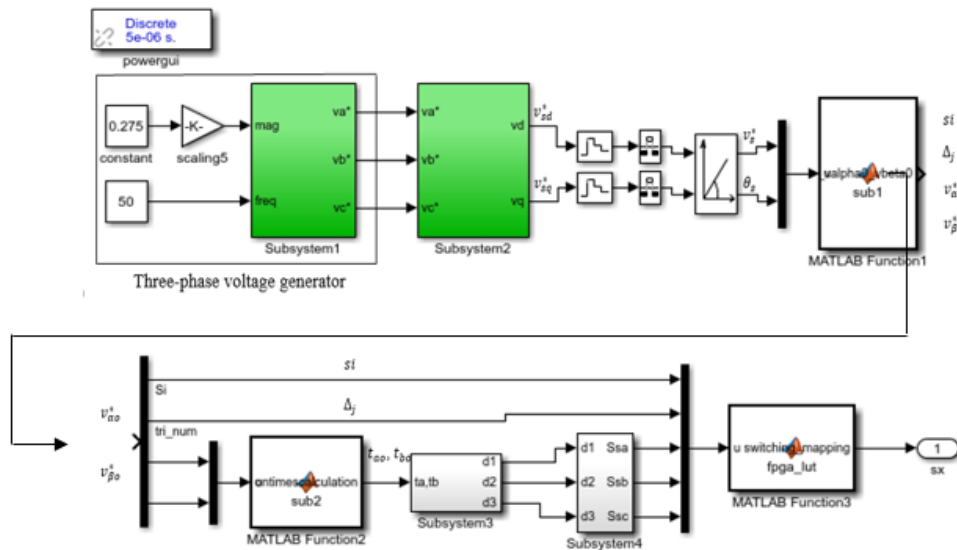
$$A = M\frac{4V_{dc5}}{\sqrt{3}} \tag{8}$$

Figure 5. Simulation model of space vector modulation (SVM) (e.g. for five-level CHMI)

where M can be varied between 0 to 1 for adjusting the magnitude of input and hence output voltages. This means, M is set to 1 for producing the maximum output voltage. The three-phase voltage is then transformed into reference voltage components v_{sd}^* and v_{sq}^*, as the input of the modulator. The transformation is obtained using (9) and (10).

$$v_{sd}^* = \frac{2}{3}\left[v_a^* - \frac{v_b^*}{2} - \frac{v_c^*}{2}\right] \tag{9}$$

$$v_{sq}^* = \frac{1}{\sqrt{3}}\left[v_b^* - v_c^*\right] \tag{10}$$

Using these equations, the transformation is constructed using Simulink blocks as presented in Figure 7. These Simulink blocks are grouped as a *Subsystem2*, as shown in Figure 5.
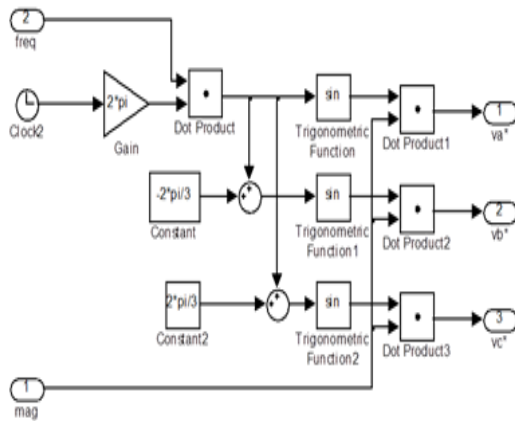
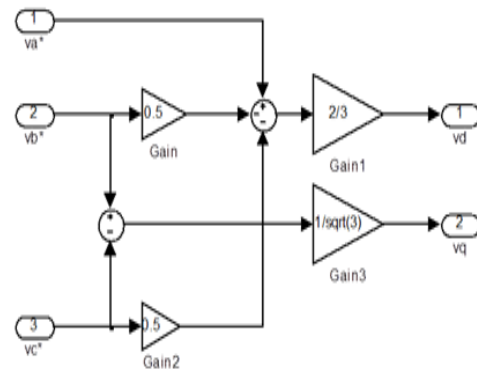Figure 6. The simulation model block of three-phase generator (at *Subsystem1*)

Figure 7. The simulation model block of three- to two-phase transformation (at *Subsystem2)*

It can be noticed from the complete simulation model shown in Figure 5 that the reference voltage components v_{sd}^* and v_{sq}^* are sampled at $DT_1 = 200\ \mu s$ using *Zero-Order Hold* blocks. These two inputs are used to produce reference voltage vector into a polar form using (11) and (12). Then, the magnitude and angle of reference voltage vector, i.e. v_s^* and θ_s are being fed to *MATLAB Function1* block for detecting sectors si, triangles Δ_j, and calculating $v_{\alpha o}^*$ and $v_{\beta o}^*$, as discussed in previous sections. The source code or c-programming written in the *MATLAB Function1* block as shown in Figure 8.

$$v_s^* = \sqrt{\bar{v}_{sd}^{*\,2} + \bar{v}_{sq}^{*\,2}} \tag{11}$$

$$\theta_s = tan^{-1}\left(\frac{\bar{v}_{sq}^{*\,2}}{\bar{v}_{sd}^{*\,2}}\right) \tag{12}$$

```
%   for detecting sectors, triangles, and
calculating
    v*αo and v*βo

function sector_tri_valpha0_vbeta0 =sub1(u)

%initialization
si=0;
tri_num=0;
valphao=0;
vbetao=0;
Vdc=120; % for the case of Five-level CHMI

%define input
mag=u(1);
theta=u(2);

%Determination of sector_i
theta_deg=theta*180/pi;
m=mod(theta_deg,360);
r=rem(m,60);
theta1=r;
si=floor(m/60)+1;
    if (si >6)
        si =1;
    end
%Calculation of k1 & k2
valpha=mag*cos(r*pi/180);
vbeta=mag*sin(r*pi/180);
k1=floor(6/Vdc*(valpha+vbeta/sqrt(3)));
k2=floor(6/Vdc*(2*vbeta/sqrt(3)));
```

```
%Calculation of valphai & vbetai
valphai=6/Vdc*valpha-k1+0.5*k2;
vbetai=6/Vdc*vbeta-k2*sqrt(3)/2;

%calculation of valphao & vbetao
%Determination of triangular number
valphai_=valphai*sqrt(3)
if(vbetai <= valphai_ )
    valphao=valphai*Vdc/3;
    vbetao=vbetai*Vdc/3;
    tri_num=k1^2+2*k2;

else
    valphao=Vdc/3*(0.5-valphai);
    vbetao=Vdc/3*(sqrt(3)/2-vbetai);
    tri_num=k1^2+2*k2+1;

end

  if(tri_num >=15)
    tri_num = 15;
  end

% output
sector_tri_valpha0_vbeta0=[si, tri_num, valphao,
vbetao];
end
```

Figure 8. Source code listing for MATLAB function1 for detecting sectors, triangles, and calculating $v_{\alpha o}^*$ and $v_{\beta o}^*$

```
%    Calculation of on-duration

function ontimescalculation =sub2(u)

%initialization
VdcHB = 120/4;
T = 1/5000;
%define input
valpha0=u(1);
vbeta0=u(2);

%calculation of ta & tb.
ta = 1.5*T/VdcHB*(valpha0-vbeta0/sqrt(3));
tb = sqrt(3)*vbeta0*T/VdcHB;

% output
ontimescalculation=[ta; tb];
end
```

Figure 9. Source code listing for MATLAB function2 for calculating on-duration

The reference voltage components v_{sd}^* and v_{sq}^* produced from *MATLAB Function1* block are then used as the inputs of *MATLAB Function2* block. This block is responsible to calculate on-duration for switching vectors within a triangle for five-level CHMI. The source code for calculating on-duration shown in Figure 9. The on durations t_{ao} and t_{bo} produced from the *MATLAB Function2* block are used to calculate duty ratios of pre-switching states for each phase, d_a, d_b and d_c. The calculation is performed by *Subsystem3* block, as can be noticed in Figure 5. Figure 10 shows Simulink blocks contained in *Subsystem3* block, which are constructed using (13), (14) and (15) for five-level CHMI.

$$d_a = \frac{T - 2\left(\frac{t_{og}}{4}\right)}{T} \tag{13}$$

$$d_b = \frac{T - 2\left(\frac{t_{og}}{4} + \frac{t_{ao}}{2}\right)}{T} \tag{14}$$

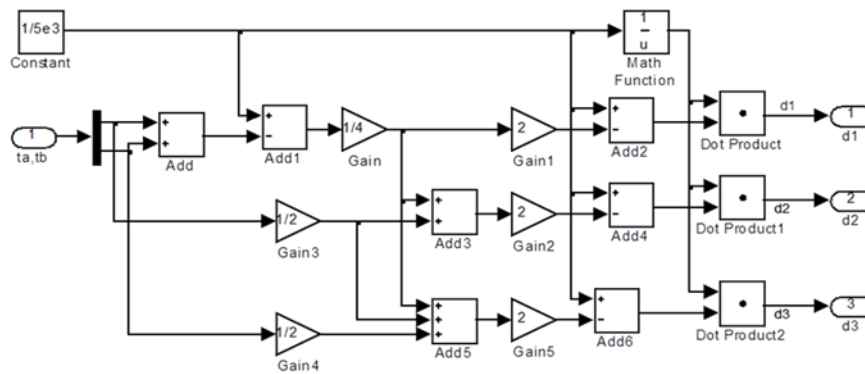$$d_c = \frac{T - 2\left(\frac{t_{og}}{4} + \frac{t_{ao}}{2} + \frac{t_{bo}}{2}\right)}{T} \tag{15}$$

Figure 10. The simulation model block of duty ratios calculator (at *Subsystem3)*

Figure 11 shows a simulation model of pre-switching states generator which is developed based on the comparison between duty ratios and triangular waveform. The simulation model or Simulink blocks are grouped as a *Subsystem4*, as depicted in Figure 5. The triangular waveform is generated at sampling time $DT_2 = 5\mu s$ by the *Repeating Sequence* block, while the duty ratios are updated every $DT_1 = 200\ \mu s$.
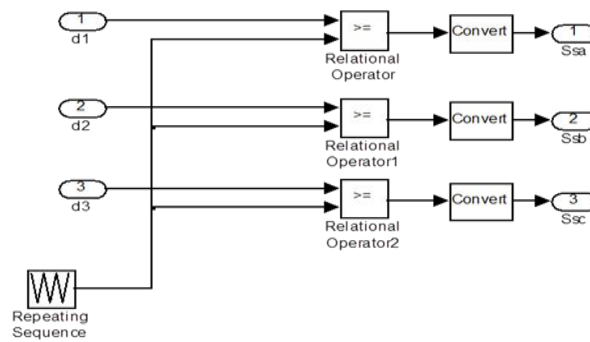
Figure 11. The simulation model block of pre-switching states generator (at *Subsystem4*)

At the last part of Figure 5, it can be observed that all the information such as sector (si), triangle (Δ_j) and pre-switching states (S_{sa}, S_{sb} and S_{sc}) for selecting appropriate switching states to drive IGBTs of five-level CHMI. That performed by *MATLAB Function3* block, as shown in Figure 5, the source code as shown in Figure 12 is given first sector (si) at first triangle (Δ_j).

```
%    Calculation of on-duration

function switching_mapping = fpga_lut(u)

%initialization
sx=[0 0 0 0 0 0 0 0 0 0 0 0];

%define input
si=u(1);
tri_num=u(2);
s1=u(3);
s2=u(4);
s3=u(5);

% inputs: sector=u[0],number of
triangular=u[1],s1=u[2],s2=u[3],s3=u[4]

%generation of gate pulses s1, s2 & s3;
%For sector=1
*********************************************
********
if (si == 1)
    %For triangular = 0
    if(tri_num == 0)|
        if (s1 == 0 && s2 == 0 && s3 == 0)
            sx = [1 0 0 0 1 0 0 0 1 0 0 0];
        elseif (s1 == 1 && s2 == 0 && s3 == 0)
            sx = [0 0 0 0 1 0 0 0 1 0 0 0];
        elseif (s1 == 1 && s2 == 1 && s3 == 0)
            sx = [0 0 0 0 0 0 0 0 1 0 0 0];
        elseif (s1 == 1 && s2 == 1 && s3 == 1)
            sx = [0 0 0 0 0 0 0 0 0 0 0 0];
        end
```

Figure 12. Source code listing for MATLAB FUNCTION3 for producing switching states

Finally, the switching states are used to drive IGBTs of the inverter. Figure 2 depicts simulation models for five-level CHMI. Note that, the switching of IGBTs is determined by the switching states, provided that the switching of upper and lower IGBTs for each leg must be complimented to each other. The output of each inverter is connected to an identical three-phase and series connected resistive and inductive loads.

2.3. The description of experimental setup

In this section describes the assignments of the circuits or components employed to set up the experimental platform for verifying the effectiveness of SVM technique for five-level cascaded H-bridge multilevel inverters. The structure of experimental platform indicated the components used, as shown in Figure 13. The Field Programmable Gate Arrays (FPGA) Controller was utilized to perform the tasks of SVM technique.

2.4. FPGA controller

The Field Programmable Gate Arrays (FPGA) Controller is known to have high-speed clock which is superior to execute logical or digital operation. It featured a powerful Altera Cyclone IV EP422F17C6N FPGA with 22,320 logic elements, 32 MB of SDRAM, 2 kb EEPROM, and a 64 Mb serial configuration memory device. The FPGA board 40-pin Headers (GPIOs) provided 72 I/O pins, 5V power pins, two 3.3V power pins and four ground pins, 153 maximum FPGA I/O pins and 56 embedded multipliers. The DE0-Nano board included a built-in USB Blaster for FPGA programming, and the board could be powered either from this USB port or an external power source. Inputs and outputs included 2 pushbuttons, 8 user LEDs and a set of 4 dipswitches. The board included expansion headers to attach various terasic daughter cards or other devices. Figure 13 shows the FPGA receives information of Quartus II program and pre-switching states S_{sa}, S_{sb} and S_{sc}. The FPGA is accountable to perform the assignment of selecting suitable switching states based on the date received. This task is similar to the *MATLAB Function3* block as depicted in Figure 5.
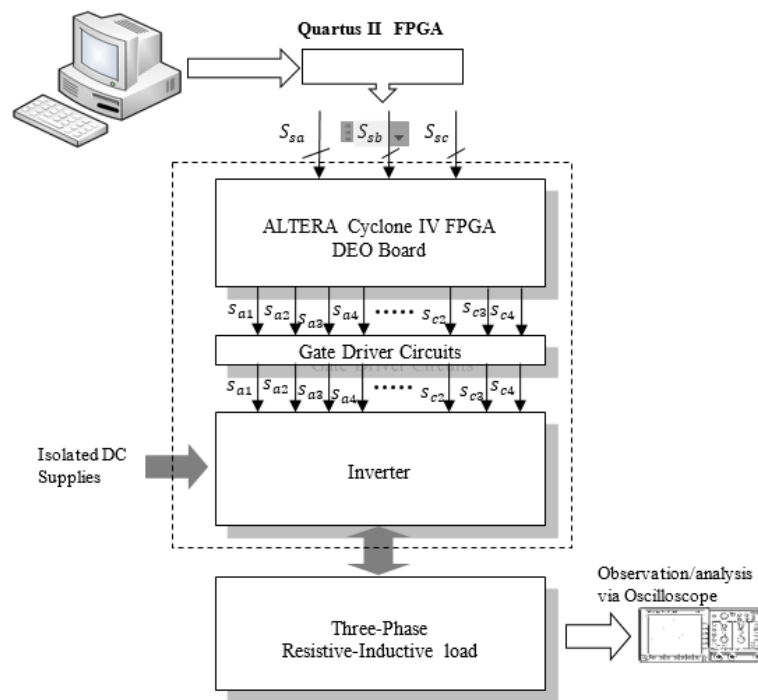

Figure 13. The experimental setup

2.5. Quartus II program for FPGA controller board

The Quartus II absorbed the data obtained from the switching signals for driving IGBTs stored in MATLAB workspaces. Then, the data were saved in Excel file. Next, the data were transferred to mif file. The first part in programming created a project name (New Project), family and device settings for FPGA. The number of word (4001) were selected which could transfer the data from 12 switching states of Excel file to 12 switching states of mif.file. This file consisted of 0-4000, then, displayed the mif file. at Quartus II. The Mega Wizard Plug-In Manager would insert (sa1...sa4, sb1...sb4 and sc1...sc4) under (mif file). VHDL file was created and saved as 'svm5level'.vhd for computational purposes. In addition, other VHDL Files saved as 'clk_div'.vhd, 'blanking_comparator'.vhd, 'blanking_lower_counter'.vhd, 'blanking_mod18'.vhd, 'blanking_upper_counter'.vhd and 'blankingteme_main'.vhd, edit coding were created as shown in Figure 13. Then, the project was analysed after verifying the success of the analyses. The assigning pin on FPGA selected pin planner for 2 inputs and 24 output pins 12 lower switching outputs and upper switching outputs. Hence, a full compilation design was successful to programme the FPGA hardware in order to see the display of output waveform on oscilloscope, as shown in Figure 14.
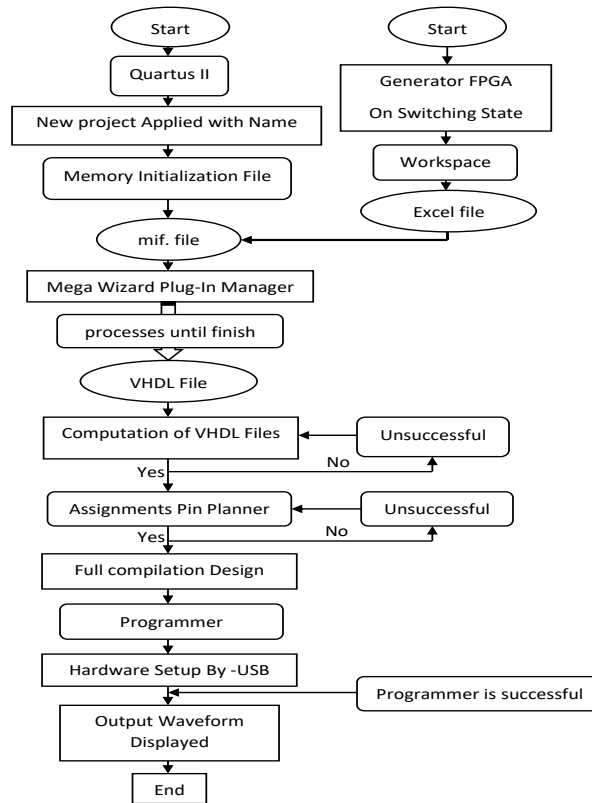
Figure 14. Flowchart of applaid FPGA in quartus ii program

2.6. Power inverter and gate driver circuits

Figure 15 the FPGA for circuit cascaded H-bridge multilevel inverter CHMI and gate driver e.g. for five-level. The FPGA controller, it applied the date from Quartus II Program to absorb the gate driver and power inverter circuits they are used to produce desired output voltages. The aim of use gate driver circuits was to provide isolation between the electronic control circuits and power inverter circuits and provide enough power expansion for switching IGBTs. Hence, the same switching states were produced from the output of gate driver circuits, yet, with different grounding points. The identical switching states were used to drive IGBTs in CHMI with enough voltage and current. Figure 15 showed the six units of H-Bridge inverter circuits to plant five-level CHMI as shown in Figure 2. Every H-Bridge inverter circuit was supplied by an isolated DC voltage supply.
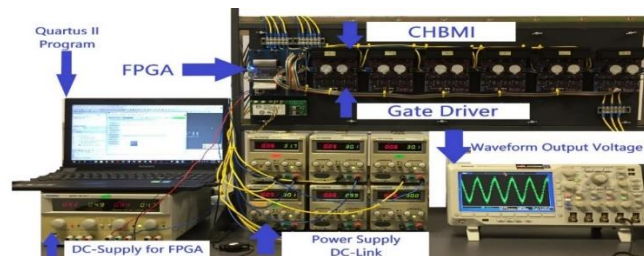

Figure 15. The FPGA for circuit CHMI and gate driver e.g. for five-level

3.   RESULTS AND DISCUSSION

In this part evaluates the total harmonic distortions (THD) of output voltage and the fundamental output voltage V_a for five-level inverter of Space Vector Modulation (SVM) technique. The evaluation is based on the simulation results i.e. the values of THD and fundamental output voltage are obtained using Fast Fourier Transforms (FFT) analysis and validated with the experimental results. The results are obtained at

modulation indices $M_i = 0.9$. The results obtained from the evaluation as shown in Figure 16 in which simulation results as well as experimental results are shown at figures, it can be observed that the experimental results are in close agreements with the simulation results. The compered obtained between the fundamental output voltage in SVM technique being enhanced about 15% of that obtained in the conventional SPWM technique at same modulation indices $M_i = 0.9$ as shown in Figure 17. Note the results are obtained using sampling time $DT_2 = 5 \ \mu s$ i.e. at fast rate of computation, where the error between the simulation and experimental results is insignificant and approximately less than 1 %.
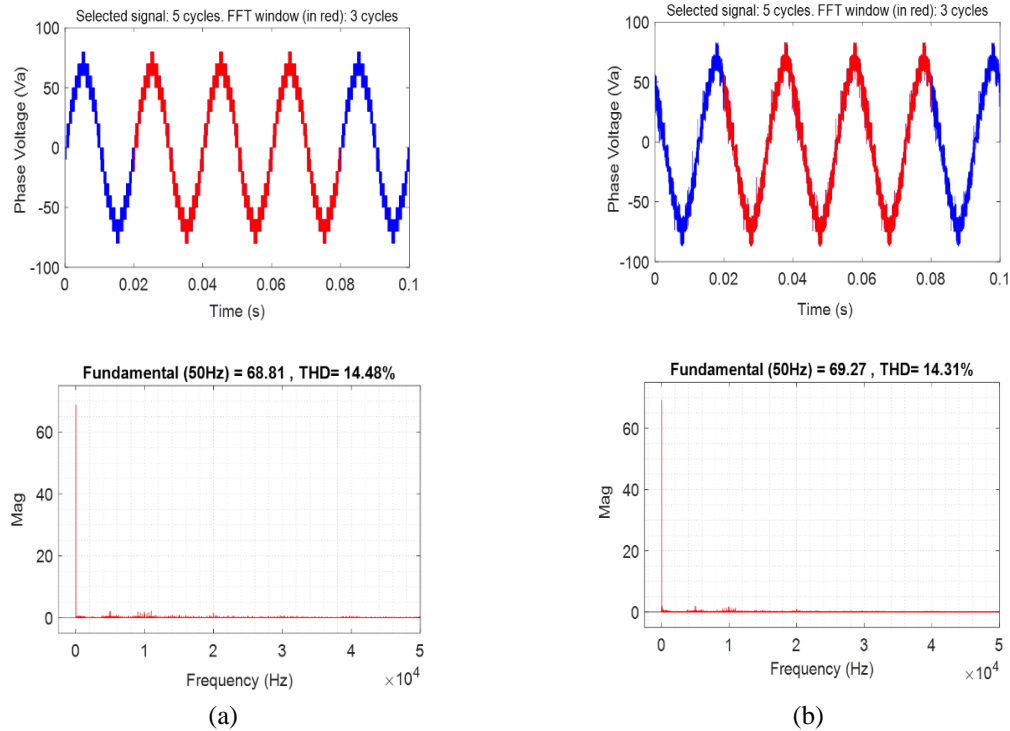

(a)   (b)

Figure 16. The simulation and experimental results of THD and fundamental output voltage for SVM technique five-level inverters (a) simulation results (b) experimental results
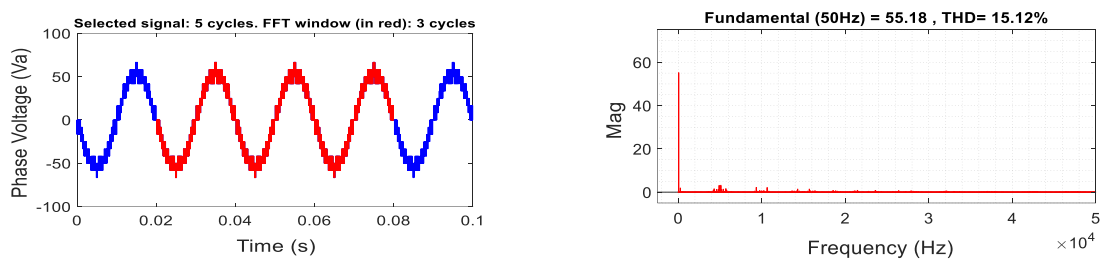

Figure 17. Simulation results of THD and fundamental output voltage for five-level inverters SPWM technique

4. CONCLUSION

This paper has provided in-depth verified the advantage of multilevel inverter CHBI producing lower total harmonic distortion THD output voltage for five-level inverter, via simulation and experimental results. It has shown that the experimental results are nearly to the simulation results of the SVM technique, thus verify the effectiveness and proper operation of the SVM hardware implementation. The similarity between the simulation and experimental results as well as similarities between the fundamental output

voltage obtained via simulation and calculation value, confirming that the development of the space vector modulator using a FPGA controller concept is accurate which suitable to be applied in AC motor control for high performances, that the generation of switching signals performed by FPGA is at the same sampling time TD=5 μs, i.e. as sampled in MATLAB. Using this approach, the computational burden of SVM become greatly minimized and the desired output voltage can be obtained. The compered obtained between the maximum fundamental output voltage in SVM technique being enhanced about 15% of that obtained in the conventional SPWM technique

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