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Asymmetric hybrid multilevel inverter with reduced harmonic using hybrid modulation technique

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Article Info	ABSTRACT
	This paper studies the Asymmetric cascaded three phase multilevel inverter developed with hybrid modulation technique applied for an industrial application. The aim of this paper to reduce the Total harmonics distortion in the cascaded multi level inverter by introducing the new concept to develop the three phase CMLI. This inverter has two segments, one segment has H-bridge inverter and another segment has sequential arrangement of power semi conductor switches with asymmetrical voltage source in the ratio of 1:2. Similarly develop the segments for other phases. This new topology is called as Hybrid MLI. This hybrid MLI is used to reduce the no of semiconductor device requirement and the Total harmonics distortion. The inverter is controlled by Phase disposition (PD) and alternative phase opposition disposition PWM technique (APOD). This control technique is used to minimize the current harmonic and increase the system performance. The circuit is simulated using Matlab circuit and its performance is compared using PD and APOD PWM techniques and verified with simulation results.

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1. INTRODUCTION

Power electronics converters are mostly used to convert low voltage DC into high voltage DC conversion and other conversion (AC to DC) applications due to their advancements. Many industries are required good quality and high power for running the equipment. Due to industry requirements many research works are going in the field of increasing power handling capACity and improve the power quality. In this paper discuss about reduce the harmonic using hybrid modulation technique and improve the power handling capACity of the inverter. MLIs are used to improve the power quality and high-power applications [1-6]. Cascaded multi level inverter is discussed in [7-11] and it is superior compare than other multi level inverter topologies [7-11]. Cascaded multi level inverter is also further classified symmetrical and asymmetrical type. The symmetrical topology has equal voltage source and required more DC source and H-bridge inverter. Asymmetrical topology has unequal voltage source and less no of DC sources and H-bridge compare than symmetrical method [12-18].

The combination of two other inverter topologies is called as Hybrid topology. Hybrid topology has proposed further reduced the component and harmonics [19]. Many modulation techniques are developed for control the inverter and reduced the harmonic [20-25]. Each method has some advantage and disadvantages. The combination of neutral clamped three level inverter with H-bridge based three phases asymmetrical VSI fed three phase induction motor circuit is proposed in this paper. The proposed hybrid inverter is used to

reduce the harmonic and power handling capACity. This inverter is controlled by using hybrid modulation technique. The circuit operation and simulation results will be discussed in the following section.

2. CIRCUIT DESCRIPTION

The proposed three phase hybrid MLI which combines the asymmetrical neutral point diode clamped three level inverters with integrated h-bridge inverter fed induction motor circuit diagram is as shown in figure 1. This proposed circuit has asymmetrical input source, three level and H-bridge combination and motor load. The three-level inverter is used to distribute the power and increase the power handling capACity. This inverter switches are controlled by multi carrier PWM technique. The switching table is as shown in table 1 for single leg. Similarly, other two legs switches are triggered with 120-degree Phase shift from eACh phase. Table 1 shows the switching state of HMLI. the output voltage level is produced based on the voltage level required. For generating +3 VDC switch S1, S4, S5 and S8 are turned ON. Similarly, other voltage levels are also AChieved.
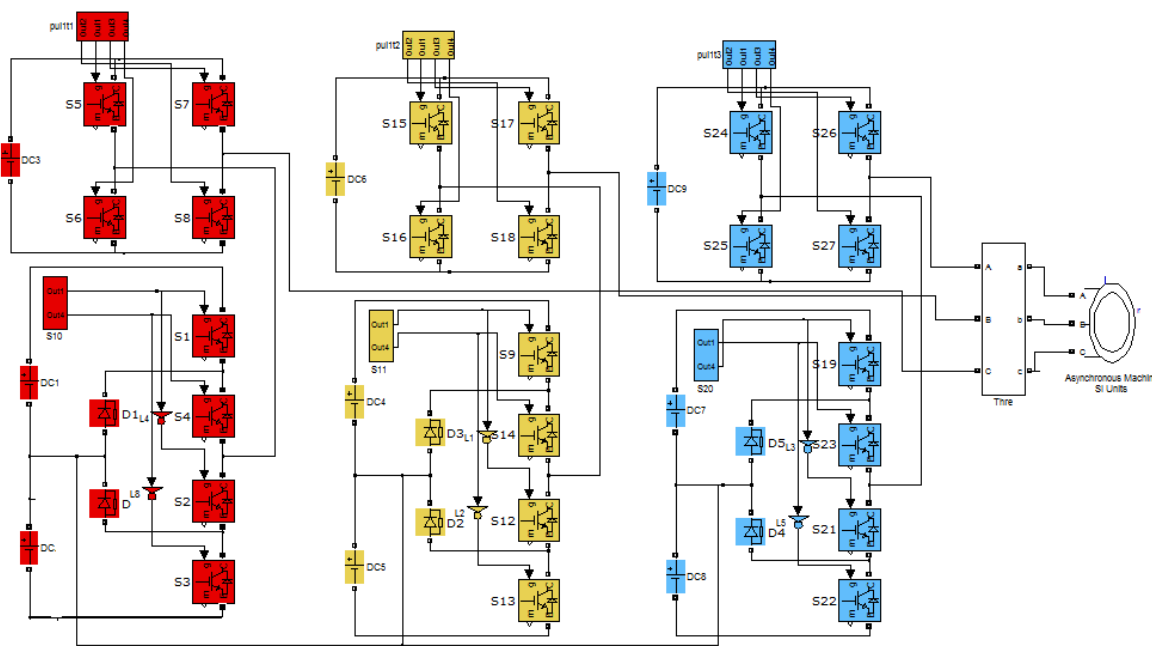

Figure 1. Proposed 3 phase HMLI circuit diagram

Table 1. Switching states of HMLI topology

Level	S1	S2	S3	S4	S5	S6	S7	S8
-3V	0	1	1	0	0	1	1	0
-2V	0	1	0	1	0	1	1	0
-1V	0	1	1	0	1	0	1	0
0V	0	1	0	1	1	0	1	0
1V	1	0	0	1	1	0	1	0
2V	0	1	0	1	1	0	0	1
3V	1	0	0	1	1	0	0	1

3. CONTROL TECHNIQUE：

Multi carrier Sine PWM technique is applied for control the proposed inverter. In this method sine reference signal is compared with multiple triangle carriers with different voltage level. EACh carrier produces different voltage level of the inverter. PD and APOD method were generated for control the proposed inverter output. When eACh carrier signal is generated in opposite phase is called as phase opposite disposition PWM technique. This pulse generation method is as shown in Figure 2 (a) and Figure (b).
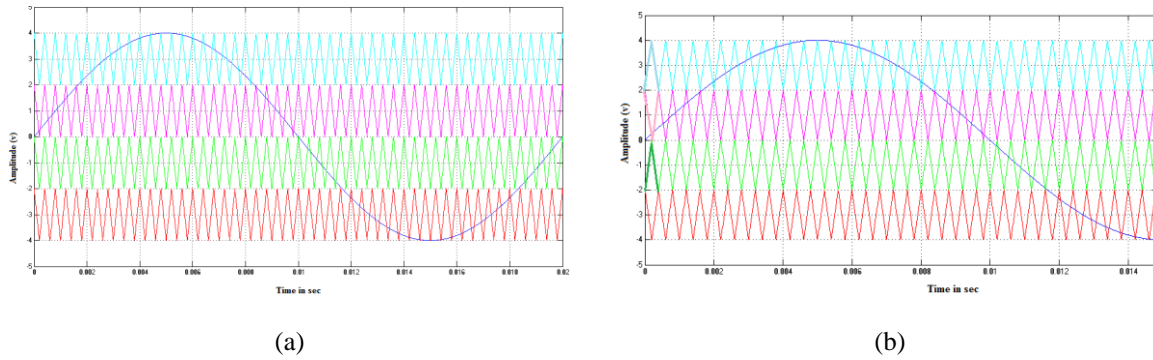
(a)   (b)

Figure 2. Hybrid multilevel inverter using a) PD method. b) APOD method

4. SIMULATION RESULTS:

The simulation diagram has been developed for the proposed inverter. This inverter output voltage is controlled by multi carrier PWM technique. PDPWM method and APODPWM method are developed for determine the inverter performance. Figure 3(a) and Figure 3(b) shows the output phase voltage HMLI for resistive load. It has almost sinusoidal waveform the output phase voltage for 7 level hybrid multi level inverter using phase opposition disposition and Alternative phase opposition and disposition as shown Figure 3(a) and Figure 3(b)
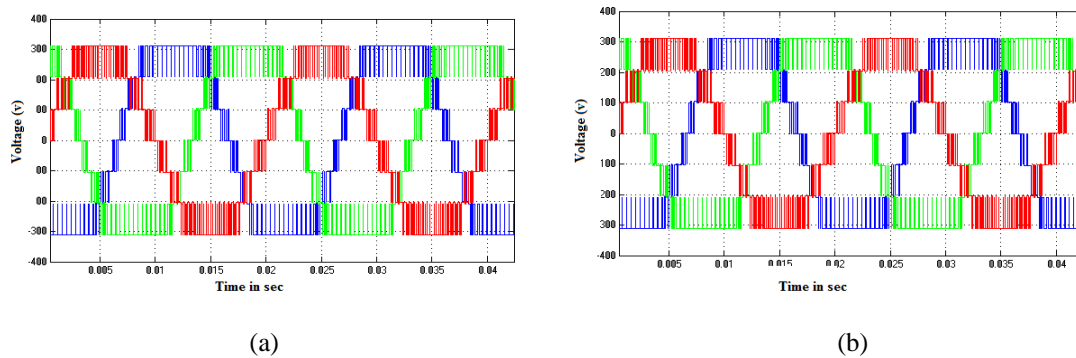

(a)   (b)

Figure 3. Output phase voltage for HMLI using a) PD b) APOD method (R LOAD)

Figure 4(a) and Figure 4(b) shows the output line voltage HMLI for motor load. It has approximately sinusoidal waveform The output line voltage for 7 level hybrid multi level inverter using phase opposition disposition and Alternative phase opposition and disposition are as shown Figure 4(a) and Figure 4(b).

(a)   (b)

Figure 4. Output line voltage for HMLI using a) PD b) Figure 4. APOD method (motor LOAD)

Figure 5(a) and Figure 5(b) shows the load current HMLI for motor load. The load current for 7 level hybrid multi level inverter using phase opposition disposition and Alternative phase opposition and disposition are as shown in Figure 5(a) and Figure 5(b)
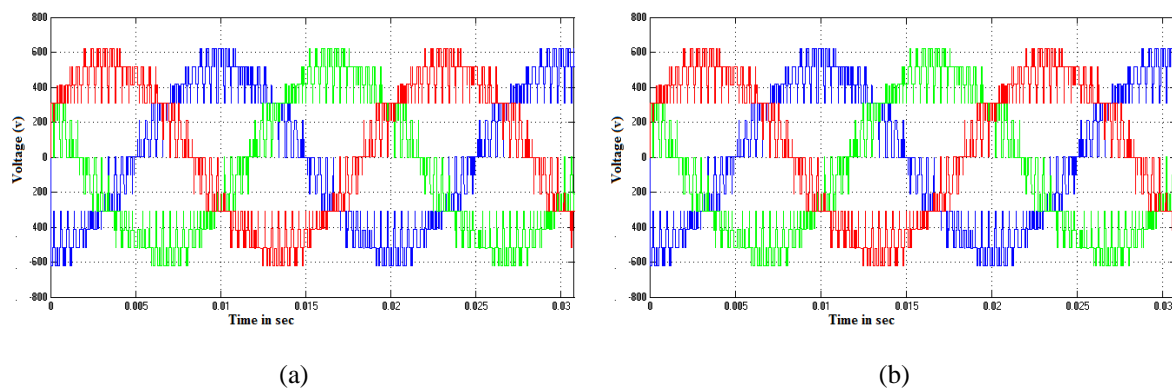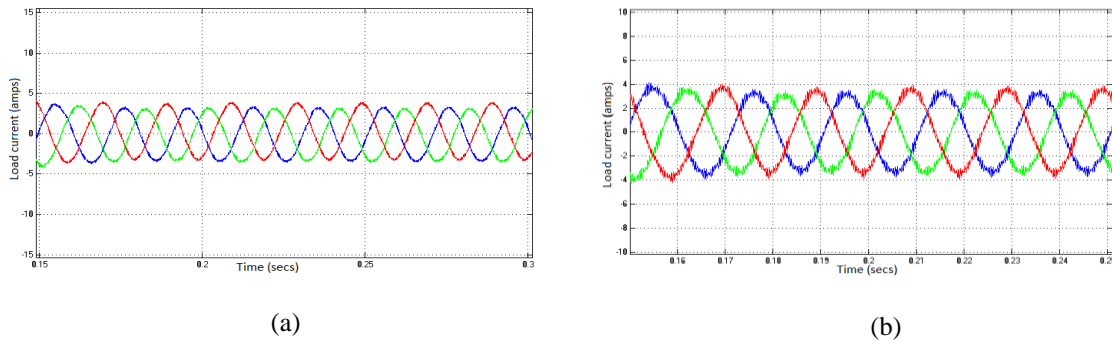

(a)   (b)

Figure 5. Load current for HMLI using a) PD, b) APOD method (motor LOAD)

Figure 6 shows the load current FFT analysis for HMLI. As a result this current output has less current harmonic. The load current FFT analysis for 7 level hybrid multi level inverter using phase opposition disposition and Alternative phase opposition and disposition are as shown in Figure 6(a) and Figure 6(b). Figure 7 shows the rotor speed of motor connected with HMLI. The rotor speed for 7 level hybrid multi level inverter using phase opposition, phase disposition and Alternative phase opposition and disposition are as shown in Figure 7(a) and Figure 7(b). Figure 8 shows the rotor torque in HMLI. The rotor torque for 7 level hybrid multi level inverter using phase opposition disposition and Alternative phase opposition and disposition are as shown in Figure 8(a) and Figure 8(b).
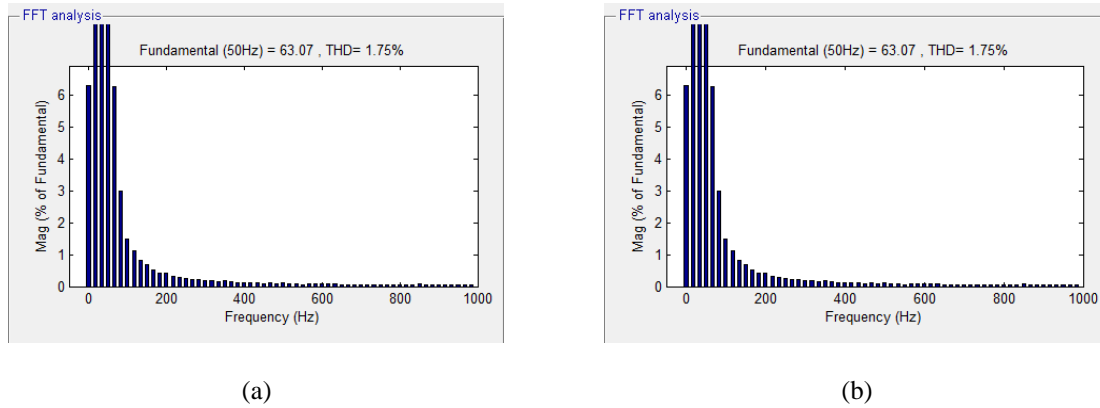

(a)   (b)

Figure 6. FFT Analysis for output current (m=1) using, a) PD, b) APOD method (motor LOAD)
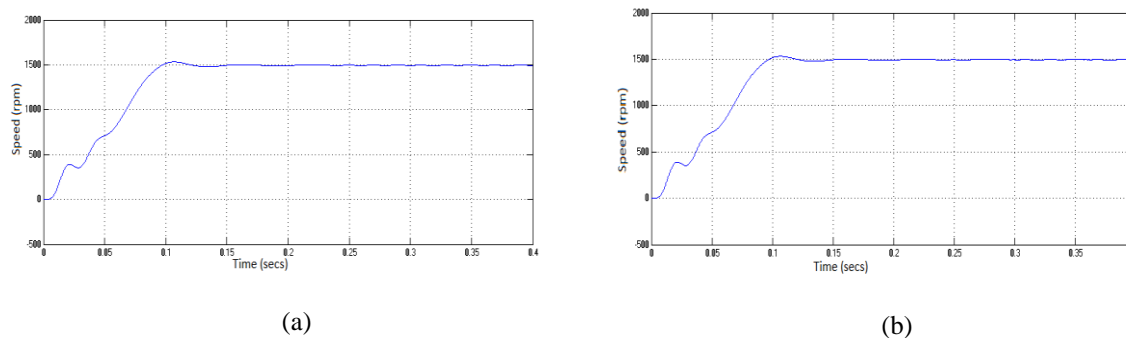

(a)   (b)

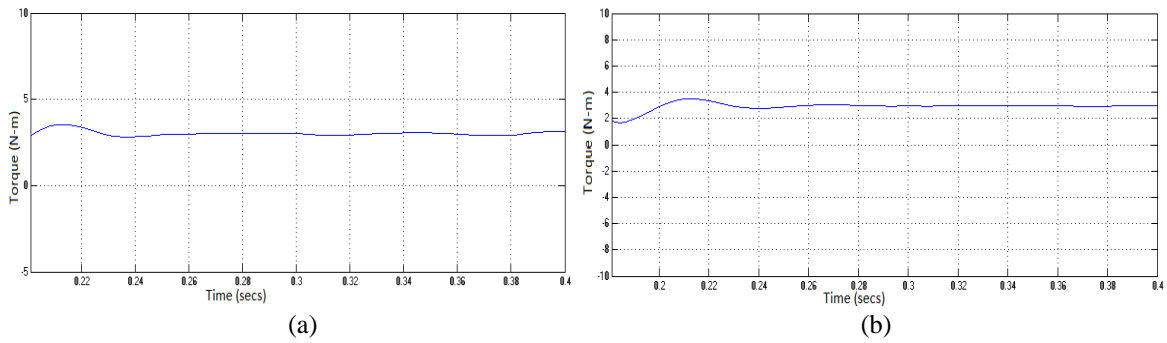Figure 7. Rotor speed in rpm, a) PD b) APOD method (motor LOAD)

Figure 8. Torque in n-m a) PD, b) Figure 8. APOD method (motor load)

5.   COMPARATIVE ANALYSIS:

Both PDPWM and APODPWM methods are used to determine the proposed inverter performance. PD method has less harmonic compare than APOD technique by varying modulation index from 0.7 to 1. It is shown from Table 2 and Figure 9. Inverter output voltage has more distortion in APOD PWM method compare than PDPWM method.

Table 2. Modulation index vs % of THD

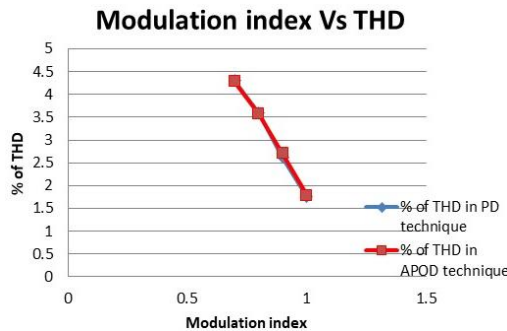| Modulation index	% of THD in PD technique	% of THD in APOD technique
0.7	4.3	4.28
.8	3.59	3.57
.9	2.62	2.70
1	1.75	1.79

Figure 9. Graph between modulation index and total harmonic distortion

6.   CONCLUSION

The asymmetric cascade three phase multilevel inverter-based power supply proposed for AC motor application. This circuit is simulated using PDPWM and APODPWM method for compare the system performance. PD method has less current harmonic of 1.75% compare than APOD technique current harmonic of 1.79% by modulation index 1. Inverter output voltage has more distortion in APODPWM method compare than PDPWM method. PDPWM method gives better performance compare than APODPWM method. It is proved from simulation results. This proposed hybrid multilevel inverter has less components count compare than other multilevel inverter topology.

REFERENCES
[1]   Pharne I.D. and Bhosale Y. N, "A Review on Multilevel Inverter Topology," *IEEE Conference on Power Control and Embedded Systems*, pp.700-703, Feb 2013.
[2]   R Anjali Krishna and L Padma Krishna, "Brief Review on Multi Level Inverter Topologies," *International Conference on Circuit, Power and Computing Technologies*, *IEEE*. Mar, 2016.

[3]   Jos Rodrguez, Jih-Sheng Lai, "Multilevel Inverters: A Survey of Topologies, Controls, and Applications," *IEEE TransACtions on Industrial Electronics*, vol. 49, no.4, pp.2703-2712, August 2002.

[4]   B. ZhiHong and Z. ZhongChao, "Conformation of Multilevel Current Source Converter Topologies Using the Duality Principle," *Power Electronics, IEEE TransACtions*, vol. 23, pp. 2260-2267, 2008.

[5]   P. Steimer and M. Manjrekar, "PrACtical Medium Voltage Converter Topologies for High Power Applications," in *Proceedings of the IEEE Industry Applications Society Annual Meeting (IAS)*, vol. 3, 2001, pp. 1723-1730.

[6]   J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron*, vol. 54, no. 6, pp. 2930-2945, Dec. 2007.

[7]   M. Malinowski, K. Gopakumar, J. Rodr´ıguez, M. A. Perez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron*, vol. 57, no. 7, pp. 2197-2206, Jul 2010.

[8]   A. Ajami, M. R. Jannati Oskuee, M. T. Khosroshahi, A. Mokhberdoran, "Cascade multi-cell multilevel converter with reduced number of switches," *IET Power Electron*, vol. 7, no. 3, pp. 552-558, 2014.

[9]   Thiyagarajan V, Somasundaram P, "A New Seven Level Symmetrical Inverter with Reduced Switch Count," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 9, no. 2, pp. 921-925, Jun 2018.

[10]   Muhammad T, et al, "Cascaded Symmetric Multilevel Inverter with Reduced Number of Controlled Switches," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 8, no. 2, pp. 795-803, Jun 2017.

[11]   Zulkefle A, et al, "Modeling and Simulation of Nine-Level Cascaded H-Bridge Multilevel Inverter," *Indonesian Journal of Electrical Engineering and Computer Science (IJEECS)*, vol. 11, no. 2, pp. 696-703, Aug 2018.

[12]   S. Satish kumar Dr M. Sasikumar, "Diminution of Harmonics in a Cascaded Multilevel Inverter Using Third Harmonics Injection PWM Technique," *International Journal of Recent Technology and Engineering (IJRTE)*, vol. 8, no.3, pp. 7493-7497, Sep 2019. ISSN: 2277-3878.

[13]   S. Kakar, S. M. Ayob, N. M. Nordin, M. S. Arif, A. Jusoh, N. D. Muhamad "A novel single-phase PWM asymmetrical multilevel inverter with number of semiconductor switches reduction," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 10, no. 3, pp. 1133-1140, Sep 2019.

[14]   V S Prasadarao K1, V Joshi Manohar, "Grid Interconnection of PV System Using Symmetric and Asymmetric MLI Topology," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 9, no. 4, pp. 1616-1623, Dec 2018.

[15]   Motaparthi Nagaraju, Malligunta Kiran Kumar, "Analysis of series/parallel multilevel inverter with symmetrical and asymmetrical configurations," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 10, no. 1, pp. 300-306, Mar 2019.

[16]   J. Song-Manguelle, S. Mariethoz, M. Veenstra and A. Rufer, "A Generalized Design Principle of a Uniform Step Asymmetrical Multilevel Converter for High Power Conversion," in *Proceedings of the European Power Electronics and Applications Conference (EPE 2001)*, Graz, Austria, 2001.

[17]   S. Mariéthoz and A. Rufer, "Design and Control of Asymmetrical Multi- Level Inverters," in *Proceedings of the IEEE Industrial Electronics Society Conference (IECON 2002)*, 2002.

[18]   Lipika Nanda, A Dasgupta, U. K. Rout, "A comparative Analysis of Symmetrical and Asymmetrical Cascaded Multilevel Inverter Having Reduced Number of Switches and DC Sources," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 8, no. 4, pp. 1595-1602, Dec 2017.

[19]   Babitha T Abraham, Anish Benny, "Asymmetric Multilevel Hybrid Inverter with ReducedNumber of Switches," International Conference on Magnetics, MAChines & Drives (AICERA-2014 iCMMD)

[20]   R. Gupta, A. Ghosh, A. Joshi, "Switching charACterization of cascaded multilevel-inverter-controlled systems," *IEEE Trans. Ind. Electron*, vol. 55, no. 3, pp. 1047-1058, Mar. 2008.

[21]   N Sujitha, S Satish Kumar, M Sasikumar, "Design And Implementation Of Hybrid Spwm Control For Cascaded H-Bridge Multi Level Inverter For Motor Drives," *IU-Journal Of Electrical & Electronics Engineering*, ImpACt FACtor:- 0.14, vol. 14, no. 1, pp. 1721-1727, March 2014

[22]   M. Calais, L. J. Borle, V. G. Agelidis, "Analysis of Multicarrier PWM Methods for a single-phase Five Level Inverter," Power Electronics Specialists Conference, 2001. PESC. IEEE 32nd Annual, pp. 1351-1356.

[23]   M. G. Hosseini Aghdam, and S. H. Fathi, "Analysis of Conduction and Switching Losses in Three-Phase Asymmetric Multi-Level Cascaded Inverter," *WSEAS TransACtions on Circuits and Systems*, vol. 4, no. 7, pp. 773-780, July 2005.

[24]   A. Ajami, M. R. Jannati Oskuee, A. Mokhberdoran, H. Shokri, "Selective harmonic elimination method for wide range of modulation indexes in multilevel inverters using ICA," *J. Cent. South Univ*, vol. 21, no. 4, pp. 1329-1338, 2014.

[25]   Youssef Babkrani, Ahmed Naddami, Mohamed Hilal, "A smart cascaded H-bridge multilevel inverter with An optimized modulation techniques increasing the quality and reducing harmonics," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 10, no. 4, pp. 1852-1862, Dec 2019.