A Novel Packaging and System-Integration Platform with Integrated Antennas for Scalable, Low-Cost and High-Performance 5G mmWave Systems

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***Abstract*— In this work, we present a novel packaging and system-integration platform with integrated antennas (antenna-in-package, AiP, platform) for 5G millimeter-wave (mmWave) systems. We illustrate the application of the platform for the development of miniaturized, scalable, low-cost and high-performance 5G mmWave systems for new radio (NR) base stations. RF characterization of the dielectric material of the platform and the integrated mmWave antennas as well as thermal investigations of the platform are presented. The process steps required for the fabrication of the platform are discussed, and an example of a mmWave chip embedded in the platform is shown.**

***Index Terms*—5G mmWave, PCB embedding, system-integration platform, integrated antenna, antenna-in-package, mobile communication system, new radio, base stations**

I. Introduction

The development of 5G millimeter-wave (mmWave) systems is a challenging task, partly because of the extremely high channel losses in the mmWave band which have severe impact on signal-to-noise ratio and throughput. To overcome this challenge, a myriad of mmWave MIMO system architectures which enable hybrid beamforming have been extensively studied, predominantly from signal processing perspective, within the last five years [1] – [5]. However, hardware implementation of these architectures requires new mmWave packaging and system-integration platforms with integrated antennas, also referred to as antenna-in-package (AiP) platforms in published literature. In order to be used for the development of scalable, miniaturized, low-cost and high-performance 5G mmWave systems, these AiP platforms must meet at least five key requirements, namely low-cost, high-performance, reliability, scalability and miniaturization requirements.

So far, a variety of outstanding packaging and system-integration platforms with integrated antennas (AiPs) for 5G mmWave have been proposed by academia and industry. These include organic-based multilayered AiP with integrated air cavity [6], ceramic-based multilayered AiP [7], mold-based fan-out wafer level AiP [8] and glass-based AiP [9] platforms. Although each of these AiP platforms meet some of the key requirements for the development of scalable, low-cost, miniaturized and high-performance 5G mmWave systems, none of them meet all the requirements.

In this work, we present a novel AiP platform which meets all the key packaging and system-integration requirements for 5G mmWave. We also illustrate the application of this platform for the development of miniaturized, scalable, low-cost and high-performance 5G mmWave systems for new radio (NR) base station applications.

The remaining sections of this paper are structured as follows: In section II, the five key packaging and system-integration requirements for 5G mmWave are given. In section III, the new AiP platform is extensively discussed. Since this platform meets all the key requirements for 5G mmWave, it was used for the development of 5G mmWave systems within the framework of a European Union (EU) flagship project, called SERENA. In section IV, the fundamental mmWave AiP module being developed in the SERENA project is presented. RF characterization of the dielectric materials of the platform and the integrated antennas as well as thermal characterization of the platform are discussed in section V and section VI, respectively. Finally in section VII, the printed circuit board (PCB) embedding process used for fabricating the module is presented.

In this work “packaging and system-integration platform with integrated antennas” is used synonymously with “antenna-in-package (AiP) platform”.

II. Key Packaging and System-Integration Requirements for 5G mmWave

In this section, the key packaging and system-integration requirements for 5G mmWave are briefly presented. An elaborate discussion is given in [10].

The authors of this paper believe that the most important requirement is the **low-cost requirement**. The packaging materials, interconnects and processes used for fabricating mmWave AiP platforms must be cost-effective, and thus enable the development of low-cost 5GmmWave modules and systems. To meet the **high-performance requirement**, the AiP platform must enable the following:

1) Fabrication and integration of high gain and broadband mmWave antennas arrays
2) Intra-system electromagnetic compatibility (EMC)
3) High equivalent isotropic radiated power (EIRP) for the same antenna gain and output power of power amplifier
4) Signal integrity (SI)
5) Power integrity (PI)
6) Fabrication and integration of high quality factor (Q-facor) passives for co-design of active mmWave frontend transceiver components
7) Heterogeneous integration (HI)

Another key requirement that must be met by AiP platforms for 5G mmWave is the **scalability requirement**. This enables the development of a fundamental module (e.g., 2X2, 2X4), which can be up-scaled in both lateral dimensions to address a vast range of applications with different power requirements. In order to meet the **reliability requirement**, the AiP platform must, at least, provide a direct thermal path from the chip to the outside world, so as to enable the heat generated by the power amplifiers to be conducted out of the package. Lastly, the AiP must meet the **miniaturization requirement**, especially if it is to be used for the development of mobile devices.

III. A New Packaging and System-Integration Platform (AiP) for 5G mmWave Systems

Figure 1 shows an example of a stack-up of the novel AiP platform for 5G mmWave applications, proposed in German, European and US patent applications [11], [12]. It consists of at least an antenna layer, a shielding layer, a routing/redistribution, a component layer and a temperature control layer. These layers are depicted by the numbers (1) to (5), respectively in figure 1.

This platform is conceptually designed to meet all the requirements given in section II. The mmWave frontend chips are embedded face-up in the component layer. The top side of the chips are connected directly to the antenna using very short interconnects through the routing/re-distribution layer. This enables very high-frequency signals to be transmitted between the chip and antenna with negligible insertion and return losses. The bottom side of the chips are connected to the outside world, for example, through a metal core or thermal vias (in the temperature control layer) and solder balls for heat dissipation. Passive components can be fabricated on the re-distribution layer very close to the mmWave frontend chips, or embedded in the component layer beside the chips (fan-out area). This close proximity between the chips and the passives minimizes the parasitic effects of the interconnects between the two components.

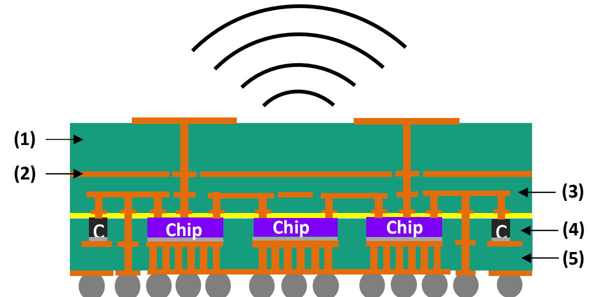


Figure 1: Example of a stack-up of the novel AiP platform for 5G mmWave. (1) antenna layer; (2) shielding layer; (3) re-distristribution/rougting layer; (4) component layer; (5) temperature control layer.

In the following sub-section, an in-depth analysis of how the proposed AiP platform meets the packaging and system-integration requirements for 5G mmWave is given.

a) Low-Cost Requirement

The proposed AiP platform meets the low-cost requirement because of three main reasons:

1) PCB-based materials, interconnects and packaging processes are used for fabricating the platform.
2) Since it is an embedded platform, no additional “interposer” is required. By not using an interposer, the cost of packaging materials as well as the number of process steps required for fabricating the platform are reduced.
3) The fabrication processes of the AiP enable the use of panel-level packaging, through which hundreds or thousands of 5G mmWave modules can be simultaneously manufactured. This greatly reduces cost.

b) High-Performance Requirement

The proposed AiP platform meets all the high-performance criteria outlined in section II, as discussed below.

1) High Gain and Broadband mmWave Antennas Arrays

One of the main advantages of the mmWave band is the large continuous bandwidth it provides, relative to the sub-6 GHz band. To exploit this bandwidth advantage, the antennas must be broadband. To overcome the high channel losses at mmWave frequencies, the antennas must also have high gain. Antenna gain, $G(\vartheta, \varphi)$, is a function of the directivity and efficiency, as given in equation (1).

$$G(\vartheta,\varphi) = D(\vartheta,\varphi) * e_{diel.} * e_{cond.} * e_{mat.} \quad (1)$$

where $D(\vartheta,\varphi)$ is the directivity, $e_{diel.}$ is the dielectric efficiency, $e_{cond.}$ is the conductor efficiency and $e_{mat.}$ is the matching efficiency.

Our proposd AiP platform enables the fabrication and integration of high-gain and broadband antennas by providing the following:

- Dielectric and metallization layers dedicated for integration of the antenna elements, and the feeding network within the platform very close to the antenna elements.
- The flexibility of choosing a) dielectric materials in the antenna layer with smaller relative dielectric constants to increase the directivity, and hence increase antenna gain; b) dielectric materials with smaller loss tangents to minimize the dielectric losses, increase the dielectric efficiency, and hence increase antenna gain; c) thicker and/or wider metallization to minimize the conductor losses, increase the conductor efficiency, and hence increase the antenna gain; d) suitable thicknesses of the dielectric of the antenna layer to enhance the bandwidth of the antenna.
- Very short and low-loss interconnection path with fewer geometrical discontinuities between the frontend chips and antenna to ensure smaller signal reflections, higher matching efficiency, and thus higher antenna gain.

2) EIRP

EIRP is the sum of the antenna gain and output power of the power amplifier minus the losses between the antenna and the amplifier. Our proposed AiP platform ensures very low signal losses between the antenna and the power amplifier chip. Therefore, for the same antenna gain and output power of a power amplifier, our AiP platform enables a higher EIRP.

3) Intra-System EMC

AiP platforms increase the integration density of mmWave frontend modules by enabling compact placement of the frontend components in close proximity to the antenna. However, this compact integration may have a negative impact on the performance of both the frontend components and antenna, and also cause intra-system EMC issues.

The shielding layer in our AiP platform prevents electromagnetic interactions between the fields of the antennas and the integrated mmWave frontend components. This prevents detuning of the characteristics of the antennas and frontend components, and also ensures intra-system EMC.

4) SI

At mmWave frequencies, the geometrical discontinuities along signal paths in AiP platforms may severely degrade SI (i.e., the quality and timing of propagating signals) beyond acceptable limits. To prevent this, our AiP platform provides very short and low-loss interconnection paths with fewer geometrical discontinuities between the mmWave components. This ensures SI between the antenna and the amplifier chips (i.e., chip-to-antenna SI), SI between the different chips (i.e., chip-to-chip SI) and SI between the chips and other front-end components, e.g., phase shifters (i.e., chip-to-component SI).

5) PI

To ensure stable power supply and proper functioning of the mmWave frontend chips, our AiP ensures the integration of decoupling capacitors in close proximity to the chips in the component layer. It also ensures low inductive interconnect paths between the capacitors and chips, so as to reduce voltage drop and minimize the possibilities of PI problems such as simultaneous switching noise (SSN).

6) High-Q Passives for Co-Design of Active mmWave Frontend Transceiver Components

The performance of many active frontend components (e.g., power amplifiers) depends on the Q-factor of the passive components (e.g., inductors) used for the development of these active components [13]. Therefore, one possibility to enhance the performance of 5G mmWave frontend components is to improve the Q-factor of their passive components. To reach this goal, our proposed AiP platform ensures the flexibility of choosing:

- Adequate number of metal layers and dielectric thickness in the re-distribution/routing layer suited for fabricating high-Q passives, without compromising the performance of other mmWave components (e.g., antenna arrays) integrated in the platform.
- Thicker and wider metallization, as well as low-loss dielectrics for the fabrication of high-Q passives.

Furthermore, our AiP platform also ensures the integration of the high-Q passive components in the component layer in close proximity to the mmWave chips, and hence provides very short interconnection paths with negligible parasitic effects between the components.

7) HI

HI enables components or building blocks of a system to be fabricated and optimized using different technologies, and then integrated together to yield optimized system functionality [10]. Our AiP platform ensures the integration of heterogeneous mmWave components (frontend chips, antenna arrays and passive components (e.g., inductors)) in different layers using different technologies (e.g., different materials and metallization thicknesses), chosen to optimize the performance of each component, without compromising the performance of the other components. This leads to an optimization of the performance of the entire 5G mmWave module.

c) Reliability Requirement

Heat dissipated by the mmWave amplifiers in the frontend must be conducted out of the chip to prevent thermo-mechanical reliability issues. For this purpose,

our AiP platform ensures direct thermal path for heat transfer from the chips through the temperature control layer to the system-board and the environment. In the example of the stack-up shown in figure 1, thermal vias are used in the temperature control layer.

d) Scalability Requirement

Our AiP platform ensures the integration of mmWave frontend chips (in the component layer) and passive components (in the redistribution/routing or component layer) directly beneath the antenna array in such a way that the dimensions of the entire frontend module are determined by the dimensions of the fundamental antenna array configuration (e.g., 2X2, 2X4). This enables the frontend module to be systematically up-scaled in both lateral dimensions to address vast range of applications with different power requirements.

e) Miniaturization Requirement

Miniaturization enables future 5G modules to be integrated in many "things" and products around us, and thus enable the vision of connectivity anywhere, anytime from anyone and anything. Our proposed AiP platform ensures miniaturization by not using an interposer and also by eliminating the multilayered configuration typically used between the chip and the antenna in other AiP platforms (e.g., in [6] and [7]).

IV. APPLICATION OF THE NEW AiP PLATFORM FOR DEVELOPMENT OF 5G MMWAVE SYSTEMS

Since our AiP platform meets all the key packaging and system-integration requirements for 5G mmWave, it was applied to develop miniaturized, scalable, low-cost and high-performance 5G mmWave system within the framework of an EU-flagship project, called SERENA. The goal is to develop a 39 GHz 5G mmWave system with 64 elements antenna array for NR base station applications. To develop this system, we first developed a scalable mmWave massive MIMO system-architecture which enables analogue-digital hybrid beamforming. From this architecture, we derived a fundamental building block of the mmWave module. The top layer of this module consist of an eight elements antenna array, with four sub-arrays, as shown in the figure below.

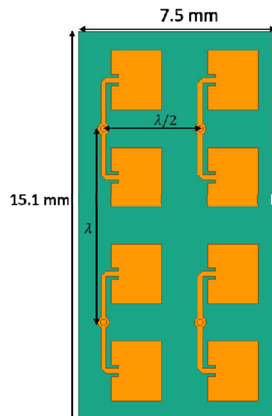


Figure 2: Fundamental array of 5G mmWave module.

Each sub-array consists of two antenna elements/ patches, and is driven by one GaN-based T/R chip from OMMIC. A T/R chip consists of a power amplifier, a low-noise amplifier and a switch. Hence, the eight elements antenna array (i.e., four sub-arrays) are driven by four T/R chips. All these four T/R chips are driven by one SiGe beam-former (BF) chip from INFINEON. Therefore, one fundamental mmWave module consists of one BF chip, four T/R chips, eight elements antenna array and decoupling capacitors required for stabilization of the power distribution network. In order to develop the hardware of this fundamental mmWave module, all the above mentioned mmWave components must be integrated together using an AiP platform. Figure 3 shows a schematic view of the stack-up of the mmWave AiP module on a system-board, used for the development of the 5G mmWave system.

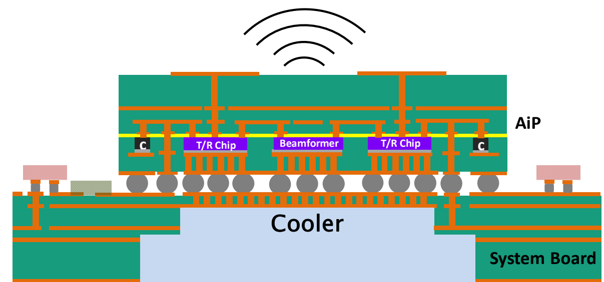


Figure 3: mmWave AiP module on a system-board.

The entire mmWave NR base station system consists of 8 mmWave AiP modules, which in turn consists of 8 BF chips, 32 T/R chips and a 64 elements antenna array. Once one of these mmWave AiP hardware modules is developed, it can then be mounted 8 times on the system-board and connected to the other system components to yield a 5G mmWave systems.

The development of the mmWave AiP hardware module requires thorough electrical and thermal characterization. In the next sections, we discuss RF characterization of the dielectric material of the platform and the integrated antenna sub-array as well as thermal characterization of the module. Finally, we present the fabrication of the module.

V. DESIGN AND MEASUREMENT OF mmWAVE ANTENNA SUB-ARRAY IN THE PROPOSED AiP MODULE

In this section, a 5G mmWave antenna sub-array consisting of two patch elements is designed, fabricated and measured. However, prior to designing the sub-array, the dielectric material of the antenna and re-distribution/routing layers was first characterized in the 39 GHz band. Megtron 7N was used as the dielectric in these layers. For its characterization, fork-shaped microstrip planar resonator structures were modelled, designed on the Megtron 7N substrate and fabricated. The fabricated samples were measured using a vector network analyzer in the 39 GHz band. Based on the measurement results, a relative dielectric constant of ε_r=3.11 and loss tangent $tan\delta$ =0.003 were extracted. These values were then used for designing the antennas.

The top and cross-sectional views of the antenna layer as well as the cross-sectional view of the re-distribution/routing layer are shown in figure 4 and figure 5, respectively. Each of the metallization layers is 25 µm thick. The dimensions of the other parameters are given in these figures. The antenna sub-array was modeled and simulated using HFSS ANSYS. Based on the simulation results, layout files were generated and used for fabrication of the antenna sub-array at Fraunhofer IZM. Figure 6 shows the top view of a fabricated sample. The return loss and radiation characteristics of the fabricated antennas were measured in an anechoic chamber. A comparison of the measured and simulated radiation patterns of the antenna sub-array are shown in figure 7. As can be seen in this figure, very good correlation was obtained between measurement and simulation results of the radiation patterns in both the E- and H-planes. The measured antenna peak gain is 8.25 dBi, which is approximately 0.15 dBi smaller than the simulated gain.

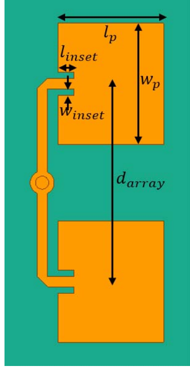


Figure 4: Top view of antenna sub-array (l_p=1.97 µm; w_p=2.3 mm; l_{inset}=0.3 mm; w_{inset}=0.1225 mm; d_{array}=4 mm).

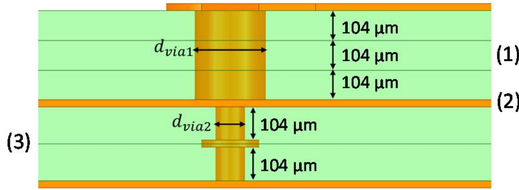


Figure 5: Cross-sectional view of antenna and re-distribution/routing layers; (1) antenna layer; (2) shielding layer; (3) re-distribution/routing layer (d_{via1}=0.3 mm; d_{via2}=0.104 mm).

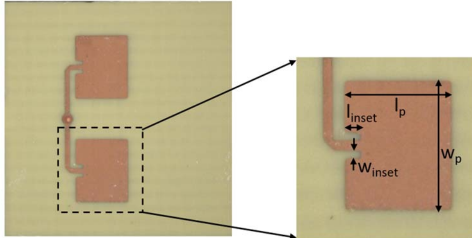


Figure 6: Top view of fabricated antenna sub-array (l_p=1.92 µm; w_p=2.273 mm; l_{inset}=0.304 mm; w_{inset}=0.122 mm; d_{array}=3.96 mm).

A good correlation was also obtained between the measured and simulated return losses, as can be seen in figure 8. The simulated resonance frequency of the return loss is approximately 37.4 GHz, whereas the measured one is shifted to 37.56 GHz. To understand the reason for the shift, we measured the geometrical dimensions of the fabricated antenna using a microscope. This enables us to capture any variation with respect to the design values, which may arise due to fabrication tolerances. Table 1 shows the dimensions of the simulated and fabricated antenna sub-array. As can be seen in table, the length of the fabricated patch is slightly shorter than the simulated patch. This explains why the resonance frequency of the fabricated patch is slightly shifted to higher frequencies.

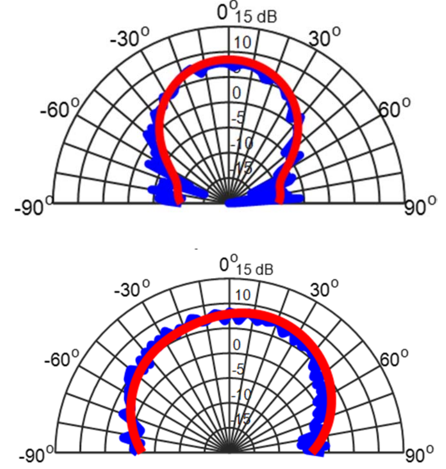


Figure 7: Simulated (red) and measured (blue) radiation patterns of the antenna sub-array: Top: θ-plane, $\varphi = 0°$; bottom: θ-plane, $\varphi = 90°$.

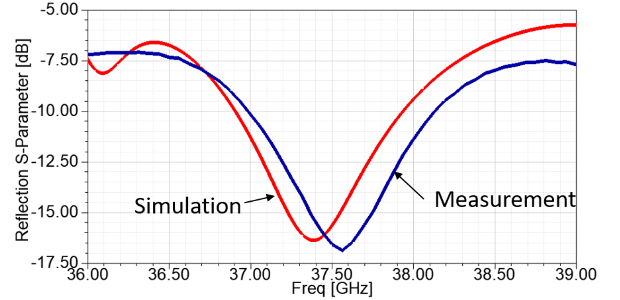


Figure 8: Simulated and measured return losses of antenna sub-array.

Parameter	Simulation	Measurement
l_p	1.97 mm	1.92 mm
w_p	2.3 mm	2.273 mm
l_{inset}	0.3 mm	0.304 mm
w_{inset}	0.1225 mm	0.122 mm
d_{array}	4 mm	3.96 mm
d_{via1}	0.3 mm	0.281 mm
d_{via2}	0.104 mm	0.094 mm

Table 1: Dimensions of the simulated and fabricated antenna sub-array.

It should be noted that the antenna test structures shown in this section were designed to resonate at 37.5 GHz.

VI. THERMAL MODELING AND ANALYSIS OF THE PROPOSED AiP PLATFORM

The thermal resistances *junction-to-board* ($R_{th\ J\text{-}B}$) and *junction-to-case* ($R_{th\ J\text{-}C}$) can be determined

according to the JEDEC standard JESD51 [14]. Since the proposed AiP platform has antenna elements on its topside, the focus of the investigations in this section is on $R_{th\ J\text{-}B}$. The AiP platform was realistically modelled, considering the integrated mmWave components. The four T/R chips, one BF chip, eight antenna elements in the antenna and routing layers, the solder balls and the test board from the JEDEC standard were all included in the simulation model. This test board, according to JEDEC consists of FR4 material and Cu layers. Figure 9 gives an impression of the simulation model having thermal vias beneath the chips for heat conduction. The relevant material properties which are used in the simulations, as listed in Table 2, are obtained from published literature.

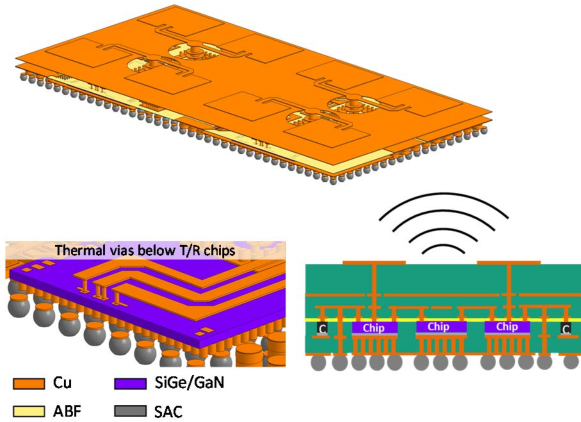


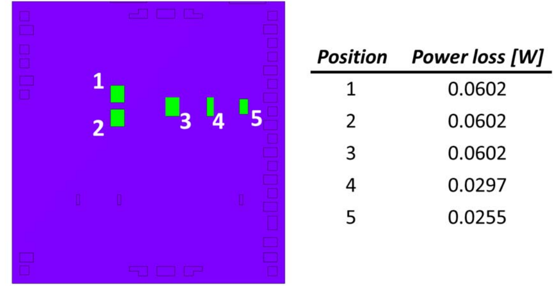
Figure 9: Simulation geometry (top & bottom left) and schematical representation (bottom right) of the AiP platform. The RF PCB and JEDEC testboard are not shown for reasons of clarity.

Material	Thermal conductivity (W/mK)	Source
Copper	403	15
RF PCB	0.42	16
ABF	0.62	16
Silicon	124	15
SAC Solder	60	17
FR4 material	0.35	15

Table 2: Thermal conductivities for thermal simulations.

During operation, the T/R chips and BF chip produce heat due to power loss (P_{loss}). The total P_{loss} of the package, i.e. four identical T/R chips and a BF chip, is normalized to 1 W, allowing an easy evaluation of the R_{th}. The active areas of the T/R chip are considered in the simulation model as shown in figure 10. In addition to the positions, the values of P_{loss} of one T/R chip are listed in this figure. The normalized P_{loss} of the BF chip is 0.0567 W which is uniformly divided over the complete area of the die.

The simulations are conducted according to the JEDEC standard. The defined temperature of the ring style cold plate for the $R_{th\ J\text{-}B}$ is assumed by a 0°C boundary condition on the test board, according to the geometry of the cold plate. Furthermore, convection effects are not considered here, meaning that the worst-case assumption is investigated.



Position	Power loss [W]
1	0.0602
2	0.0602
3	0.0602
4	0.0297
5	0.0255

Figure 10: Location and intensity of the active areas where power loss occurs on one T/R chip.

To determine the R_{th}, the maximum junction temperature and the board temperature, halfway along the longer side of the package are obtained. The R_{th} is calculated as follows:

$$R_{th\ J-B} = \left(T_{junction} - T_{board}\right) * {P_{loss}}^{-1} \qquad (2)$$

Since P_{loss} is set to be 1 W, the change in temperature increase equals R_{th}. The results of the simulation is shown in figure 11. The cross-sectional view displayed in this figure is located at the highest junction temperature in the mmWave chip. The calculated $R_{th\ J\text{-}B}$ is 3.55 K/W.

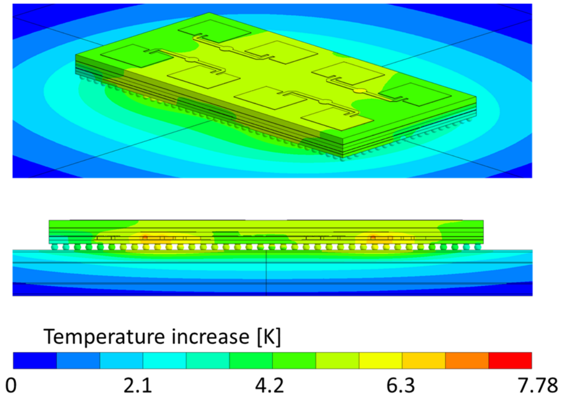


Figure 11: Resulting temperature increase due to 1 W of power loss. The $R_{th\ J\text{-}B}$ of the AiP is 3.55 K/W.

The estimated temperature increase in the used phase can now be calculated by multiplying the total power loss of the package with the $R_{th\ J\text{-}B}$ estimated above.

The results of the thermal simulation can be used manifold. First, different packaging concepts can be compared easily, due to the used JEDEC standard boundary conditions. Secondly, it allows to define the maximum power loss for a given application (environmental temperature, maximum AiP temperature, electrical parameters, etc.). Finally, it allows to determine the possible range of application for a given P_{loss}.

VII. FABRICATION OF PROPOSED AiP PLATFORM

In order to fabricate the AiP platform, the PCB embedding process was modified because of the challenges posed by the mmWave chips to be embedded. Some of these chips, e.g., the GaN T/R chips contain air

gaps, which are not compatible with the conventional bonding pressure for die sintering onto the substrate. Furthermore, they have very thin gold contacts (3 µm), therefore UV-laser drilling through the build-up film while not cutting through the contacts is challenging. After modifications of the fabrication processes, the platform was fabricated using the following steps: First a PCB core (2 copper layers) is fabricated, with a circuity containing the bond pads for capacitors and the mmWave chips. Thermal vias to the reverse side are placed directly under the bond pads of the mmWave chips. Components are mounted onto the core by sintering gluing, embedded into the build-up (prepreg & ABF) and electrically connected by µ-vias. By sequential lamination and structuring of further build-up layers, antenna structures are integrated into the module. On top of the ABF-film and routing layer 100 µm Megtron 7N and 25 µm copper is build-up and connected to the copper structures below by micro-vias.

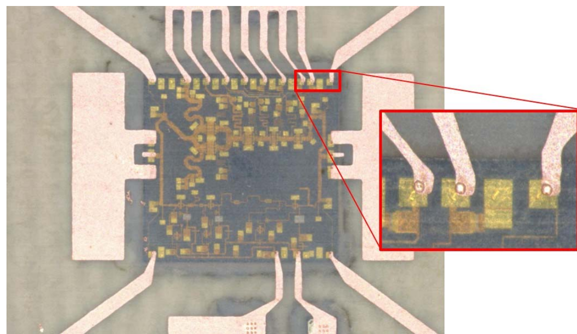


Figure 12: Top view of an embedded T/R chip, connected by plated µ-vias to the copper circuitry.

This copper layer is used as ground plane. Next, a thick build-up consisting of approximately 312 µm Megtron 7N and 25 µm copper for the antenna structures is added. Electrical connections to the copper structures in lower layers are mechanically drilled blind holes with conformal copper metallization. Figure 12 shows an example of mmWave T/R chip embedded in the AiP platform.

VIII. SUMMARY

In this paper, a new AiP platform which meets the key packaging and system-integration requirements for 5G mmWave is presented. We also illustrate the application of this platform for the development of miniaturized, scalable, low-cost and high-performance 5G mmWave systems for new radio (NR) base station applications. RF characterization of the dielectric materials of the platform and the integrated antennas as well as thermal characterization of the platform is discussed. Finally the PCB embedding process used for fabricating the module is presented.

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