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Implementation and Design of FIR Filters using Verilog HDL and FPGA

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Abstract: Digital filters play a major role in Very Large-Scale Integration Technology (VLSI), as most VLSI systems use addition as an integral operation. One such filter is FIR filter, whose basic implementation is achieved by adders. This paper mainly aims at designing a Moving Average 4-tap FIR filter using Verilog HDL and is implemented using Xilinx software and Spartan 6 FPGA kit with the concepts of Multiply and Accumulate (MAC) operation and convolution.

Keywords: VLSI systems; Digital Filter; FIR filter; Linear phase; Impulse Response; MAC operation; FPGA kit

I. INTRODUCTION

Digital filters are those systems that are used for performing certain mathematical operations in signals like discrete time signals in order to change the facets of the signal. There are two main digital filters namely, Infinite Impulse Response (IIR) Filter and Finite Impulse Response (FIR) Filter. FIR filters are generally used whenever there is a necessity for a linear phase characteristic within the given pass band of the filter. This linear phase characteristic is very important requirement as there is only a delay in the input signals but, phase distortion is avoided. Hence, this serves as a major advantage for FIR filters. The applications of FIR filters are mainly involved in biomedical, communication and control due to its easy implementation, stability and best performance. It is also widely used in image processing, video and communication systems.

The major components of a FIR filter are adders and multipliers, so depending upon the value of N which gives the order or the number of taps used in the filter. As this paper deals with the design of a 4-tap filter, the number of multipliers and adders used are lesser compared to higher order filters. Using the concept of MAC unit and convolution, the goal of this paper is to implement this design in the Xilinx software and the Spartan 6 FPGA kit.

II. DESIGN OF FIR FILTER

As the name suggests the impulse response of a FIR filter is of finite duration as it settles down to zero after a limited period of time. The impulse response is also said to be finite as there is no feedback in FIR filter. However, in the case of moving average filter despite the N^{th} sample is fed back every time a new sample is arrived, the impulse response is finite and after the N samples the output will be zero. The output of the filter is the weighted some of the present as well as the previous inputs. When a causal system is taken into consideration, the output depends only the past and present inputs. When a non-causal system is considered then the output obtained is same as the output obtained for the causal system but, with some delay. For an Nth order discrete time FIR filter, the impulse response exists exactly for N+ 1 sample, after which the response settles to zero [1].

The tap of an FIR filter denotes the co-efficient or delay pair. The number of FIR taps often indicates- the calculations required, the memory required for implementation of the filter and to what level filtering can be done. Therefore, it is clear that when there are more taps in a filter there is more stop band attenuation, less ripple and narrower filters can be achieved.

This is a 4-tap filter which means that the order of the filter is 3 and hence the number of co-efficient is 4. The inputs and outputs are chosen to be 8 bits and 16 bits wide respectively. Negative numbers are stored in 2's complement format by the inputs and outputs. The output for a discrete time FIR filter is the weighted sum of the current and a finite number of previous values of the input. This operation is described by the following representation, which defines the output sequence *y(n)* in terms of its input sequence *x(n)*.

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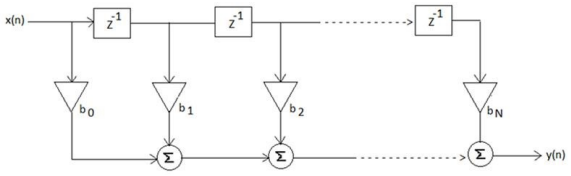

Fig 1. Representation of N tap filter [2].

Fig.1 shows the data flow diagram for N-tap FIR filters. Triangle shape indicates multiplier. The incoming *x[n]* is multiplied with b_0, b_1, b_2, b_3, etc. which are the coefficients. Encircled plus sign symbol shows adders which are used to accumulate the convolution of an *x[n]* where $n = 0,1,2,3$ etc. [2]

N[th] order equation of a FIR Filter is given by,

$$y(n) = b_0x(n) + b_1x(n-1) + b_2x(n-1) + \cdots + b_Nx(n-N) \quad (1)$$

Equation (1) can also be expressed as a convolution of the co-efficient sequence bi with the input signal,

$$y(n) = \sum_{i=0}^{N} b_i x[n-i] \quad (2)$$

i.e., the filter output is a weighted sum of the current and a finite number of previous values of the input [4].

III. LITERATURE SEARCH

In this section, the survey related to the existing literatures on the design of FIR filters using VHDL and FPGA kit has been briefed.

Emmanuel S. Kolawole Warsame H. Ali, Penrose Cfie, John Fuller, C. Tolliver, Pamela Obiomon [1] in paper entitled "Design and Implementation of Low-pass, High-pass and Band-pass Finite Impulse Response (FIR) Filters using FPGA". In this paper the design and implementation of a low-pass, high-pass and a band-pass Finite Impulse Response (FIR) Filter using Spartan-6 Field Programmable Gate Array (FPGA) device is done. The Filter Design and Analysis (FDA) are used to test the filter performance and FIR tools from Math works. The filter order and coefficients are defined using the FDA Tool and for the Simulink simulation the FIR tool is used.

S. Subathradevi and C. Vennila, [2] in paper entitled "Delay Optimized Novel Architecture of FIR Filter using Clustered-Retimed MAC unit Cell for DSP Applications" explains the construction of FIR filter and its design as a delay optimized one. It has been demonstrated by an experiment that the delay reduction is achieved using the reduction in the path delay. Different architectures have been implemented with 3-tap, 4-tap, 5-tap and 6-tap with the input bit size as 4-bit, 8-bit, 12-bit and 16-bit. Using this concept we have described the representation of an N-Tap filter in our paper. We have also designed 4-Tap FIR filter in Direct Form.

Proakis & Manolakis [4], the book entitled "Digital signal processing – Principles Algorithms &Applications" consists of the fundamentals of discrete-time signals, systems and modern digital processing algorithms which helps us understand the basic concepts as well as concepts required for this paper. This book consists of all the concepts required for designing FIR filters which we have been used to understand the topic.

Samir Palnitkar [5], the book titled "Verilog HDL: A Guide to Digital Design and Synthesis" consists of hierarchical modeling concepts, basic Verilog constructs and modeling techniques, and the necessary knowledge to write small models and run simulations. In this paper we have used this book as a reference to develop codes for designing FIR filters using Verilog HDL.

Bahram Rashidi, Farshad Mirzaei, Bahman Rashidi and Majid Pourormazd [6] in paper entitled "Low power FPGA Implementation of Digital FIR Filter based on Low Power Multiplexer Based Shift/Add Multiplier", International Journal of Computer Theory and Engineering. This paper puts forward a design of low power and low delay finite-impulse response (FIR) filter. As of now there are many portable applications that require low power and high throughput. Therefore, low power system design has become a notable performance goal which uses the FIR as an essential component. In the FIR filter, hybrid adders (uses concept of ripple carry adder and carry select adder) and vedic multiplier (performs multiplication hierarchically) are used. Thus, minimizing the power consumption and delay of FIR filter.

Zhang Chi and Guo Li Li [9] in paper entitled "Design of FIR filter with MATLAB and running on FPGA", Applied Science and Technology. vol. 33, no. 6, pp.83. This paper mainly portrays the design of low pass FIR half band filter that is based on MATLAB and implemented using Field Programmable Gate Array (FPGA). The digital down converter in SDR makes use of such half band filters. Adders used in the design are based on the concept of ripple carry adder.

Manuel G. Gericota, Gustavo R. Alves, Miguel L. Silva, Jose M. Ferreira [13] in a paper entitled "Concurrent replication of active logic blocks: A core solution for online testing and logic space defragmentation in reconfigurable systems". In this paper Test Methodologies for Field Programmable Gate Array (FPGA) Based Systems is used to test and diagnose the FPGA faults. An off-line-Built-In Self-Test (BIST) technique that exploits the FPGA to set up the BIST logic and an off-line test methodology based on a non-BIST approach, to test the FPGA CLBs (Configurable Logic Blocks) is used. The FPGA Input/output Blocks (IOBs) are used in application to capture test responses and to test vectors.

IV. DESIGN IMPLEMENTATION OF FIR FILTER

The operation required for designing an FIR filter in direct implementation is called the Multiply and Accumulate operation (MAC). In this type of operation, the co-efficient of the filter is directly multiplied with the

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variable and then added to get the final result. The following expression [4] explains the MAC operation:

$$y = \sum_{k=0}^{N-1} h_{n-k} x_k \quad (3)$$

In case of 1 tap filter, the filter co-efficient h_0 is directly multiplied with variable x_0 and the result is assigned to the output. In a 4-tap filter, the filter co-efficient are multiplied with corresponding variables, the result of 4 multipliers are added and assigned to the result.

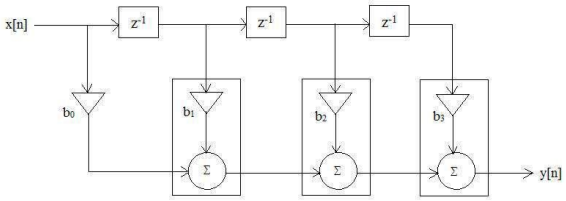

Fig 2. 4-tap FIR Filter (Direct form) [2].

Fig. 2 shows the data flow graph diagram for a 4-tap FIR filter. When the number of taps increases the longest path delay also increases. Also, number of multipliers and adders required in the architecture also increases. The data flow graph shown in Fig. 2 is in direct form [2].

This design implementation of FIR filter has been achieved in Verilog using a software tool Xilinx and Spartan 6 FPGA kit. Xilinx ISE (Integrated Synthesis Environment) is a software tool which is produced by Xilinx. This software performs the analysis and synthesis of the user defined HDL designs. By using this software and the designers in the RTL description to the logic synthesis tool the designs can be described at a very abstract level a new gate level net list can be created. Timing analysis, examining of RTL diagrams, simulation of design reactions to different stimuli and configuration of the target device can be performed by the designer with the programmer.

The system level testing in Xilinx can be performed with ISIM and such test programs should be written in HDL languages. FPGA kit (Field Programmable Gate Array) it is an integrated circuit which is designed to be configured by a designer. Its configuration is usually specified using a hardware descriptive language. The FPGA's have large resources of logic gates and RAM blocks which are used in complex digital computations. The behavior of the FPGA can be defined by the user in a hardware descriptive language or as a schematic design.

All the test programs must be written in HDL languages and the system level testing in Xilinx can be performed with ISIM.

A. XILINX

An integrated circuit which is designed to be configured by a designer is called an FPGA kit (Field Programmable Gate Array). The configuration of an FPGA kit is usually specified using a hardware descriptive language. The large resources of logic gates and RAM blocks in FPGA's are used in complex digital computations. The user can define the behavior of FPGA in a hardware descriptive language or as a schematic diagram as shown in Fig.3.

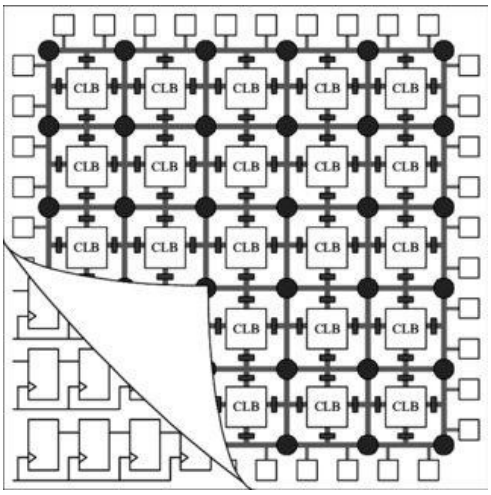

Fig 3. Schematic representation of an FPGA [13].

V. EXPERIMENTAL RESULTS

Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	123	2400	5%
Number of fully used LUT-FF pairs	0	123	0%
Number of bonded IOBs	21	102	20%
Number of BUFG/BUFGCTRLs	1	16	6%

Table 1. Utilization of Devices

The details of the devices used in the Xilinx software which is of Target device- XC6SLX4-3TQG144 belonging to the Spartan 6 family is given in Table 1.

The output for the impulse response of the Moving Average 4-tap FIR Filter for the given input signals has been calculated and is shown in Table 2. This output has been obtained from ISIM Simulator as shown in Fig.4.

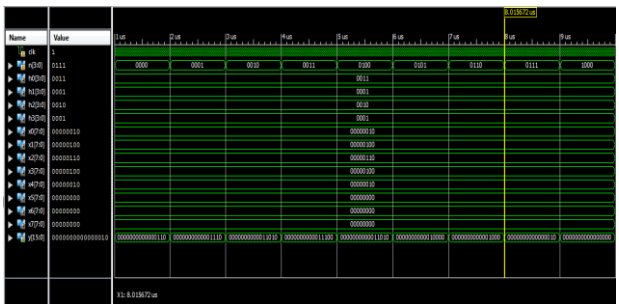

Fig 4. Simulation output

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n	n<0	0	1	2	3	4	5	6	7	n>7
x[n]	0	2	4	6	4	2	0	0	0	0
h[n]	0	3	1	2	1					0
h[0]x[n]	0	6	12	18	12	6	0	0	0	0
h[1] x[n-1]	0	0	2	4	6	4	2	0	0	0
h[2] x[n-2]	0	0	0	4	8	12	8	4	0	0
h[3] x[n-3]	0	0	0	0	2	4	6	4	2	0
y[n]	0	6	14	26	28	26	16	8	2	0

Table 2. Output impulse response of 4-tap filter

VI. CONCLUSION

In this paper, designing of Moving Average 4-tap FIR Filter has been done using Verilog HDL and implemented using Xilinx Software and Spartan 6 FPGA kit. It is found that after the implementation process, less number of devices have been utilized for synthesis and simulation. The main focus of this paper is to introduce a method of implementing an FIR Filter, which is achieved through MAC operation and convolution.

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