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Walking the Route to GHz Solution-Processed Organic Electronics: An HEROIC Exploration

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Limited charge carrier mobility of organic semiconductors, especially for solution-processed polymer thin films, has typically relegated organic electronics to low-frequency operation. Nevertheless, thanks to a steady increase in electronic properties of organics, much higher operation frequencies are feasible, suggesting a possible and appealing scenario where lightweight, cost-effective, and conformable electronics can integrate both sensing and radio-frequency transmitting functionalities, which are the key to unlock pervasive networks of distributed sensors revolutionizing human–environment interaction. Few years ago, it was suggested that gigahertz (GHz) field-effect transistors could be achievable even with solution-based processes. This was the basis for the European Research Council project high-frequency printed and direct-written organic-hybrid integrated circuits (HEROIC), which in the last few years investigated such unexplored path. Here, the authors report their vision toward the achievement of radio-frequency organic electronics mainly with solution-based and scalable processes, with reference to the experience of the HEROIC project and to some of the most notable literature examples. The authors show that the achievement of solution-processable organic field-effect transistors with GHz operation is indeed feasible, but requires considering a carefully revised scenario in which the main role is played by charge injection, together with the geometric overlap, the capacitive parasitism associated to fringing and some constraints on the dielectric layer thickness.

1. Introduction

The growing demand for quality-of-life improvement will be an essential trait of the future society, which will be facing crucial challenges related to aging, healthcare, food, environment, and energy. This goal requires a strong effort in the exploration and development of new concepts, capable of unlocking new possibilities that are not available to date. Within this background, the cost-effective integration of large-area sensing and computational capabilities into common everyday objects will both promote the human–object interaction and will allow to access and collect a vast amount of data from the environment at acceptable costs. This, in turn, will expand the potential to devise and implement new effective strategies to face the challenges we have ahead. This concept also intertwines with the Internet of Things (IoT) framework, whose foreseen potential lies in the implementation of extensive networks of interconnected objects with sensing capabilities, which will exchange the gathered information, cooperate, and interact.

Thus, the implementation of stand-alone devices through integration of electronic functionalities into everyday objects will unlock disruptive advancements by enabling new applications in the fields of personal health monitoring, medical diagnostics, smart energy management, design, and entertainment.

During the past two decades, organic electronics has gained its place within the group of promising technologies to comply with this objective, by virtue of a set of distinctive features.[1] First, organic materials are compatible with flexible and conformable substrates, which facilitate the integration of this kind of electronics onto curved surfaces. Second, such materials can be deposited from solution and with the adoption of fabrication techniques derived from the graphic arts, which enable cost-effective, energy-efficient fast manufacturing of large surfaces integrating electronic functionalities. Third, selected organic materials are compatible with living cells and biological entities, which are an imperative requirement for biomedical applications.

Common requirements for all the envisioned applications are simple signal processing and computational capabilities, which will serve to link sensors and actuators to additional external devices (e.g., mobile phones, cables, readers). The design of organic electronic circuitry to provide these functionalities can be facilitated by following the same guidelines and topologies developed in the field of silicon electronics in the past. In particular, the designers can apply the same ideas at the core of the successful complementary metal-oxide semiconductor (CMOS) technology, which is at the basis of the plethora of electronic applications available nowadays. Similar to silicon

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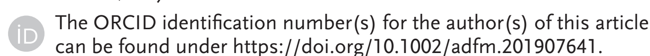
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electronics, organic CMOS-like circuitry requires the availability of organic field-effect transistors (OFET), whose electrical performance will determine the maximum potential achievable in organic-CMOS applications.

The scientific community has put huge effort in the past years to improve some fundamental figures of merit (FoMs) of OFETs and the ideality of their behavior. Examples include the improvement of the effective mobility[2] in OFET structures, closely related to the enhancement of charge injection into the OFET channel,[3] the reduction of the operational voltage,[4] and the reduction of the device footprint.[5] These achievements allowed to demonstrate the applicability of organic electronics to an extensive set of fields: portable flexible displays,[6,7] energy harvesting,[8,9] wearable health monitoring,[10] and biomedical devices.[11]

However, to further enlarge the range of applications that can be targeted, continued effort is necessary in combining these achievements altogether and in boosting additional FoMs. In this respect, increasing the maximum operational speed of an OFET is crucial to unlock a variety of necessary features for new applications, including fast addressing drivers for flexible displays and large sensor arrays, and wireless communication through radio frequency identification (RFID). The ultimate goal is the gigahertz (GHz) operation regime, which would enable new scenarios, such as wireless body-area networks of distributed sensors interconnected with mobile phones via conventional protocols (e.g., Bluetooth).[12]

While megahertz (MHz) operation of OFETs has been shown feasible more than a decade ago,[13] unlocking high-frequency operation above several tens of MHz has been a goal that attracted the scientists and engineers in the recent years. Continuous advancements have been driven by the availability of improved materials with enhanced charge mobility and by the development of high-resolution fabrication techniques facilitating downscaling. Recently, a route to achieve GHz-range operation of OFETs has come into sight and has become an argument of discussion.[14] Within this frame, the HEROIC European Research Council project, which sees the direct involvement of the authors, is partaking in the exploration of this route, aiming at filling the gap between low-operation frequencies of printed, organic flexible electronics and the high-frequency regime, fabricated by means of maskless and scalable processes in order to retain low temperature manufacturability of cost-effective large area electronics on plastic. This challenge requires to address and combine multiple aspects: 1) the development of scalable high-resolution processes for the patterning of functional inks; 2) the development of printable or solution-processable dielectrics with high areal capacitance; 3) the improvement of the control of charge injection and transport in printed semiconductors; and 4) the development of advanced printed and direct-written transistors architectures with low parasitic capacitances for high-speed operation.

In this progress report, we will review the advancements achieved by the community toward GHz operation of OFETs, with particular attention to the aspects related to solution-based and direct-writing fabrication processes, together with collecting the insights gathered in the course of our research in the frame of HEROIC. We aim to present the existing challenges to be addressed to achieve GHz operation, while at the same time providing the community with additional insights and reviewing some promising options for overcoming these barriers.

In Section 2, we illustrate the aspects related to high-speed operation of OFETs and its characterization, with an overview of the relevant FoMs and of the state-of-the-art transistor performance. Afterwards, in Section 3, we describe how a simple approach based on the transistor parameters (i.e., charge mobility, channel length, parasitic overlap) must be integrated with additional considerations in order to devise a scheme to reach GHz operation. In practice, these considerations constitute a set of challenges requiring to tailor the strategies to achieve high-frequency operation: 1) the achievement of high

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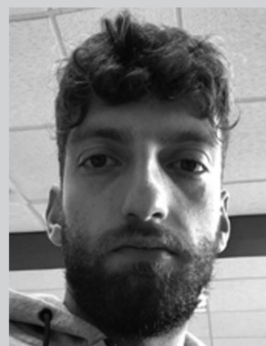

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effective charge mobility in the OFET structures, which will include the strong optimization of charge injection into micron-sized channels; 2) the development of high-resolution printing or direct-writing techniques, suitable for the future upscaling to industrial manufacturing; 3) the downscaling of the thickness of the dielectric layer, with an attention to the selection of appropriate materials for high-frequency and upscalable fabrication techniques; 4) the implementation of strategies to reduce the capacitive parasitism without negatively affecting the transistor performance; and 5) the correct management of heat dissipation in downscaled devices, which is particularly problematic for plastic substrates and functional materials characterized by low thermal conductivity. In the concluding section, we show that the achievement of solution-processable OFET with GHz operation is indeed feasible, but requires considering a carefully revised scenario in which the main role is played by charge injection, together with the geometric overlap, the capacitive parasitism associated to fringing and some constraints on the dielectric layer thickness.

2. High-Speed Operation: FoMs and State-of-the-Art OFETs

This section is dedicated to introduce the established FoMs for the evaluation of the maximum operational speed of transistors, to illustrate the available and most commonly used measurement techniques and, finally, to quickly review the recent improvements in terms of operational speed of OFETs that have been demonstrated in the literature.

There is no unique FoMs for high-speed operation of OFETs that unequivocally quantifies the device performance. Sometimes, the adopted FoMs are related to the time domain (usually in the field of digital electronics),[15] while other times, they are related to the frequency domain (usually for analog electronics).[16,17] What FoM to adopt is a choice depending on the application or on convenience in terms of characterization complexity. Here, we consider three relevant FoMs for OFETs: the transition frequency, the maximum oscillation frequency, and the intrinsic delay time.

The transition frequency f_t (unity-gain frequency) is a small-signal FoM defined as the frequency at which $\frac{|i_d|}{|i_g|}=1$, where i_g is the small-signal gate current and i_d is the small-signal drain current. From such definition, for the case of OFETs, a simplified analytical expression linking f_t to the device transconductance (g_m) and the total capacitance between the gate electrode and small-signal ground (C_g) can be derived, which reads[18]

$$f_t = \frac{g_m}{2\pi C_g} \quad (1)$$

f_t represents the maximum frequency at which it is possible to obtain current gain with a transistor.

The transition frequency does not take into account the influence of the gate resistance and output conductance, which are also determining the high-frequency behavior of a transistor. In particular, even if the current gain is 1 at f_t, the transistor might still be able to provide power amplification, depending on the matching conditions between input and output impedances. This information is provided by the maximum oscillation frequency f_{max}, which identifies the boundary between a passive and an active network, and is defined as the frequency at which the unilateral power gain is unity under matched-impedance conditions. In a simplified expression,[19] f_{max} depends on the transition frequency, on the resistance of the gate electrode R_g, and on the gate-drain capacitance C_{gd}: $f_{max} = \left(\frac{f_t}{8\pi R_g C_{gd}}\right)^{0.5}$. In the context of organic electronics, f_{max} is neither measured nor calculated in the wide majority of cases, and it is even not possible to reanalyze the literature since the values for R_g are rarely reported. However, compared to f_t, the maximum oscillation frequency is a more realistic FoM for assessment of the transistor frequency performance in circuital applications, since it accounts for real signal amplification.[20,21]

In the literature related to OFETs, the most reported FoM is the transition frequency. The most frequently adopted characterization techniques for f_t can be referred as “direct measurement,” consisting in measuring both the small-signal AC gate current i_g and the small-signal AC drain current i_d as a function of frequency. The measurement of f_t then follows easily from its definition, and the transition frequency can be evaluated in a plot as the frequency corresponding to the crossing point between the i_g and i_d curves. Unfortunately, the maximum bandwidth of the majority of these methods is intrinsically limited to a value below few MHz. This limitation is related to the parasitism introduced by the characterization setup itself and, only in few cases, the measurement bandwidth was extended to few tens of MHz by adopting inductive probes. Consequently, f_t of the most performing OFETs to date was often determined via extrapolation from the data obtained at low frequency, where parasitism is negligible or can be easily accounted for.[22–25] In the few cases in which inductive probes were used,[26,27] f_t values around 20 MHz have been measured without extrapolation. However, even in this case, the maximum setup bandwidth is still limited and prevents the access to higher frequency measurements.

Therefore, it is not possible to rely on direct measurement methods for characterizing the upcoming organic high-frequency (100 MHz–1 GHz) devices. For this reason, two-port scattering parameters (S-parameters),[28] adimensional quantities which relate the AC currents and voltages between the drain and the gate contacts, become essential also for organic FETs. They are determined with resistive terminations, which obviate the difficulties involved in obtaining the broadband open and short circuit conditions and provide stable and reliable boundary conditions, allowing to widen the measurement bandwidth up to the GHz range, and well above. Starting from them, a series of parameters can be mathematically computed, such as admittance parameters (Y-parameters), which are useful to extract physical device parameters, for example, device capacitances. This method was applied successfully for polymer FETs, measuring successfully an f_t of 19 MHz without extrapolation.[29]

Both f_t and f_{max} are valid for the small-signal operation regime, while digital electronic circuits operate with large signals. In this regime, the dynamic performance can be characterized in the time domain, where the intrinsic delay time τ_d is typically adopted to evaluate the time for an input signal to propagate to the output of a transistor.[19] A simplified

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Table 1. Selected results in the literature for high-frequency organic transistors and circuits.

References	f_t [MHz]	τ_p [µs]	Low voltage[a)]	Flexible substrate	Maskless fabrication	Main technological approach
Perinot and Caironi[25]	14.4	–	7 V	PEN	Yes	Femtosecond laser—Printing
Giorgio and Caironi[29]	19	–	X	X	Yes	Femtosecond laser—Printing
Kitamura and Arakawa[23]	27.7	–	X	X	X	PL—EV
Kheradmand-Boroujeni et al.[30]	40 (pulsed)	–	8.6 V	X	X	EV
Uno et al.[31]	25	–	X	X	X	PL—EV—Single-crystal
Uemura et al.[24]	20	–	X	X	X	PL—EV—ALD—Spin-coating
Nakayama et al.[27]	19	–	10 V	X	X	PL—EV—ALD
Noh et al.[13]	1.6	–	8 V	X	Yes	Spin-coating—Printing
Kitsomboonloha et al.[32]	1.92	–	X	PEN	Yes	Printing
Yamamura et al.[33]	20	–	X	X	X	PL—EV—ALD—Printing
Higgins et al.[34]	3.3	–	X	Plastic	Yes	NIL—Printing—EV
Borchert et al.[35]	6.7	79×10^{-3}	–3 V or –4.4 V	PEN	X	Stencil lithography—EV
Stucchi et al.[36]	–	1.3×10^{3}	10 V	PEN	Yes	Printing—CVD
Takeda et al.[37]	–	770	10 V	Parylene	Yes	Printing—CVD
Takeda et al.[38]	–	1.1×10^{3}	10 V	Parylene	Yes	Printing – CVD
Ante et al.[39]	–	230×10^{-3}	4.2 V	X	X	EV
Fukuda et al.[40]	–	6.9×10^{3}	X	Teflon	X	EV—CVD
Mandal et al.[41]	2×10^{-3}	31	X	PEN	Yes	Printing
Heremans et al.[42]	–	0.19	X	PEN	X	EV
Ogier et al.[43]	1.08	93×10^{-3}	X	X	X	PL—EV—Spin-coating

–, not reported; ALD, atomic layer deposition; CVD, chemical vapor deposition; EV, evaporation; PEN, polyethylene terephthalate; PL, photolithography; X, not applicable.
a)Bias not above 10 V.

definition is $\tau_d = C_g \frac{V_g}{I_{ds}}$, where V_g is the gate voltage and I_{ds} is the drain-source current, highlighting τ_d as the time needed to charge the gate capacitance with the current driven by the transistor.[15,20] In large-signal circuit operation, however, the time delay is difficult to calculate since it depends on the operational regime of the transistor. From the experimental point of view, a modified definition of delay time is used, derived from the propagation delay τ_p of CMOS ring oscillators (ROs).[15,19] A RO is a cascaded combination of an odd number of inverter stages put together into a closed-loop chain, and the average propagation delay through a single stage can be derived from the measurement of the frequency of the oscillation of the ring. If the number of delay stages is N, the oscillation frequency of the ring is $f_{RO} = 1/(2N\tau_p)$ and the propagation delay can be easily derived.

We summarize in **Table 1** a selection of the best results reported in the literature for organic transistors and circuits,[13,23–27,29–43] in terms of f_t or τ_p, while data for f_{max} are generally not available in the literature of OFETs. In our summary, we not only try to select the best achieved results in the literature, but we also aim at emphasizing some selected features of interest for the future applicability of organic electronics to real-life examples and its ease of scalability to industrial manufacturing. These features include low-voltage operation, fabrication on flexible substrate, and exclusive adoption of processing techniques that do not require the use of masks.

Overall, the results achieved by the community in the recent years have demonstrated that operational frequency in excess of 10 MHz is now established, and in several cases, this is also combined with maximum bias voltages below 10 V, promoting the compatibility with flexible batteries and energy harvesters. The achievement of this performance on flexible substrates has also been shown to be at reach, with a set of instances where OFETs and circuits were fabricated on plastic or paper. However, the examples where all the previous aspects were combined with upscalable, solution-based fabrication methods are rare.

As of now, the achievement of high-frequency operation (100 MHz–1 GHz) organic electronics is in sight,[14] and it will unlock an extensive set of new applications. However, a feasible route must be devised to achieve such performance through a cost-effective, efficient process flow.

3. Open Challenges in the Route to GHz Organic FETs

To date, the main guideline for the formulation of the roadmap to high-frequency OFETs has been based on a simple way to express Equation (1) in order to conveniently connect the physical, geometrical, and operational parameters of an OFET to f_t. By substituting in Equation (1) $g_m = \mu C_{diel} \frac{W}{L}(V_{gs} - V_T)$ and $C_g = C_{gd} + C_{gs}$, where $C_{gd} = WL_{ov}C_{diel}$ and $C_{gs} = WC_{diel}(\alpha L + L_{ov})$, the following equation is obtained:[18]

$$f_t = \frac{\mu\left(V_{gs} - V_T\right)}{2\pi L(\alpha L + 2L_{ov})} \tag{2}$$

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where μ is the charge carrier mobility, V_{gs} is the gate-source voltage, V_T is the transistor threshold voltage, L and W are the channel length and width, respectively, C_{diel} is the areal capacitance of the dielectric layer, and L_{ov} is the geometrical gate to source/drain overlap length. α is a parameter between 2/3 and 1 that can assume different values according to the operation regime of the transistor and varying with the bias-voltage dependence of the mobility.[44,45] In the following, we chose to give a conservative estimation for f_t and set $\alpha = 1$, which corresponds to approximating the channel capacitance with the parallel-plates (PP) model.

The above equation allows to readily identify the relevant knobs to be tuned for the enhancement of the speed performance of transistors. Of course, the geometrical dimensions of the device must be appropriately downscaled: the reduction of L_{ov} decreases the overlap parasitic capacitance between gate and source/drain electrodes and, more importantly, the reduction of the channel length L intervenes both in increasing the transconductance and in decreasing the capacitance of the channel area. The parameter μ, indicating charge mobility, should be regarded as an effective parameter, representative of the technology/device. In the following, we refer to such effective mobility as μ_{eff}, which not only includes the contribution of the intrinsic charge mobility of the semiconductor layer (μ_{int}) but is also affected by other implementation-specific limiting factors (e.g., charge injection). The bias voltage, instead, cannot represent a mean for achieving high-frequency operation, but should be considered as a specification defined by the target application: while some use-cases allow for high supply voltage, the majority of portable, stand-alone devices require the compatibility with thin-film power sources or energy harvesters. Following such considerations, some authors have recently reported the voltage-normalized transition frequency f_t/V alongside with the simple f_t.[25,46] Since it encompasses the OFET speed performance only in terms of geometrical and physical parameters, f_t/V can be considered as a more convenient mean for the comparison of different technologies.

To assess whether high-frequency operation in the 100 MHz–1 GHz range is possible, we start from the simplified picture illustrated above and use Equation (2) to calculate the f_t of OFETs for a set of different channel lengths, electrode overlaps, and charge mobilities. We chose to present the data for a bias voltage of 10 V, which we believe can be set as an upper boundary to comply with the requirements of stand-alone, portable devices presented above.

Results of these over simplified calculations, shown in **Table 2**, provide us at least with a promising starting point: OFET operation at frequencies in excess of 100 MHz and low bias voltage of 10 V is indeed possible with the adoption of materials and technologies that have already been demonstrated to date, albeit in independent works. This includes high-mobility semiconductors with μ in the range 1–10 cm^2 V^{-1} s^{-1} and fabrication methods with resolution down to the micron-scale. In addition, also the more challenging GHz operation is within reach with the most performing materials and techniques available nowadays.

However, despite the approach based on Equation (2) has driven the success of enhancing the f_t of OFETs from the kHz to the MHz regime, the first demonstrations of transistors in the tens of MHz range have started to highlight how a number of aspects cannot be neglected anymore. In other words, the first-order model above is not sufficient for the next stages of the roadmap for high-frequency OFETs. Most part of the reason lies in the fact that there is a large interplay between many of the transistor parameters: the geometrical dimensions, the effective charge mobility, the operational voltage, the properties of the dielectric layer and of the semiconductor/dielectric interface are intertwined, and their enhancement cannot be approached separately. Moreover, the impact of this interplay is more severe as the critical dimensions shrink and the charge mobility improves.

Table 2. Calculated transition frequencies for OFETs with the indicated channel lengths L, overlap length L_{ov}, and effective mobility μ, for a supply voltage of 10 V.

L [µm]	L_{ov} [µm]	Mobility [cm^2 V^{-1} s^{-1}]		
		1	5	10
2	2	13 MHz	66 MHz	133 MHz
1	2	32 MHz	159 MHz	319 MHz
1	1	53 MHz	265 MHz	531 MHz
1	0	159 MHz	796 MHz	1592 MHz
0.8	0	249 MHz	1244 MHz	2488 MHz
0.6	0.3	221 MHz	1106 MHz	2212 MHz
0.5	0	637 MHz	3185 MHz	6369 MHz

As a result, the simple adoption of materials and/or fabrication methods whose high performance (i.e., charge mobility or critical resolution) has been demonstrated in contexts outside the case of high-frequency transistors (which require optimized, specific architectures) is neither sufficient nor a good predictor of the achievable improvement in f_t.

Thus, in order to draft a roadmap for high-frequency OFETs, the simple perspective illustrated above must be integrated with additional elements. In this section, we aim to give insight into a selection of aspects that we consider as the most relevant to this goal and for the improvement of the operational frequency of OFETs into the 100 MHz–1 GHz range. We discuss a set of five main aspects in the form of challenges, by collecting the evidence and investigations already available in the literature and by providing, for some of them, some original analysis stemming from our experience in the frame of the HEROIC project. In this respect, we give particular attention to the problems and solutions related to solution-based and direct-writing fabrication methods, by virtue of their suitability for the upscaling to mass manufacturing.

3.1. High Effective Mobility in Downscaled Transistors

One of the fundamental requirements to attain high-frequency operation in the 100 MHz–1 GHz regime is the implementation of transistors exhibiting high charge mobility, in the 1–10 cm^2 V^{-1} s^{-1} range. Achieving this goal requires considering multiple aspects: primarily the availability of materials and fabrication methods to deposit active layers exhibiting high

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intrinsic mobility and second, the fact that charge injection can drastically limit the effective charge mobility into aggressively downscaled devices. In this section, we do not comprehensively review the vast literature available about the physics of charge mobility and injection in organic semiconductors, but we aim at highlighting the main factors and identifying the most promising strategies to retain high effective mobility into downscaled, micron-size OFETs for high-frequency operation, fabricated with scalable techniques.

A multitude of works has reported the availability of a variety of approaches for depositing high-performance active layers, yielding measured μ_{eff} in a suitable range for achieving, in principle, GHz OFETs. However, the parameter μ_{eff} is intrinsically linked to the specific device implementation and to the experimental conditions, such as the device bias point. Thus, care should be taken when assuming that high performance can be readily replicated in different contexts compared to the one where it was first reported.

The first aspect to be considered refers to a circumstance occurred in the recent years, known as the "mobility hype."[2] In the past years, an increasing number of works have reported mobility values exceeding 10 cm^2 V^{-1} s^{-1} for organic semiconductors, measured through OFET structures and extracted using the gradual channel approximation (GCA) model, the validity of which has later become argument of discussion. In particular, a number of authors have debated the correctness of the use of such extraction method in actual instances where some of the highest mobility values were measured, identifying a certain number of recurring patterns in the data and in the extraction methods that substantially invalidate an important number of high mobility claims.[47–51] In practice, the validity of the GCA can be compromised owing to poor charge injection into the semiconductor and to the dependence of charge injection on the voltage applied to the electrodes. A distinctive indication of the onset of these issues is the presence of features now known as "kink" or "double slope."

Paterson et al. have recently reviewed the literature from the past years for high-mobility, solution-processed organic semiconductors.[2] They identified how a fraction as high as 55% of the works, since when mobility started approaching 1 cm^2 V^{-1} s^{-1}, contains data appearing to deviate from the GCA transistor model (**Figure 1**a). This, in turn, poses a high risk for overestimation of the reported figures for the mobility.

In the context related to high-frequency OFETs, this aspect drives the first consideration: despite having seen in the

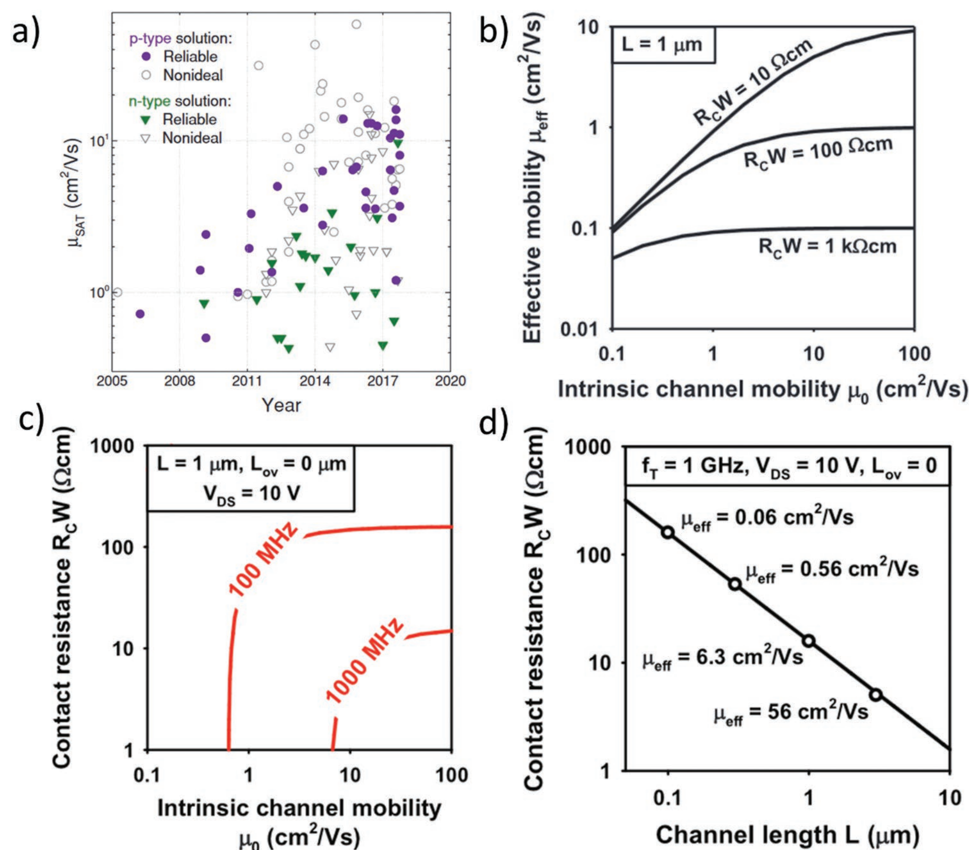

Figure 1. a) Solution-processed mobilities approaching 1 cm^2 V^{-1} s^{-1}, by carrier type and data quality, according to Paterson et al. Reproduced with permission.[2] Copyright 2018, Wiley-VCH. b) Effective charge mobility degradation for different contact resistances, c) calculated f_t for given values of intrinsic charge mobility and contact resistance, d) maximum acceptable values for R_cW to achieve GHz operation of OFETs with a given channel length L, alongside with the corresponding effective mobility calculated for the corresponding parameters. b–d) Reproduced with permission.[14] Copyright 2018, Wiley-VCH.

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literature a wide number of options in terms of materials and techniques for organic semiconductors with an intrinsic mobility in the range 1–10 cm^2 V^{-1} s^{-1}, in reality the size of the available set of choices has been distorted by the mobility hype. In particular, the reported values for the mobility in several works cannot be assumed as good estimators of the μ_{int} achievable with a specific choice of materials/techniques. On the other hand, however, an encouraging increasing trend of the genuine charge mobility exhibited by organic semiconductors is confirmed by the same survey. More importantly, it is not limited to the use of single-crystal or vacuum-evaporated materials, and some options relying on fast solution-processing techniques are available, based for example on small-molecule/polymer blends.

Nonetheless, high mobility active layers are typically demonstrated in DC, proof-of-concept transistor structures, not optimized for high-frequency operation, one of the distinctive features being the use or relatively long channels. Therefore, to enable high-mobility active layers in micron-scale transistors, the availability of performing materials and processes must be combined with efficient charge injection from the contact electrode into the OFET channel. This consideration is very well known and has been extensively studied: the origin of possible limitations in charge injection may be related to energetic barriers, charge trapping at the electrode or at the dielectric interface. These effects are generally comprised into the concept of contact resistance (R_c), which condenses such charge-injection limitations into a single number. As of now, several models and mathematical tools have been developed to describe R_c and to formulate strategies to limit its impact. The interested reader could find additional information in several thorough reviews.[3,52,53]

In the context of high-frequency OFETs, a major contribution on this topic has recently been presented by Klauk,[14] who discussed the requirements in terms of R_c given a target transition frequency of 1 GHz and for different variations of the intrinsic charge mobility and device channel length. First he showed that, for micron-sized channels, width-normalized contact resistances (R_cW) in the 10–1000 Ωcm range can severely degrade the effective charge mobility compared to its intrinsic value (Figure 1b). In particular, retaining effective mobilities in the 1–10 cm^2 V^{-1} s^{-1} range into OFETs with L = 1 µm requires R_cW in the 10–100 Ωcm range, regardless of how much the intrinsic charge mobility exceeds the effective mobility. In terms of f_t, these considerations are highlighted in Figure 1c: for GHz operation of OFETs, both an intrinsic charge mobility in the 1–10 cm^2 V^{-1} s^{-1} range and R_cW below the 10–100 Ωcm range are needed, for a reasonable selection of the transistor geometrical and electrical parameters (L = 1 µm, geometric overlap L_{ov} = 0 µm, drain-source voltage V_{DS} = 10 V). Such requirement on R_cW can be slightly relaxed with the reduction of the channel length, but cannot be compensated by boosting the intrinsic charge mobility: even if an unrealistic intrinsic mobility of 10^4 cm^2 V^{-1} s^{-1} is chosen, R_cW should still remain below 100 Ωcm to obtain GHz-range operation (Figure 1d).

Overall, the considerations made by Klauk highlight a fundamental guideline: at the relevant channel lengths (1 µm and below) and voltage bias for high-frequency OFETs, when the intrinsic mobility exceeds several cm^2 V^{-1} s^{-1}, the effective mobility (and, in turn, the operational frequency) is almost entirely determined by the contact resistance. In other words, to exploit high-mobility active layers, it is paramount to direct the effort into the reduction of R_cW.

There are a multitude of factors concurring into determining the charge injection performance, and thus the contact resistance. Among these, a major role is played by the architecture of the OFET device (staggered or coplanar). A large set of theoretical and experimental demonstrations indicate that staggered architectures exhibit lower contact resistances compared to their coplanar counterparts.[53] This can be explained by the fact that in staggered configurations, the charge injection takes place from an extended area, in contrast to coplanar arrangements where charges are injected from the contact edge. By virtue of this advantage, in the following, we limit our considerations to staggered structures only. It is, however, important to remark that it was recently shown, both via simulations[54,55] and experimentally,[56] how coplanar architectures may exhibit contact resistances lower than 30 Ωcm and below the ones exhibited by the corresponding staggered configurations if certain conditions are met. One of the most important factors in achieving such regime is the adoption of a very thin dielectric layer (below few tens of nanometers). In such case, coplanar structures become a competitive candidate for optimized, low contact resistance devices, allowing also a more effective management of the capacitive parasitism, owing to the fact that injection properties are not strongly related to the geometrical electrode overlap.

In staggered architectures, charge injection is described via the well-established current-crowding model, according to which R_cW can be expressed as[57]

$$R_cW = \sqrt{\rho_c R_{sh}} \coth\left(\frac{L_{OV}}{L_T}\right) \tag{3}$$

The above equation links R_c on the following set of geometrical and electrical parameters for the device: L_{ov} is the overlap length between the gate and the source-drain electrodes, R_{sh} is the sheet resistance of the accumulated transistor channel, and ρ_c is the specific contact resistance, a parameter depending both on the interfacial properties between the electrode and the semiconductor, and on the bulk transport properties across the semiconductor. $L_T = \sqrt{\frac{\rho_c}{R_{sh}}}$ is a parameter known as transfer length, and represents the critical size of the injection area, from which 63% of the charges are injected into the channel. For simplicity, in our derivation in the following, we assume that the predominant component of the total R_cW of the device is associated to the source electrode, where the charges need to overcome an energetic barrier in order to be injected into the semiconductor. Thus, L_{ov} in Equation (3) only represents the geometrical overlap of the source electrode. By doing so, we explicitly assume that the interfacial component of ρ_c, which is active only at the source/semiconductor interface, is the limiting factor for injection, while the bulk transport component, developing in the bulk region of the semiconductor close to both source and drain electrodes, is negligible in comparison. This is in agreement with experimental observations for appropriate selection of architectures and semiconductors with high

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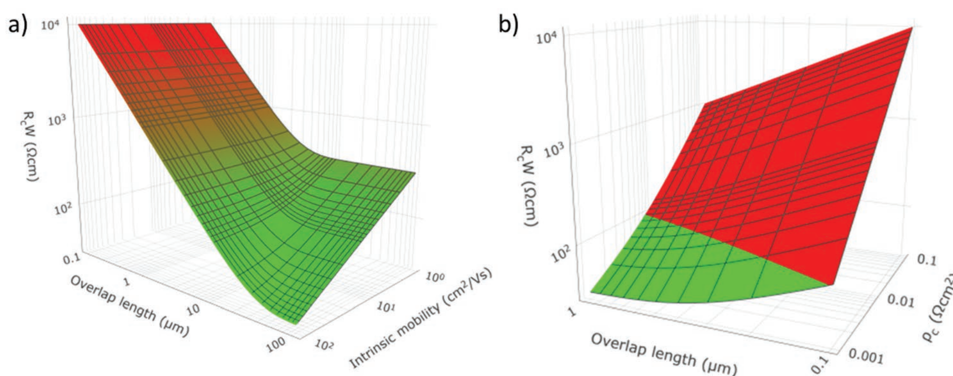

Figure 2. a) R_cW versus overlap length L_{ov} and intrinsic mobility μ. b) R_cW versus overlap length L_{ov} and specific contact resistance ρ_c (values for $R_cW < 100$ Ωcm are colored in green).

bulk mobility.[58] An analogous assumption was also used to fit experimental data with a semi-phenomenological model, yielding excellent agreement with the measurements.[59]

Now, it is interesting to draw some considerations on the main contributing factors for R_cW in the range of parameters useful for GHz operation. In particular, whether the interfacial properties (encompassed in ρ_c) or the extended channel area for injection (encompassed in R_{sh}) is predominant for reasonable geometrical and physical parameters of the OFETs. The sheet resistance of the accumulated channel can be expressed as $R_{sh} = (\mu_{int}C_{diel}(V_g - V_T))^{-1}$, where μ_{int} is the intrinsic mobility of the semiconductor, C_{diel} is the areal capacitance of the dielectric layer, V_T is the threshold voltages of the device, and V_g is the applied gate bias. Despite the previous expression introduces the intrinsic charge mobility as a contributor to the determination of the contact resistance, through the resistance of the accumulated channel, we remark that this does not include all the dependencies of R_cW on the mobility, which also contributes to the interfacial and bulk transport properties, expressed in this model via ρ_c.[53] However, the field-effect mobility in the channel is likely to differ from the value of the mobility at play in the interfacial and bulk processes, due to the generally different morphology of the semiconductor in the vicinity of the electrodes and due to charge-density dependence of the mobility. Therefore, the following dependencies of R_cW versus μ should be considered only with the aim to assess the relative importance of R_{sh} and ρ_c in determining R_cW.

By combining the previous expression for R_{sh} and Equation (3), we can plot the value of R_cW versus μ and L_{ov} and identify the predominantly contributing factors for the ranges of parameters of interest for high-frequency OFETs. The result of the calculations is shown in **Figure 2**a, for $V_g = 10$ V, $V_T = 0$ V, $C_{diel} = 100$ nF cm^{-2}, and $\rho_c = 0.1$ Ωcm^2.

Two regimes for R_cW can be identified: when L_{ov} is large, the contact resistance decreases with the increase of μ; when L_{ov} is short, R_cW does not depend on the mobility (via R_{sh}) and is solely determined by the overlap length. This poses a problem for the implementation of architectures optimized for high frequency, which require the minimization of the overlap length in order to minimize the parasitism. Such trade-off between efficient charge injection and capacitive parasitism has been already identified in the past.[39,60] Here, we substantiate further this aspect by highlighting that, for the relevant values for 100 MHz–1 GHz operation (i.e., L_{ov} below 1 μm) and for reasonable geometrical and physical parameters, R_CW is within a regime where the intrinsic mobility does not contribute to enhancing charge injection (at least via R_{sh}).

Therefore, in this range of parameters and for the reasonable values adopted in the simulation, the achievement of low contact resistance must be approached through the reduction of ρ_c. With the same model, we have calculated the achievable R_cW for different values of L_{ov} and ρ_c, with $\mu = 1$ cm^2 V^{-1} s^{-1} and the other parameters as in the previous simulation. The results are shown in Figure 2b, where the data points corresponding to R_cW below 100 Ωcm are highlighted in green. For 0.1 μm $< L_{ov} <$ 1 μm, which is a relevant range for high-frequency OFETs, the calculations show that ρ_c is required to be below 0.01 Ωcm^2 to achieve $R_cW < 100$ Ωcm. Unfortunately, the achievement of such low ρ_c is still a challenge: the best results achieved in the literature, to the best of our knowledge, have shown figures in the 0.1–0.01 Ωcm^2 range.[3] A thorough review is, however, complicated by the fact that most works only report R_cW. Nonetheless, even in terms of R_cW, the lowest demonstrated values are rarely below 100 Ωcm.[3,14,33,52,56] To date, the lowest reported contact resistance for an organic device was 10 Ωcm for a transistor integrating an electrolyte dielectric in a staggered architecture.[61] The authors attribute such enhanced performance to the diffusion of the ions from the dielectric into the semiconductor area, where they assist the injection close to the contact region. However, schemes based on ion movement are not applicable to high-frequency operation, due to the intrinsically low ionic mobility, which would not allow operation in the 100 MHz–1 GHz range. When excluding OFET implementations based on ionic doping, a low R_cW of 29 Ωcm has been reported, obtained for a coplanar structure by virtue of a low dielectric layer thickness of 3 nm.[56] The key requirement for achieving such performance is the low dielectric thickness, which was realized by growing a self-assembled monolayer (SAM) dielectric on a Al_2O_3 layer deposited via atomic layer deposition (ALD). In another instance, an R_cW of 46.9 Ωcm was obtained in a staggered structure where two-layered organic crystalline semiconducting films were deposited from solution.[33] The authors also suggest that their deposition technique is promising in view of scalability to large area.

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Thus, a strengthening of the solution-based strategies for the reduction of ρ_c needs to be devised in order to access GHz operation of solution processed OFETs. The factors concurring to the determination of ρ_c are twofold: one component is related to charge transport across the bulk of the semiconductor, from the electrode to the channel area of the transistor, a second component is related to the properties of the electrode/semiconductor interface promoting/hampering charge injection. In addition, both of these contributions also depend non-linearly on the electric field in the vicinity of the contact.[59] The former aspect can be approached by reducing the resistance of the region that the charges have to travel to access the channel from the electrode (where the adoption of high-mobility semiconductors could still play a role), while approaching the latter requires a more articulated discussion.

The semiconductor/electrode interface is generally modeled as a Schottky contact, for which the current density is governed either by thermoionic emission or tunneling (when the barrier width is short, for example, for heavily doped semiconductors).[19,52] Within these models, ρ_c can be reduced by lowering the energetic barrier height between semiconductor and electrode φ_b or by introducing a sufficiently high dopant density in order to allow charge tunneling. Many approaches have been proposed in the past to this purpose, and the interested reader can find details in many comprehensive reviews.[3,52,53,62] However, this goal should also be reached by appropriate techniques suitable for the future scale-up to mass production. Approaches of this kind that also demonstrated ρ_c in the suitable range for high-frequency OFETs (i.e., below 0.01 Ωcm^2) are not yet available for staggered structures, to the best of our knowledge, and in the following, we concentrate on suggesting promising routes toward this goal.

In principle, the most powerful approach would replicate the strategy already adopted for the MOSFET technology, based on the introduction of appropriate dopants in the semiconductor region in order to shrink the injection barrier width and allow for charge tunneling. A wide set of techniques suitable to this purpose have been attempted, including the introduction of molecular dopants, metal salts, and polymeric or metal-oxide interlayers. Doping of the contact region is a powerful technique with a twofold advantage: in addition to enabling an ohmic contact due to charge tunneling across the energetic barrier, in the case of bulk doping, it also enhances charge transport across the semiconductor via filling of charge trapping sites.[52] However, despite some remarkable advancements in this direction, some aspects remain problematic to date, for example, the insufficient electrical stability due to dopant migration in the polymeric film and the limited doping efficiency (usually below 10%) of organic molecules.[62,63] Moreover, this approach requires that the doped region be confined only in the contact area in order to maintain a high ON/OFF ratio for the transistor and ideal behaviour.[64] Of course, this requires some kind of patterning, which is problematic once we consider the case of scalable fabrication techniques for micron-sized OFETs.

Alternatively, the barrier height can be reduced via the introduction of appropriately engineered dipoles, conventionally in the form of SAMs. This approach has been used extensively in the past, and is particularly powerful for downscaled OFETs, fabricated via cost-effective techniques, by virtue of two advantages: first, the molecules composing the SAMs can be appropriately engineered so to yield a variety of potential drops across the dipole, thus they can be matched with the materials in use, and second, the anchoring group can be designed so to bind specifically to the electrode material, without the need for dedicated, high-resolution patterning schemes.

Overall, we think that it is necessary to combine the advantages of SAMs and dopants in order to achieve, with scalable fabrication processes, the extremely low ρ_c (below 0.01 Ωcm^2) required for GHz-range OFETs. In particular, a suitable doping scheme, which would enable low-resistivity ohmic contacts via charge tunneling, should be integrated via a self-assembling process, which would allow for a modification of the semiconductor properties only in the vicinity of the contact region, avoiding detrimental effects on the ideality of the OFET behavior. To this goal, promising approaches have been proposed in the past years by a number of authors. Seah et al. proposed a method consisting on the self-assembly of polyelectrolyte monolayers on metal electrodes.[65] In their scheme, polyelectrolytes self-assemble on the metal through image-charge attraction and self-align on the contact without the need for additional patterning. Then, after the deposition of the semiconductor, a doped charge region is induced in the latter near the contact area, possibly enhanced via an intermediate processing step in which dopant molecules are exchanged into the polyelectrolyte. The authors demonstrated with this method to be able to reduce ρ_c to values below 0.1 Ωcm^2. Moreover, their approach is general, since it can be applied to different polyelectrolytes and semiconductors, and is effective against dopant migration, which would degrade the achieved performance over time. Another approach has been proposed by Nicht et al., in which a molecular dopant is functionalized with a triazole anchor group in order to achieve self-assembly on a gold electrode.[66]

However, as an alternative to self-assembly, methods relying on self-aligned photo-doping or photo-dedoping can be used. In these schemes, photosensitive dopant molecules[67] are deposited on the electrodes or introduced in the active layer without patterning. Then, doping/dedoping is induced by irradiating the whole sample with light while the electrodes are used to mask some regions from modification. For instance, Jacobs et al. have shown a technique in which P3HT films, doped with F4-TCNQ, can be dedoped upon irradiation with light at a selected wavelength.[68] Such a process can be also applied to other polymer/dopant combinations.[69] More information on such methods can be found in the study by Jacobs and Moulé.[70]

Overall, a certain number of options, including also solution-based approaches, have been demonstrated for the fabrication of OFETs yielding the necessary high mobility for GHz operation. However, high mobility in excess of several $cm^2 V^{-1} s^{-1}$ is not sufficient, and it is essential to obtain unprecedented low contact resistance for staggered devices, below 100 Ωcm. Moreover, in the range of geometrical parameters required for high-frequency OFET structures, low R_c has to be achieved mainly by reducing ρ_c. This is challenging per se, and it is further complicated when the use of solution-based or scalable techniques is considered. However, low ρ_c in the range 0.1–0.01 Ωcm^2 has already been demonstrated to be feasible with organic

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transistors, and the future effort should be directed toward the achievement and improvement of this performance with one of the promising techniques that could allow the upscaling to cost-effective mass production.

3.2. High Resolution by Scalable Techniques

High-frequency operation of OFETs requires the downscaling of the geometrical features of the device, namely of the channel and overlap lengths (Equation (2)). The first-order estimations illustrated in Table 2 predict that the achievement of 100 MHz–1 GHz operation requires an aggressive downscaling of such features, below the micrometer scale, which is well below the typical dimensions of majority of state-of-the-art OFET demonstrations. To this goal, it is thus necessary to identify and develop suitable high-resolution fabrication techniques. This challenge is further complicated by the fact that such solutions should be also suitable for the future implementation of cost-effective, energy-efficient mass-production facilities, which requires selecting techniques featuring low-temperature compatibility and allowing for large area patterning with high throughput, possibly via solution-processing or direct-writing schemes. In this section, we review some of the options demonstrated in the literature in the recent years, satisfying some of these requirements and holding a potential for the future integration of high-frequency OFETs into distributed electronic applications.

Fabrication techniques can be classified into two broad categories: subtractive or additive processes. In additive processes, the material is directly deposited on the substrate according to the desired pattern, without the use of masks or masters. This approach is intrinsically more convenient, due to the reduced number of processing steps involved in the patterning and to the lower amount of material waste. In subtractive processes, the patterning is based on the removal of the functional material, previously deposited with a low resolution. The patterning could rely on the direct removal (e.g., via laser etching) or on intermediate steps in which a sacrificial material is pre-patterned (e.g., lithography). This class of techniques, usually including processing steps relying on etching or lift-off, is intrinsically subject to higher chemical and material waste. Despite these drawbacks, usually subtractive processes allow for higher resolution than additive techniques. Due to this tradeoff, and since both categories possess convenient features in view of the future implementation of mass-production schemes, we present here a selection of techniques belonging to both categories (**Figure 3**).[22,72–76]

Printing techniques are additive techniques considered among the promising candidates for the realization of a cost-effective production process at low temperature and on conformable substrates. In particular, a well-established printing method, namely gravure printing, combines these advantages with high-throughput patterning of functional inks.[77] In this technique, two cylinders operate as follows: the gravure cylinder, which is engraved with the pattern to be transferred, collects the functional ink from a bath and fills the engraved cells; then the impression cylinder imposes a pressure on the substrate placed in between the two (Figure 3b).[72] The resolution of this technique, conventionally limited to several tens of micrometers, can however be improved down to the few-micrometers range through careful cylinder design or by appropriate engineering of the ink viscosity.[78,79] Kitsomboonloha et al. have demonstrated OFETs, realized by gravure printing, featuring a channel length of 1.7 µm.[32] They exploited this improvement in resolution to demonstrate a transition frequency as high as 1.92 MHz for these gravure-printed transistors.

A second widely adopted printing technique is inkjet printing, which is a direct-writing method allowing for the fast fabrication of digitally designed patterns on a wide variety of materials, including flexible substrates. Moreover, the deposition requires no direct contact with the substrates, reducing the risk for defects induced by contact with mechanical parts. Inkjet printing allows the direct deposition of controlled volume of functional materials in a material-efficient manner (Figure 3a).[5] The conventional resolution of the pattern is generally limited (≈10 µm), and approaches to improve this figure have been proposed in the past: for example, the pre-structuring of the substrate with banks is effective in reducing the size of the final pattern by containing the jetted inks in smaller areas. Modifications of this technique were based on the adoption of electric fields to produce the formation of a droplet (electrohydrodynamic jet printing), in which the volume of the droplets is reduced below a femtoliter.[80] With this approach, the functional materials can be patterned down to a resolution of 1 µm.[81] Inkjet printing is intrinsically slower than other high-throughput printing techniques (e.g., gravure, flexography); however, this drawback can be alleviated using parallelization (multi-nozzle) strategies.

To obtain smaller channel lengths (in the sub-micrometer scale), techniques integrating printing with a self-assembly-driven process have been demonstrated. One of these is self-aligned printing, in which the surface energy of a preprinted pattern is modified with a suitable chemistry (e.g., SAMs, surfactants, or plasma-etching), in order to promote the flow-off of a second printed pattern on the side of the first (Figure 3c).[73] Noh et al. demonstrated with this technique channel lengths in the 60–400 nm range, controlled by selecting the process conditions, and fabricated OFETs with a transition frequency of 1.6 MHz.[13]

However, despite the engineering of the printing techniques illustrated above has allowed to reach useful resolution for GHz operation of OFETs, it either requires the modification of the interface of the patterns (which might be deleterious for the final device), or poses constraints on the pattern geometry (which might be problematic for the pattering of complex circuits), or might be difficult to integrate in a fast, high-throughput process.

The class of subtractive processes named nano-imprint lithography (NIL) techniques has been proposed, where the patterning is performed on a sacrificial resist layer, while the functional material is deposited afterward with an appropriate low-resolution technique. This method, while relaxing the requirement for engineering of the pattern geometry or modification of the functional material, enables patterning of features down to a size of 10 nm.[74] Implementations on roll-to-roll machinery could define patterns at speeds in the order of 1–10 m min^{-1}, over a large area.[82] Depending on the materials and energy source used in the process, NIL can be classified into thermal, UV, and electrical. In thermal NIL (Figure 3d), a mold is pressed on a melted resist deposited on the substrate. The resist will fill the mold and, after cooling down, the desired

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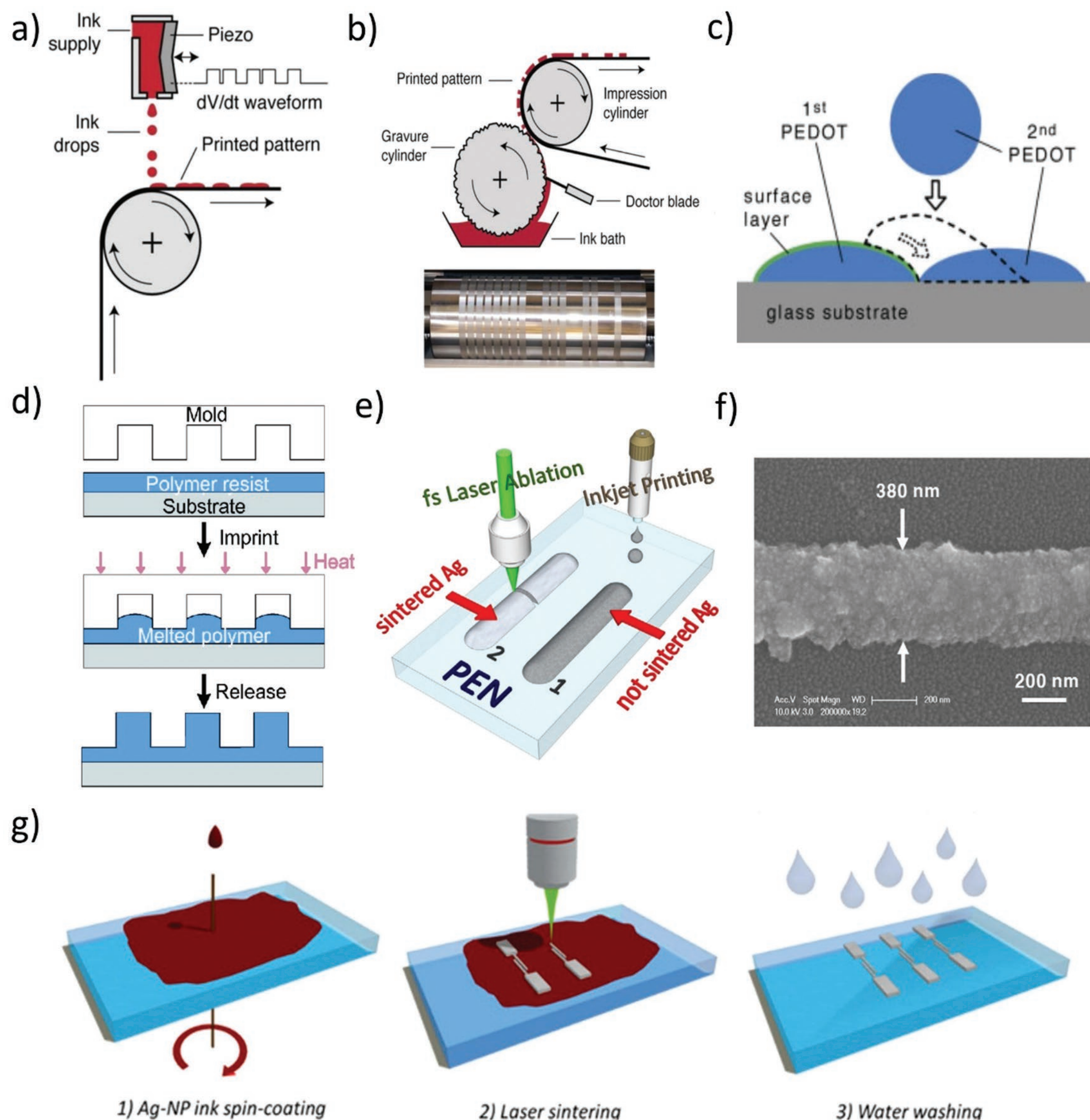

Figure 3. Schematic illustration of a) piezo-based drop-on-demand inkjet printing. Reproduced with permission.[72] Copyright 2013, Wiley Periodicals, Inc.; b) gravure printing. Reproduced with permission[72] Copyright 2013, Wiley Periodicals, Inc.; c) self-aligned printing. Reproduced with permission.[73] Copyright 2005, Wiley-VCH; d) nanoimprint lithography. Reproduced with permission.[74] Copyright 2019, Springer Nature; e) femtosecond-laser ablation. Reproduced with permission.[75] Copyright 2013, Elsevier; f) laser-sintered silver line. Reproduced with permission.[76] Copyright 2012, Elsevier; g) femtosecond-laser sintering. Reproduced under the terms of the Creative Commons CC-BY 4.0 License.[22] Copyright 2016, The Authors, published by Springer Nature Limited.

structures are formed.[74] In UV-NIL, the resist is an UV-curable polymer that is cured once the mold is slightly pressed over it. In some instances, due to the high aspect ratio of the pattern and the polymer surface tension, it can be difficult to fill the mold.[83] For this reason, electrocapillary-NIL has been developed, in which a voltage is applied between a conductive mold and the substrate, decreasing the contact angle and inducing the filling of the mold cavities by the polymer driven by electrocapillary force.[84] Higgins et al. used UV-NIL to fabricate OFETs with a channel length of 380 nm in a bottom gate-top contact configuration.[85] They first patterned the 380 nm wide bottom gate with NIL, then they integrated an UV-based self-alignment scheme to define the source and drain electrodes of the device. With this method and design, their devices featured a transition frequency of 3.3 MHz.[34]

Overall, the most desirable approach would combine the flexibility offered by direct-writing techniques, which allow for easy digital design of complex patters, with high fabrication speed and compatibility with flexible substrates. In this respect, hybrid techniques that combine solution-based pre-patterning with laser-based fast and high-resolution postprocessing have been demonstrated in the past years. Lasers are unique tools for locally modifying with very high precision the properties of surfaces with a contactless approach, since they can deposit a well-controlled amount of energy in volumes as small as 1 μm^3.

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In laser ablation, a laser beam is used to physically remove material from a surface, thus is a suitable tool to fabricate submicron-sized gaps between conductive electrodes in order to define OFET channels. Bucella et al.(Figure 3e) demonstrated ablation of inkjet-printed Ag electrodes by femtosecond laser, obtaining a submicrometer channel.[75] The use of ultrashort laser pulses (picosecond- or femtosecond-long) is fundamental to prevent any modification or damage of the material surrounding the irradiated volume.[86]

On the other hand, laser sintering allows to directly pattern micron-sized conductive features on a rigid or flexible substrate upon irradiation with a laser beam.[87] In particular, an ink containing metal nanoparticles is deposited on a substrate through conventional low-resolution printing or coating techniques and then locally sintered by laser beam, to obtain conductive structures. The nonirradiated area is unaffected, and the residual ink can be removed after laser patterning through washing with an appropriate solvent, and in case collected and recycled. Son et al.[76] (Figure 3g) realized laser-sintered conductive features down to a resolution of 380 nm with a laser power of 150 mW at a scanning speed of 400 µm s^{-1} and Perinot and Caironi (Figure 3f) fabricated with a similar approach OFETs with a channel length in the order of 1 µm on plastic substrates.[25] Despite these demonstrations were limited in terms of maximum processing speed, in the future, the throughput of the process can be improved via multiple-beam parallel processing.

In conclusion, several promising methods capable of yielding the necessary resolution (below 1 µm) for high-frequency OFETs have been shown in the past. In this section, we have briefly gone through a selection of those that we consider the most promising also in terms of combining high-resolution patterning capabilities with the requirements for fast, cost-effective, energy-efficient fabrication of OFETs on conformable substrates. To date, there is still no clear option capable of integrating high-resolution with the whole set of desirable aspects, in particular with respect to the speed-resolution tradeoff. However, there has been a clear trend of improvement in proposing and discovering new techniques, including laser-printing hybrid methods, engineered roll-to-roll gravure printing, or roll-to-roll NIL patterning. The future effort should be directed to further improve these processes and demonstrate high-resolution patterning of more complex circuits with high speed on flexible substrates, in order to clearly identify a credible route to mass production of high-frequency organic electronic applications.

3.3. Downscaling the Thickness of the Dielectric Layer

A general requirement for the implementation of organic transistors in a wide range of real applications is the operation at low voltage bias. The latter can be achieved by integrating dielectric layers with high areal capacitance, which allow both to maintain high charge density in the accumulated OFET channel with low voltage bias and to yield a steep subthreshold slope. The achievement of such goal has been an extensive subject of research and has been approached with a number of methods aiming at increasing the dielectric layer areal capacitance while retaining scalability of the fabrication process. In general, such approaches combine a reduction of the thickness of the dielectric together with the adoption of materials with a high permittivity. We will not describe here such approaches in detail and we refer the interested reader to some excellent reviews on this topic.[4,5,88,89]

In addition to the general requirement of ideal transistor operation with reduced voltage bias, high-frequency transistor operation poses additional constraints on the dielectric material and layer dimensions. One of these requirements is the containment of short-channel effects (SCEs). Such effects are well-known in the context of downscaling of FET devices and lead to the degradation of the device parameters with the reduction of the channel length and the increase of the drain-source voltage. Deteriorations induced by SCEs include lack of pinch-off, threshold voltage roll-off, increase in the OFF current, and degradation of the subthreshold slope. Such issue, in the context of silicon MOSFETs, has been attributed to the breakdown of the gradual-channel approximation and has forced to accompany the channel length scaling with the reduction of the dielectric layer thickness.[19] Analytical models have been developed for these kinds of devices, identifying a critical length λ that depends on a set of device parameters, including the dielectric constants of the semiconductor and of the dielectric, the depth of the depletion region, and the thickness of the dielectric layer.[90,91] In these cases, SCEs can be avoided if, for a selection of these parameters, the channel length is more than three times λ.

The configuration of an OFET is more similar to that of a silicon-on-insulator (SOI) MOSFET,[92] for which the analysis at the base of the definition of critical length cannot be applied.[93] To the best of our knowledge, there is no analytical model to determine an analogous of the critical length λ for these devices, and researchers have relied on simulations and on empirical relations.

In order to gain some insight, we adopt here an empirical formula proposed by Xie et al. for short-channel SOI MOSFETs,[94] which proposes that, in order to limit the SCEs, the channel length should satisfy

$$L \geq 2.5\left(t_{\mathrm{OSC}} + \frac{\varepsilon_{\mathrm{OSC}}}{\varepsilon_{\mathrm{diel}}} t_{\mathrm{diel}} + 0.18L\right) \tag{4}$$

where t_{OSC} and t_{diel} are the thicknesses of the semiconductor and dielectric layers, respectively, while $\varepsilon_{\mathrm{OSC}}$ and $\varepsilon_{\mathrm{diel}}$ are the respective dielectric constants. Within the frame of this model, we performed some simulations to determine the minimum L, named L_{min}, versus the variation of $\varepsilon_{\mathrm{diel}}$ and t_{diel}. We set $\varepsilon_{\mathrm{OSC}} = 3$ and $t_{\mathrm{OSC}} = 40$ nm, typical parameters for an organic semiconductor layer.

The surface plotted in **Figure 4**a (in which the scale for L_{min} has been limited to 1 µm) denotes the minimum channel length to avoid the appearance of SCEs for given dielectric layer properties, clarifying two aspects: first, the reduction of the dielectric thickness is required for ideally operating OFETs with a targeted channel length below the micrometer range; and second, the adoption of high-k materials helps in avoiding SCEs.

Anyway, the above analysis should be taken only as a general guidance, since the application of models specifically developed for SOI MOSFETs, despite the similar architecture,

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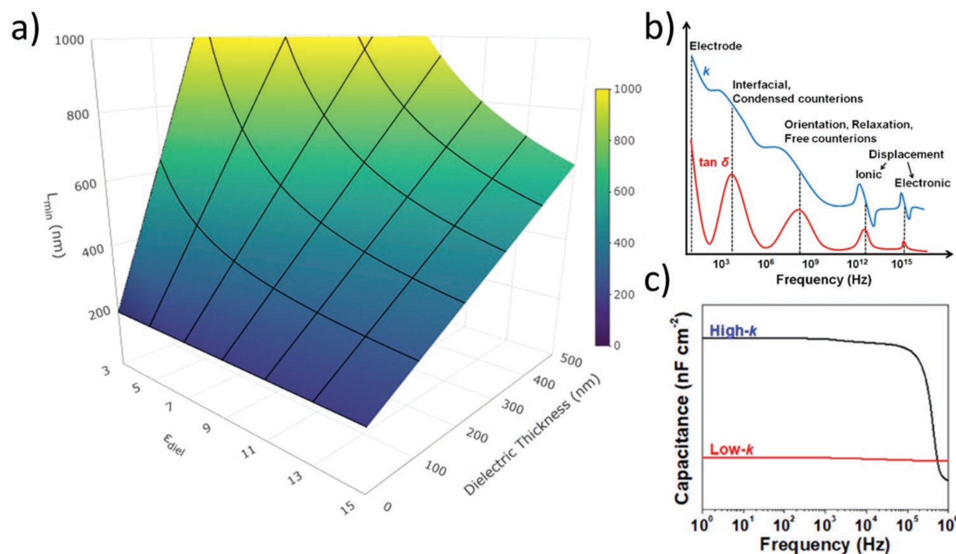

Figure 4. a) Minimum channel length L_{min} to prevent the appearance of SCEs in FETs for given parameters of the dielectric layer. b) Indicative frequency dependence of the dielectric constant k and the dielectric loss tan δ for a prototypal dielectric material, highlighting the ranges of different dielectric relaxation processes. Reproduced with permission.[4] Copyright 2018, American Chemical Society. c) Schematic comparison of the frequency-dependent areal capacitance of high-k and low-k dielectrics. Reproduced with permission.[4] Copyright 2018, American Chemical Society.

might not be directly portable to organic thin-film transistors. Moreover, it must also be considered that for the case of organic thin-film transistors, other causes might be at the origin of SCEs. It has been shown that space-charge limited current (SCLC) regions could also induce short-channel effects,[95] possibly reinforced by Poole–Frenkel mobility enhancement.[96] Nonetheless, experimental data show that also in some of these cases, SCEs can be mitigated with the scaling of the dielectric thickness.[97]

Overall, the general indication suggests that thin dielectrics with a thickness below few hundreds of nanometers are required for optimal operation of low-voltage and high-frequency solution-processed OFETs. Of course, this requires in turn selecting or devising techniques capable of yielding a robust thin dielectric layer: this remains a considerable challenge, especially for large areas, since thin solution-processed layers are more prone to suffer from structural defects (e.g., pinholes). In this respect, a clever solution could in principle be constituted by ionic gating schemes, in which a high capacitance is yielded by an atomically thin double layer at the interface with the semiconductor. This process can be exploited in combination with a solid polymeric structuring matrix, which in this case can be thicker than few hundreds of nanometers (SEGI dielectrics).[98] However, these solutions are momentarily limited by their slow switching speed, in the tens of kHz range for the best reported cases,[4,99] because of the slow movement of ions. A second approach is constituted by the use of dielectric materials with high permittivity, which could mitigate the requirement for low thickness and help in the achievement of high capacitance and more ideal transistor operation. Anyway, for these materials to be a convenient choice, they should exhibit a sufficiently high dipolar relaxation frequency for the application to be implemented, at least as high as the targeted f_t. Unfortunately, the available high-k polymers to date typically feature dipolar relaxation frequencies in the order of 10–100 kHz, and more rarely above 1 MHz (Figure 4c). This is intrinsically related to the fact that their high permittivity is due to dipolar orientational polarization (Figure 4b), which limits the maximum relaxation frequency.[89] A possible solution for future high-k dielectric materials that do not suffer from this drawback might be constituted by nanostructurally engineered polymer blends, for which the introduction of excess free volume in the film yields high k and flat frequency response.[100] Conversely, high-k metal-oxide dielectrics are not intrinsically limited by such drawback and may constitute a viable choice. Some approaches to deposit thin layers of such materials with solution-based methods at low temperature have been devised in the past. For example, it has been shown that a thin (≈20–60 nm) dielectric layer of alumina and a bilayer of alumina and zirconia can be fabricated from solution within a maximum process temperature of 150 °C. Such layers yield a reasonably flat frequency response up to the maximum measured frequency of 1 MHz.[101] A challenge for such dielectrics can be represented by their compatibility with flexible circuits, as metal-oxides layers are more prone to cracking.[102,103]

As a consequence of such complications, related to frequency relaxation and/or mechanical instability, the most credible approach to date requires low-k polymers, for which the main contribution to the permittivity comes from electronic polarization, which typically relaxes at frequencies in excess of the THz range.[4] Some authors have demonstrated in the past that solution-processed OFETs with low-k thin-film dielectrics are achievable at laboratory scale,[104–107] clarifying that a route of this kind for high-frequency FETs can be devised. In principle, ultra-thin dielectric layers based on insulating SAMs have also been demonstrated, with optimal performance in terms of high capacitance and low current leakage. However, their suitability is limited to bottom-gated architectures.

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Table 3. Summary of the ranges of achievable thickness and capacitance for dielectric layers belonging to a selection of classes.

Dielectric class	Thickness range [nm]	Capacitance range [nF cm^{-2}]
Solution-processed polymers	≈30 to >1000	<330
Low-temperature, solution-processed metal-oxides	14–180	180–705
Inorganic/organic hybrid composites	≈30 to >1000	<137
Inorganic/organic hybrid bilayers	25 to >600	<230
SAMs	≈2–3	340–1750
CVD (polymer deposition)	>6	<325

These reported values are based on the data collected in some recent reviews.[4,5,88,89]

In addition, despite solution-based methods offer major advantages in terms of speed and ease of fabrication, other options can be considered suitable for mass production, provided that at least a sufficiently high throughput is guaranteed. For example, chemical or physical deposition methods (e.g., CVD) can yield thin and defect-free dielectric layers over large areas, which, however, comes at the cost of a considerably longer deposition time compared to solution processing.

To summarize the considerations of this section, and to provide a first-order guidance for the development of high-frequency OFETs, in **Table 3**, we present the ranges of the achievable thicknesses and areal capacitances for some selected classes of dielectrics. The ranges reported here are based on the results already collected in some recent comprehensive reviews,[4,5,88,89] and should be considered simply as a general guidance, together with the considerations already illustrated above.

As of now, there is no clearly advantageous option combining high capacitance, electrical and mechanical robustness, and cost-effective deposition method at the same time. The effort toward further advancements will need to be directed to identifying a suitable scheme for fabricating robust dielectric layers combining all the necessary requirements illustrated above.

3.4. Low-Overlap Structures for Reduced Parasitism

HF operation (i.e., high transition frequency) of transistors requires the minimization of the capacitance developing between gate and source/drain electrodes (see Equation (1)). Its two main components are the channel capacitance, which is associated to the charges accumulated in the channel, and the capacitance originating from the geometrical overlap between gate electrode and source/drain. While the former is intrinsic to the device operation and cannot be eliminated, the latter can ideally be reduced without affecting other transistor parameters (primarily the transconductance). In reality, some aspects regarding the geometrical overlap between gate electrode and source/drain have to be considered.

In particular, it has been demonstrated that the contact resistance in staggered architectures, which allow to keep R_c under control even in the case of limited areal capacitances, depends on the gate overlap and on a device-specific transfer length L_T, according to the current crowding model (see Section 3.1). Ante et al. have simulated the achievable f_t versus channel and contact length downscaling, taking into account the effect of such scaling on R_c.[39] Their analysis shows that, in the most favorable case, f_t improves with the reduction of the overlap length L_{ov} until it plateaus for $L_{ov} \approx L_T$, and no further increase of the transition frequency is possible. Nonetheless, in our analysis in Section 3.1, we showed that it is possible to overcome the tradeoff set by the charge injection performance and capacitive parasitism, both depending on L_{ov}, by achieving low ρ_c, at least below 0.001 Ωcm^2. Experimentally, the same concept has been shown by Natali et al. from a different point of view. The authors have shown that, if the dominant component of R_c is charge injection from the electrode to the semiconductor, rather than the bulk access component, and the energetic barrier for injection is relatively large, L_T scales alongside with the reduction of the channel length.[108] The scaling of L_T, in their case, was associated to an increase of the lateral electric field with the downscaling of L, which in turn promoted charge injection via reduction of ρ_c. Similarly, reduction of ρ_c with the scaling of the channel length (or, equivalently, with the increase of the electric field) has also been observed via simulations using a semi-phenomenological model and fitted data extracted from experiments.[59] Overall, these findings trace a route for the reduction of the gate overlap without the introduction of detrimental effects on charge injection performance.

3.4.1. Capacitive Parasitism of No-Overlap Structures

In the following, we consider an optimized scenario where zero-overlap structures are possible. We start from a simplified case where SCEs are not present (see Section 3.3), effects that are considered only after describing the general behavior of zero-overlap configurations. In this case, according to the roadmap illustrated in Table 2, GHz operation can be achieved with $\mu < 5$ cm^2 V^{-1} s^{-1} and L in the 0.5–1 µm range, which are reasonable parameters. Nonetheless, even in an ideal situation where charge injection is optimal and the geometrical overlap can be reduced to zero in accordance with the previous guidelines, a zero-overlap architecture does not imply that the parasitic gate to source/drain capacitance can be neglected. This is related to the increasing impact of the contribution of to the fringing electric field, which becomes important as the critical size of the device features is aggressively scaled down. In this context, the parallel-plates (PP) approximation is no longer applicable, and more precise models should be adopted for the design of high-frequency devices. This aspect has been previously considered in the case of very large scale of integration (VLSI) silicon electronics, and we can refer to some of the models developed for that case to understand and tackle this issue in the context of organic FET devices. Barke has reviewed several methods for the estimation of the capacitance insisting between a conductive line and a ground plane,[109] and found that an empirical formula proposed by van der Mejis and Fokkema[110] allows to estimate such capacitance with optimal accuracy. In particular, the maximum deviation is 2% if $\frac{L}{d} \geq 1$ and if $0.1 \leq \frac{t}{d} \leq 4$ (see **Figure 5**a for the definition of the parameters)

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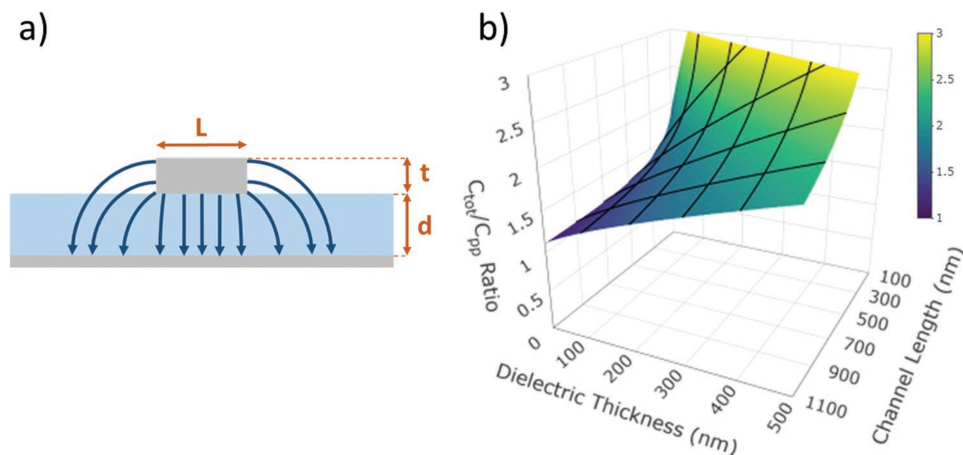

Figure 5. a) Schematic lateral view of a gate-to-ground configuration, highlighting the contribution of the fringing electric field. b) 3D plot of C_{tot}/C_{pp} versus channel length and dielectric thickness.

when compared to Chang's formula,[111] which is commonly chosen as a reference. These intervals represent a relevant range for the state-of-the-art high-frequency organic FETs. The Mejis/Fokkema formula reads

$$c_{tot} = \varepsilon\left(\frac{L}{d} + 0.77 + 1.06\left(\frac{L}{d}\right)^{0.25} + 1.06\left(\frac{t}{d}\right)^{0.5}\right) \tag{5}$$

where c_{tot} is the capacitance per unit length of the gate/plane structure and ε is the permittivity of the dielectric medium. To assess the error made using the PP model in the case of low-overlap structures, we used such approximation to calculate the ratio of c_{tot} and c_{pp} (the capacitance calculated via the PP formula) for L within the 100–1100 nm range, d within the 20–500 nm range, and with t set to 80 nm. The results are shown only for L/d and t/d satisfying the above conditions.

As shown in Figure 5b, as the channel length is downscaled the total capacitance, c_{tot} steadily deviates from the value predicted by the PP model, and reaches values as high as three times c_{pp} when the shortest L are considered. While such behavior can be mitigated if the reduction of L is accompanied by the scaling of the dielectric thickness, this approach becomes challenging in practice when considering solution-based approaches and d below few hundreds of nanometers, owing to practical difficulties in the deposition process of a robust dielectric.

The above approach is a first-order approximation where the active area of the device is schematized as a ground plane. So, to further extend our analysis, we simulated the capacitance of a representative low-overlap top-gate and a bottom electrode configuration (**Figure 6**b, inset). We used a capacitance extraction software based on a numerical solver for the Maxwell's equations.[112] In this simulation, we are excluding the channel region of the FET and we consider only the capacitance associated to fringing and geometrical overlap. Moreover, we consider that the dielectric material is only present between the two electrodes, while the surrounding volume has the dielectric constant of the vacuum. In our first simulation, we varied the size of the overlap between the two electrodes (Figure 6a). Within our reference system, positive values correspond to a geometrical overlap of the structures, while negative values represent a gap. We ran the simulation for three selected thicknesses of the dielectric ($\varepsilon_r = 5$): 100, 350, and 500 nm.

We see that, for positive values of the overlap, the capacitance increases linearly in agreement with the PP capacitor model, with steepness consistent with the thickness of the dielectric. When the overlap distance drops to 0, only a residual capacitance associated to the fringing field is present, and that capacitance is the same within the whole range of investigated thickness for the dielectric. When we further separate the electrodes by introducing a gap, the capacitance slowly decreases while widening the separation between the electrodes, with a faster decrease for thinner dielectrics. More importantly, this also highlights that, for all the investigated thicknesses and (positive) overlap distances, the fringing contribution is constant. This can be qualitatively understood by the observation that two mutually compensating processes occur as the separation between the two electrodes is reduced: the capacitance increase due to the approaching of the plates is compensated by the recession of the lateral extension of the fringing electric field. We also confirmed that such behavior (for zero-overlap distance) is maintained in the whole range of dielectric thicknesses between 100 and 500 nm (not shown). Finally, we verified that in the case of no overlap and dielectric thickness of 500 nm, the fringing capacitance linearly increases with the increase of ε_r of the dielectric medium (Figure 6b), with a small deviation for low ε_r, when the dielectric constant of the sandwiched dielectric material approaches the one of the surrounding environment.

Aided by this evidence, we can propose a first-order, approximated method for the estimation of the achievable f_t in FET structures with no geometric overlap upon scaling of the geometrical dimensions, taking also into account the contribution of the fringing field. Since the fringing capacitance per unit width ($C_{ov,0}$) depends linearly on ε_r and does not depend on the dielectric thickness, we set $C_{ov,0} = A\varepsilon_0\varepsilon_r$, and by linearly fitting the data in Figure 6b, we get $A = 0.952 \approx 1$. The substitution into the formula for the calculation of the transition frequency (see Equations (1) and (2)) yields

$$f_t = \frac{g_m}{2\pi\left(C_{ch} + 2WC_{ov,0}\right)} \cong \frac{\mu V_{ov}}{2\pi L(L+2d)} \tag{6}$$

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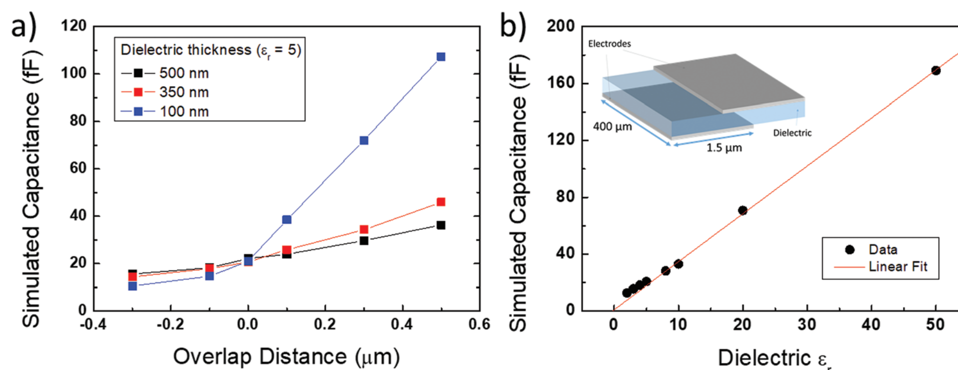

Figure 6. Simulated capacitance insisting between the schematized low-overlap electrode configuration: a) simulated capacitance versus geometrical overlap length, b) simulated capacitance versus ε_r of the dielectric layer.

where the channel capacitance is expressed as $C_{ch} = \frac{\varepsilon_0 \varepsilon_r WL}{d}$. Our simple approximated method shows that, even in the case of no geometrical overlap, the contribution of the fringing capacitance is equivalent to having an overlap length L_{ov} equal to the dielectric thickness. We remark that this approximation has been derived from simulations only in a specific range of dimensions, and care should be taken in extrapolating such results for a different geometrical sizing.

Finally, we compared the three different models for the calculation of the capacitance and the extraction of f_t (i.e., the PP model, the Mejis/Fokkema model, and our simple approximation). In **Figure 7**, we show the calculated transition frequency versus L and d, for which the capacitance has been estimated with the three methods, and the effective charge mobility and overdrive voltage have been respectively set to 5 cm^2 V^{-1} s^{-1} and 10 V. First, the simple PP model correctly yields a quadratic dependence of f_t versus reduction of L, while at the same time, no dependence on the dielectric thickness is identified. On the other hand, when we adopt one of the other methods to better estimate the achievable f_t, an additional dependence on d is introduced, which degrades the achievable maximum frequency performance for some given critical dimensions. The values closest to the estimation from the PP model are achieved for low dielectric thickness, while f_t is further reduced as d is increased for a given channel length. As an example, we can consider the geometrical sizing necessary to achieve f_t = 1 GHz according to the three models (see Figure 7, contour lines projected on the bottom plane). While the PP model (blue line) would suggest that $L \approx 900$ nm is sufficient and that no requirement is needed on the dielectric thickness, the predictions of the other methods show that a shorter channel length is necessary, with the required L plummeting if the dielectric thickness is not downscaled along with the channel length. Having elucidated the general behavior of f_t for no-overlap structures with fringing contributions, we can now integrate the analysis developed in Section 3.3 regarding SCEs. In analogy with the findings illustrated in such section, the reduction of the dielectric thickness is required also to appropriately control the OFET channel when L is downscaled. The necessary scaling of the dielectric thickness depends also on the permittivity of the dielectric material, so that the constraints on L and d are different with respect to the dielectric material integrated into the OFET device. If we integrate the previous simulations with the constraints on L and d deriving by the necessity of avoiding SCEs, we highlight that, even in this case, the effect of fringing field is non-negligible and should be considered in the design of GHz-range OFETs. For instance, in the case of a dielectric with $\varepsilon_{diel} = 5$, for which the requirements on L and d are the most restrictive, a GHz-range OFET with contained SCEs can be realized with a dielectric thickness of 200 nm: without accounting for fringing, the required L would be ≈900 nm, but the inclusion of fringing effects requires the channel length to be reduced to ≈700 nm.

In conclusion, to fully exploit the advantages of zero-overlap configurations for f_t improvement, particular care should also be taken in order to scale the dielectric thickness, even when SCEs have already been accounted for. As a tool for the design of high-frequency FETs of this kind, since the PP model ceases to be representative in the case of no-overlap configurations, we propose both the Mejis/Fokkema model and a simple empirical formula, the dielectric thickness approximation. The first

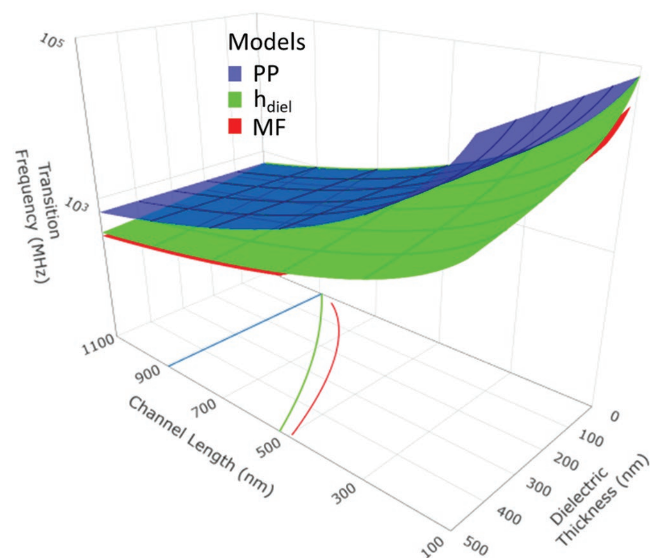

Figure 7. Comparison between three capacitance models (see main text) for the estimation of the transition frequency of FETs. The lines on the lower plane correspond to the projections of the three surfaces for f_t = 1 GHz. h_{diel}, dielectric layer thickness model. MF, Mejis/Fokkema formula; PP, parallel-plate model.

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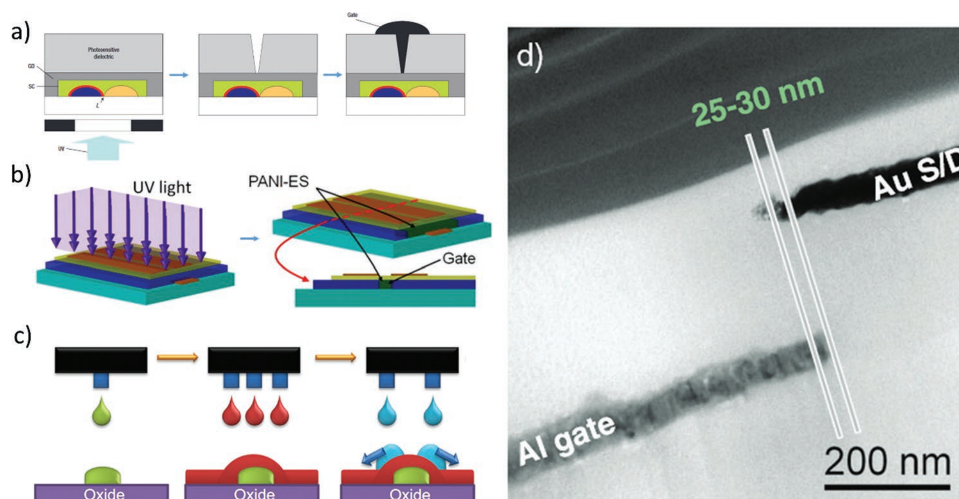

Figure 8. a) Self-aligned gate process according to Noh et al.[13] Reproduced with permission.[13] Copyright 2007, Springer Nature. b) Fabrication procedure of the self-aligned poly(aniline) gate electrode as in the study by Jussila et al.[115] Reproduced with permission.[115] Copyright 2012, Elsevier. c) Inkjet transistor process with self-aligned source and drain according to Tseng and Subramanian.[118] Reproduced with permission.[118] Copyright 2011, Elsevier. d) Overlap between source and gate electrode for UV-NIL self-alignment according to Palfinger et al.[114] Reproduced with permission.[114] Copyright 2010, Wiley-VCH.

model has been developed for the VLSI technology and has been validated by a wide number of works (e.g., Barke's[109]), but the geometry is not fully representative of the FET architecture, while the second is based on a set of simulations for representative geometries and dimensions, which is anyway limited in range. Nonetheless, we remark that despite such limited set of simulations, our model can still replicate the predictions of the Mejis/Fokkema (see Figure 7) with good approximation, while offering at the same time an interpretation based on a simple physical picture.

3.4.2. Fabrication Techniques for No-Overlap Structures

Thus, while it is paramount to accompany the reduction of the overlap with the dielectric thickness scaling, it is also desirable to achieve this with fabrication techniques that are more easily up-scalable to mass production. In this context, both goals are still an open challenge when considering the dimensions relevant for the achievement of GHz operation. We have discussed some available options to achieve the downscaling of the dielectric layers in Section 3.3, and we only review here some promising approaches based on self-alignment for the fabrication of no-overlap structures. Most approaches rely on the use of photosensitive materials that change their properties upon photo-exposure and, when the source/drain electrodes are used as a mask for the irradiation, only the channel area of the transistor is affected by the modification. A set of variants of self-alignment techniques (**Figure 8**) have been shown in the past, based on UV irradiation of resists,[13] UV-NIL,[34,113,114] poly(aniline) photoconversion,[115] and surface energy modification.[116,117] In case UV irradiation is not compatible with the used substrates or active materials, other methods have been proposed, based, for example, on dewetting promoted by optimized mesa-type structures (Figure 8c).[118]

Moreover, among the illustrated techniques, UV-NIL has also been demonstrated within an implementation into roll-to-roll production machinery,[119] proving that the future implementation of high-throughput production facilities is feasible. In **Table 4**, we report the ranges of achieved overlap length and width-normalized overlap capacitance for a selection of self-alignment techniques for the fabrication of organic transistors.

In general, these works clarify that, even though a minimum residual overlap length of 30 nm can be achieved using such techniques, zero-overlap structures are difficult to implement. We also report the measured overlap capacitances, since they represent the achieved value of the parasitism in experimentally realized devices. On the other hand, these values are only related to a specific implementation of the method and depend on the particular adopted dielectric material and thickness. If we assume that the self-alignment methods illustrated by the reported works can be replicated also with other selections of dielectric materials and layer thicknesses, the primary characterizing parameter remains the overlap length. In terms of dielectric layer thickness, the selected works report figures of at least several tens of nanometers (e.g., 65 nm as in the study by Gold et al.[113]), and here we assume that this will be the best achievable range for future implementation of these kinds of techniques.

Overall, combining the illustrated rules-of-thumb with the results achieved in the literature, it is to be expected that future organic devices optimized for high-frequency operation will have a minimum equivalent overlap length, sum of the geometrical overlap of both electrodes and "equivalent overlap" due to fringing field, in the order of 200 nm, which is sufficiently low for achieving GHz operation.

3.5. Self-Heating Effects in Ultra-Scaled Devices

The downscaling of the device dimensions required to enable high-frequency operation brings along an often overlooked issue: the increased impact of self-heating on the performance of OFETs. The current flow across the device, along with the

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Table 4. Selection of electrode self-alignment techniques for organic transistors, alongside with the ranges of achieved overlap lengths and width-normalized overlap capacitance.

Technique	Overlap (single electrode) [nm]	Capacitance per unit width (both source/drain electrodes) [pF mm^{-1}]	Refs.
Self-aligned gate by Noh et al.	200–1000	0.7–1.1	[13]
PANI conversion	–	2.5–10[a),b)]	[115]
UV-NIL 1	200	0.12	[113]
UV-NIL 2	210	0.3–0.46[a)]	[34]
UV-NIL 3	30	–	[114]
High-speed R2R UV-NIL	2000	–	[119]
Wetting-based roll-off	470	0.37[a)]	[118]

[a)]Our calculation from reported data; [b)]Not reported whether single electrode or both electrodes.

voltage drop associated with the device operation, induces the generation of a thermal power per unit area according to[120]

$$P_{\mathrm{th}} = \frac{V_{\mathrm{ds}}\, I_{\mathrm{d}}}{WL} = \frac{1}{2}\,\frac{\mu C_{\mathrm{diel}}}{L^2}\left(V_{\mathrm{gs}} - V_{\mathrm{T}}\right)^2 V_{\mathrm{ds}} \tag{7}$$

P_{th}, in turn, induces a temperature rise that depends on the dissipation properties of the materials constituting the device and the surrounding environment.

For non-downscaled OFETs with moderate performance (e.g., $\mu = 0.1$ cm^2 V^{-1} s^{-1}, $C_{\mathrm{diel}} = 5$ nF cm^{-2}, $L = 50$ µm, and voltage bias of 40 V), the generated power density is 0.64 W cm^{-2}. However, for the downscaled dimensions and electrical performance required for 100 MHz–1 GHz operation (e.g., $\mu = 1$ cm^2 V^{-1} s^{-1}, $C_{\mathrm{diel}} = 100$ nF cm^{-2}, $L = 1$ µm, and voltage bias of 10 V), the same calculation yields $P_{\mathrm{th}} = 5$ kW cm^{-2}, posing huge challenges into the appropriate design of heat dissipation strategies.

Self-heating effects have previously been observed in amorphous silicon, polysilicon, and metal-oxide semiconductors. In the field of organics, cases of thermal runaway reaching temperatures in excess of 200 °C (**Figure 9**a) and destructive breakdown of the devices (Figure 9b) have been shown.[121]

Such studies in the field of organic transistors are rare, with a few examples where this effect has been shown to be active, leading to non-idealities originated by trap generation or temperature dependence of the mobility.[122–124] An additional element of complication is introduced for the case of organic semiconductors, in which charge transport is usually thermally activated, thus introducing a positive feedback for the self-heating process. Uncontrolled thermal runaway could ultimately occur, leading to the breakdown of the device. Direct measurements of the temperature rise in an operating OFET on silicon substrates has shown that the device channel temperature can reach values in excess of 54 °C.[125]

This issue is particularly exacerbated in consideration of the fact that the applications of organic electronics, which are based on the conformability/flexibility of the devices, require the use of materials and substrates with low thermal conductivity. In conventional silicon electronics, the main path for heat dissipation flows through the silicon substrate, which has a thermal conductivity ≈150 W m^{-1} K^{-1}. The use of plastic substrates, or even glass, exhibiting thermal conductivities in the range 0.1–1 W m^{-1} K^{-1}, severely complicates the dissipation of the excess heat.[92]

Recently, Kheradmand-Boroujeni et al. have realized a vertical organic transistor structure operating in the kiloampere per square centimeter current density regime. Such a device structure is capable of offering a huge performance in terms of speed of operation, but is also prone to suffer from severe thermal stress when operated in DC, due to the high driving current density and associated temperature rise. To characterize the small-signal transistor parameters, the authors proposed and implemented an approach relying on pulsed operation, in which the device is turned on, measured, and turned off within a time frame in the order of 10 µs. With this method, the authors could measure $f_{\mathrm{t}} = 40$ MHz at a bias voltage of 8.6 V, free of self-heating effects.[30] The authors propose that this kind of device is suitable for the implementation of applications in which the high-performance organic transistor suffering from self-heating stress in DC operation is only turned on for short period of time. These kinds of applications could include pulse-mode wireless data transfer or switching power converters.

In general, more efficient dissipation strategies should be devised in order to implement applications that require

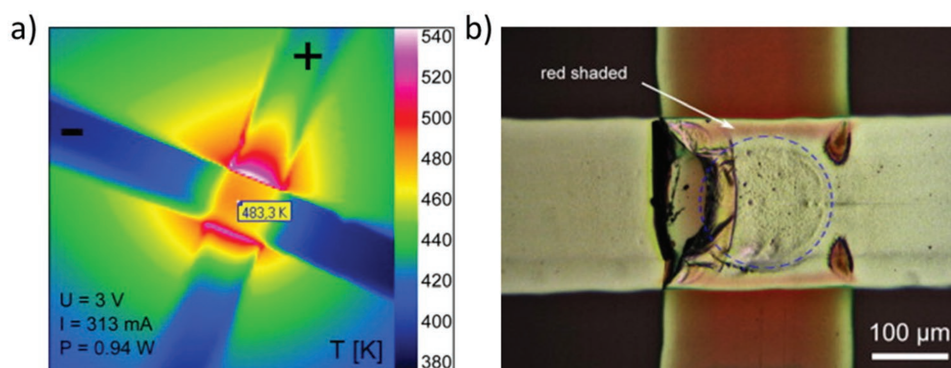

Figure 9. a) Thermal image of an organic device consisting of C_{60} sandwiched between two electrodes in a crossbar structure, shortly before thermal breakdown. Temperatures of 483 K in the center are reached. b) Picture of a similar device after breakdown. Reproduced with permission.[121] Copyright 2012, Elsevier.

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continuous operation of a device generating high power density. Some authors have proposed the integration of metal wirings and heat pipes in the dielectric layer to remove hotspots generated by excessive heat.[92] An additional option is to adopt flexible substrates with increased thermal conductivity, in order to offer a path for heat dissipation and contain the temperature increase.[120]

Flexible substrates with improved thermal dissipation properties can, for example, be achieved through polymeric composites with high thermal conductivity. These materials embed inorganic fillers with high thermal conductivity (e.g., boron nitride, aluminum nitride, aluminum oxide) in the polymer matrix and can reach thermal conductivities in excess of 10 W m^{-1} K^{-1}, which is one to two orders of magnitude higher than conventional polymer-based flexible substrates.[126–129] Overall, thermal management will be one of the limiting factors for the downscaling of organic devices on flexible substrates, and new models and approaches will have to be developed, possibly derived from the ones already elaborated in the field of silicon electronics to address analogous issues.[130]

4. Conclusions and Outlook

Winning the challenge of fabricating high-frequency organic devices and circuits and combining GHz operation with the mechanical properties of organic devices on ultra-thin, conformable substrates, fabricated via high-throughput, cost-efficient production methods will unlock a plethora of disruptive applications based on distributed, low-cost, conformable electronics. The combination of these features will provide ultra-thin surfaces characterized by nonconventional form factors with basic data transmission capabilities, which will allow imagining, designing, and realizing applications overcoming the mechanical limitations that prevent the adoption of hybrid solutions, integrating conventional silicon chips with large-area sensors.

Winning this challenge requires to carefully consider an ample set of problems, to design new powerful strategies to overcome these obstacles and finally to integrate the envisioned solutions into a comprehensive scheme taking all these issues into consideration. In addition, the envisioned scheme should solely adopt fabrication processes that allow for the future implementation of cost-effective mass-production facilities.

In this progress report, we have analyzed a set of five important challenges to this goal, in order to spur and inspire the scientific community, while also providing a set of guidelines for the next steps of the roadmap to GHz organic transistors. First, we have shown that a range of approaches to obtain sufficiently high intrinsic mobilities is available, which includes solution-based techniques. However, to exploit this performance, and considering the regime where the electrode overlap is required to be low, it is of paramount importance to reduce the specific contact resistance ρ_c to record-low figures. Second, we have reviewed the available set of upscalable fabrication techniques capable of resolutions down to the micron scale, identifying a variety of solutions for the realization of the OFET electrodes and channel. Third, we have analyzed the implications of the device downscaling in terms of requirements for the thickness of the dielectric layer in order to reduce/avoid short-channel effects. As a guideline, we proposed an approach already used for silicon SOI devices, which identifies a critical minimum channel length depending on the thickness and permittivity of the semiconductor and dielectric layers. Then, we examined the impact of the fringing capacitance in determining the parasitism of low-overlap structures optimized for high-frequency operation. We proposed a simple model to aid in the design of these kinds of structures and in the prediction of the frequency performance. We then reviewed and suggested a variety of available techniques to self-align the electrodes of the OFETs, in order to realize these low-overlap structures with scalable processes. Finally, we briefly considered some implications in terms of self-heating of high current density in aggressively downscaled transistors, and identified some options for the choice of a substrate material with improved thermal conductivity properties, in order to implement flexible, high-frequency devices.

To conclude, we propose a revised scenario with respect to the simple roadmap illustrated in the introduction to Section 3 (see Table 2), in which we integrate the insight provided by these analyses. As a result, we propose to consider the specific contact resistance as a defining parameter in place of the intrinsic mobility, due to the fact that, as of now, it is the limiting factor for micron-sized transistors. Differently from Table 2, we exclude here the possibility of true zero-overlap structures: the minimum achievable L_{ov} will be 100 nm, which encompasses the contributions of the fringing field and of the best reported geometrical overlap, in agreement with the conclusion of Section 3.4. Moreover, L_{ov} also influences the achieved contact resistance in the following estimations, in accordance to the current-crowding model in the regime of narrow electrodes (please note that the fringing field is accounted for in the calculation of the contact resistance, in the form of "equivalent overlap" as illustrated in Section 3.4).

The results of the calculation (**Table 5**) highlight clearly how, within this revised scenario, the specific contact resistance is the main factor in determining the order of magnitude of the achievable operational frequency, even when μ_{int} is fixed to 10 cm^2 V^{-1} s^{-1}. A similar conclusion has already been drawn by Klauk in terms of R_cW, and we here substantiate further this aspect for the case of staggered devices where the injection is described by current crowding. In such case, considering also the requirement for low capacitive parasitism and thus narrow electrode overlap, the process of charge injection is within a regime where the interfacial and bulk transport properties are dominating. In this context, ρ_c is the defining parameter for the achievable performance in terms of μ_{eff} and, in turn, f_t. However, extreme reduction of the overlap is always detrimental below a point depending on the magnitude of ρ_c, due to reduced injection performance. In any case, the reduction of L enhances the achieved f_t. It should be noted that we did not include in our models the dependencies of ρ_c on the mobility, bias, and dielectric capacitance, which are likely to promote the injection as they increase, thus improving the frequency values shown here. More accurate models can be developed in the future, to integrate this picture. Finally, in addition to the

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Table 5. Calculated transition frequencies for OFETs with the indicated channel lengths L, overlap length L_{ov}, and specific contact resistance ρ_c, for a supply voltage of 10 V and for μ = 10 cm^2 V^{-1} s^{-1} and for C_{diel} = 100 nF cm^{-2}.

L [µm]	L_{ov} [µm]	Specific contact resistance [Ωcm^2]		
		0.01	0.001	0.0001
1	1	47 MHz	229 MHz	403 MHz
1	0.1	13 MHz	120 MHz	653 MHz
0.8	0.3	33 MHz	269 MHz	926 MHz
0.8	0.1	16 MHz	147 MHz	869 MHz
0.5	0.3	43 MHz	368 MHz	1560 MHz
0.5	0.1	23 MHz	216 MHz	1484 MHz
0.3	0.1	32 MHz	308 MHz	2389 MHz

guideline illustrated by this table, the designer should also consider the requirement for the dielectric layer thickness (which depends on the actual selected materials) and should select an appropriate thermally conductive substrate.

To conclude, high-frequency OFETs in the range 100 MHz–1 GHz are in sight and, while some requirements can already be satisfied with techniques and materials available today, some other aspects require additional effort. To aid the community in the exciting path toward this achievement, we revised the current scenario and proposed an updated roadmap, together with a set of tools for the design and development of new materials, processes, and fabrication schemes. We also believe that a feasible route must be devised to achieve high-frequency operation through a cost-effective, efficient process flow. Solution-based and direct-writing, maskless techniques can play an important role toward this achievement, thus we proposed, within each section, a set of processes of this kind that, in our opinion, hold a potential for overcoming current bottlenecks. While hoping that the insights we illustrated within this report can be of inspiration for the community, we also invite the researchers to explore new ideas to integrate solution-based and direct-writing methods in their process flow for high-frequency OFETs and circuits.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

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