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Simplified down sampling factor based modified SVPWM technique for cascaded inverter fed induction motor drive

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ABSTRACT

This paper presents a rivew, investigation and performance analysis of novel down samples factor based modified space vector PWM is called clamping SVPWM technique for cascaded Multilevel Invereter fed to Induction motor drive. In this paper the reference sine wave generated as in case of conventional off set injected SVPWM technique is modified by down sampling factor the reference wave by order of 10. The performance analyses of this modulation strategies are analyzed by apply for five level, seven level, nine level and eleven level inverter. The performance analysis of cascaded inverter interms of line voltage, stator current, speed, torque and total harmonic distortion. The results are depicting that PD PWM is more effective among the four proposed PWM technique. It is observed that the CSV Pulse width modulation ensures excellent, close to optimized pulse distribution results compared to SPWM technique and also 11-level inverter beter performance in case of low THD and better foundemental output voltages comapared to 5, 7, 9-level inverter. The proposed technique has been simulated using MATLAB/SIMULINK software. This proposed technique can be applied to N-level multilevel Inverter also.

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1. INTRODUCTION

Multi-level diode clamped voltage fed inverters are recently becoming very popular for multi-megawatt power applications. The main advantage of such an inverter topology is voltage division, i.e., the output voltage is produced through small steps of voltage, and therefore the individual switches are submitted only to these small voltages steps [1, 2]. The other advantages are low harmonic distortion at output, low *dv/dt* and extended range of under modulation. But it has the disadvantages like the increased number of switching devices and the complex control algorithm. Another important topology, named Cascade H-Bridge (CHB), has fewer components to achieve the same number of output voltage levels [3, 4].

In addition, several modulation and control strategies have been developed or adopted for multilevel inverters including the following: multilevel sinusoidal pulsewidth modulation (PWM), multilevel selective harmonic elimination, and space-vector modulation (SVM). The results of a patent search show that multilevel inverter circuits have been around for more than 25 years. An early traceable patent appeared in 1975, in which the cascade inverter was first defined with a format that connects separately dc-sourced full-bridge cells in series to synthesize a staircase ac output voltage [5].

In this paper presents proposed down sampling based clamping SVPWM control strategy of three-phase five level, seven level, nine level and eleven level inverters are compared for THD. The paper mainly deals with the computation and the comparison of the motor harmonic losses of proposed CSV PWM solutions and with the selection of the solutions providing the best results. Finally, the drive harmonic losses will be compared for each levels. Special attention is dedicated to the latest and more relevant industrial applications of these inverter. Finally, the possibilities for future development are addressed.

2. GENERALIZED DOWN SAMPLING FACTOR BASED CLAMPING SVPWM FOR CASCADED MULTILEVEL INVERTER

The down sampling-based clamping SVPWM technique proposed by Lipo is based on SVM and the modification improved the vector sequences of the switching space. An offset voltage is required in the three phases' references of the inverter, calculated by (1) to center the active vectors within the switching period. Different pulse width modulation strategies are used in multilevel medium and high-power conversion applications [6]. They can generally be classified into three categories such as Multistep, staircase frequency switching strategies, which synthesise the AC voltage by adding rectangular waveforms by means of the multilevel concept, and which often use pre calculated switching angles. Space vector PWM strategies, which have been extended from two level SVPWM technique and have been applied to three phase multilevel inverter. Carrier based PWM strategies the vertically shifted carrier scheme (LSCPWM) can be easily realizable on any digital controller. This scheme comes with three different techniques such as PD, POD and APOD. And the horzatically shifted carrier scheme as Phase Shifted Carrier PWM (PSCPWM) is the common PWM for cascaded MLI [7]. The main parameters of the modulation process are shown in Figure 1. In conventional SVPWM for multilevel inverters to find the switching time duration, for different inverter vectors, the mapping of the outer sectors to an inner sub hexagon sector is to be done. The switching inverter vectors corresponding to the concrete sectors are switched and the time periods premeditated from the mapped inner sectors. Implementing such a scheme in multilevel inverters will be very difficult, because higher number of sectors and inverter vectors are present. And in this method the computation time is increased for real time application. In carrier based PWM scheme aproper offset voltage is added to sinusoidal references before comparing with carrier waves, to attain the performance of a SVPWM [8] shown in Figure 2.

$$Vas = (Vm\,Sin(wt)) \quad (1)$$

$$Vbs = (Vm\,Sin(wt - 120)) \quad (2)$$

$$Vcs = (Vm\,Sin(wt + 120)) \quad (3)$$

$$Voffset = \frac{-(V\,max + V\,min)}{2} \quad (4)$$

After that we adding the three reference singals with Voffset voltage we generated reference singal shown in below equations Van, Vbn and Vcn.

$$Van = (Vas + Voffset) \quad (5)$$

$$Vbn = (Vbs + Voffset) \quad (6)$$

$$Vcn = (Vcs + Voffset) \quad (7)$$

In this paper, a simple technique to determine the offset voltage (To be added to the reference phase voltage for PWM generation for the entire modulation range) is presented, based onely on the sampled amplitudes of the reference phase voltages. The proposed modified reference PWM technique presents a simple way to determine the time instants at which the three reference phases cross the triangular carriers. To obtain the maximum possible peak amplitude of the fundamental phase voltage in linear modulation, the procedure for this is given in [9, 10]. After the modified SVPWM technique output, we can do the Down sampling of the order 10 each phase shown in Figure 2. Which is also sometimes called decimation, down sampling used for reduces the sampling rate and removes the samples from the signal. Whilst maintaining its length with respect to time. Some mathematically analysis to find out the down sampling factor shown in bellow, we can used descriptive time is 2e-6, sampling frequency is one by descriptive time (10^6/2), number of samples per phase is the ratio of sampling frequency by fundamental frequency such as 10k samples,

in order reduced the down sampling by order of 10 such as 1k samples. By using the down sampling based modified space vector PWM technique such as PD, POD, APOD and PS. We can observe the reduced the THD in output line to line voltages. From (1), (2), (3), (4), (5), (6) and (7) we get generate reference wave compared to triangular carrier shown in Figure 3 to Figure 6. Is shown in the waveform results generated by adding the offset voltage described in with the reference sinusoidal waveform.

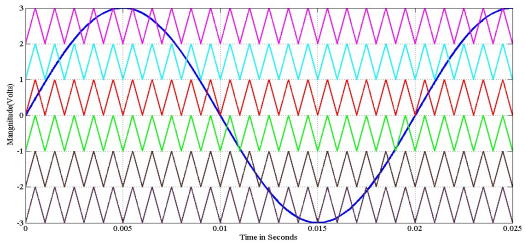

Figure 1. PDSPWM

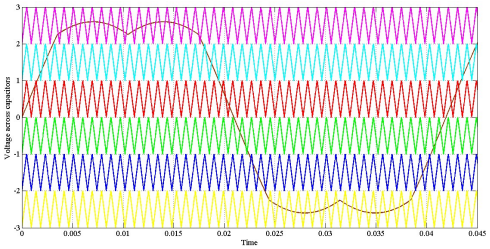

Figure 2. Modified SVPDPWM

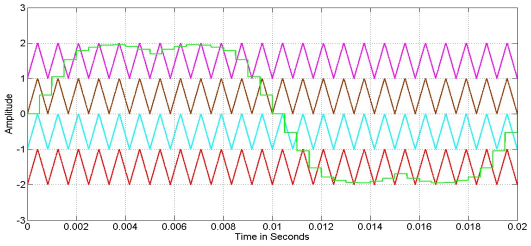

Figure 3. CSV PDPWM

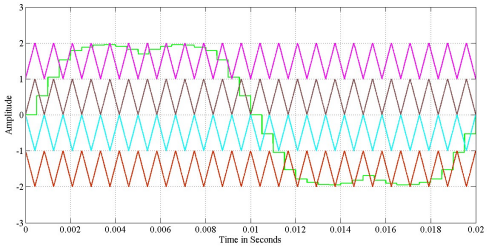

Figure 4. CSV PODPWM

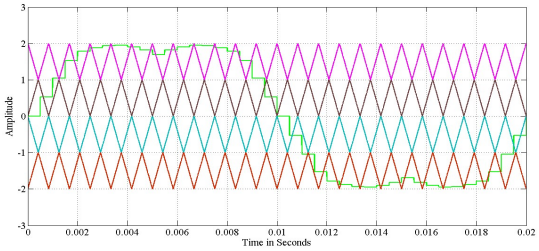

Figure 5. CSV APODPWM

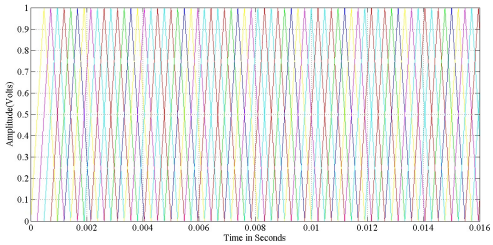

Figure 6. CSV PSPWM

3. SIMULATION RESULTS AND DISCUSSION

Simulations have been carried out in MATLAB/Simulink environment for the 5-level, 7-level, 9-level and 11-level CMLI by implementing CSVPDPWM, CSVPODPWM, CSVAPODPWM and CSVPSPWM techniques. A 3-phase induction motor is considered as load for this scheme. Simulation results are analyzed by computing %THD and plotting harmonic spectra of different PWM techniques. The circuit arrangement for N-level CMLI is shown in Figure 7. This circuit can be used to implement all other PWM techniques related to SPWM, THIPWM and modified SVPWM. The necessary simulation parameters for CMLI are as follows: the total DC-link voltage for a phase- 400V, reference wave frequency-50Hz, and carrier frequency- 10KHz. The harmonic analysis of 5-level CMLI for CSVPDPWM, CSVPODPWM, CSVAPODPWM and CSVPSPWM technique with triangular carrier wave is shown in Figure 8 to Figure 11. The magnitude of fundamental component in the CSVPSPWM with triangular carrier technique produces more value of 430.4V. The CSVPDPWM with triangular carrier gives better total harmonic distortion of 17.10%. In the five-level single phase CMLI contain two H-bridges with series connections with the output phase voltage is 5-level and line voltage is 9-level of the inverter and we can obverse CSVPODPWM and CSVAPODPWM contain apporximetely value of THD and fundmental output voltages.

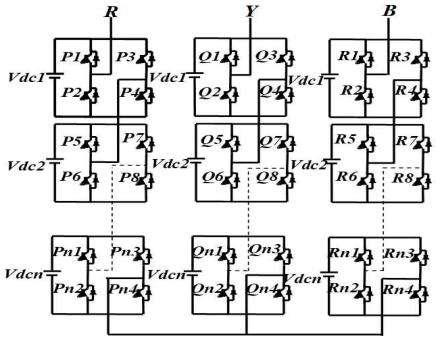

Figure 7. Three phase N-level CMI inverter

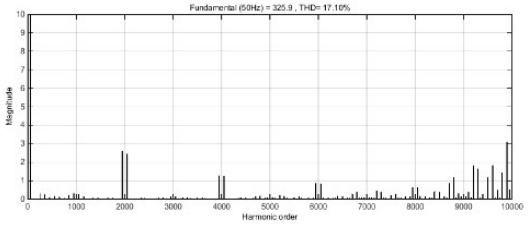

Figure 8. Five level THD for CSV PDPWM

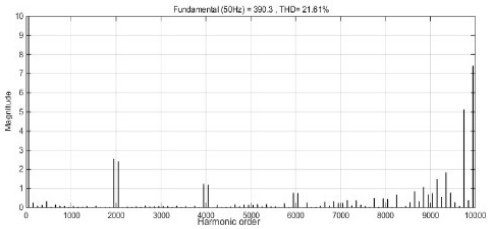

Figure 9. Five level THD for CSV PODPWM

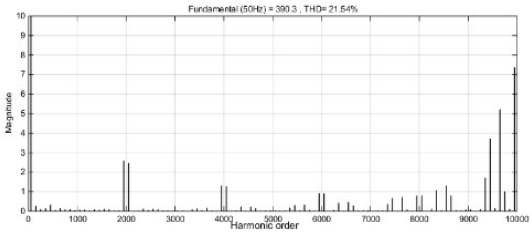

Figure 10. Five level THD for CSV APODPWM

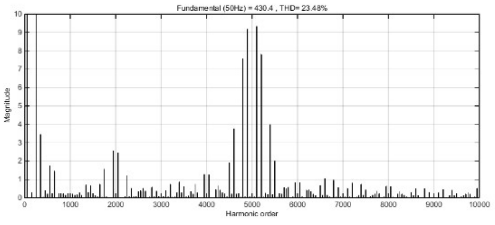

Figure 11. Five level THD for CSV PSPWM

The harmonic analysis of 7-level CMLI for CSVPDPWM, CSVPODPWM, CSVAPODPWM and CSVPSPWM technique with triangular carrier wave is shown in Figure 12 to Figure 15. The magnitude of fundamental component in the CSVAPODPWM with triangular carrier technique produces more value of 651.2V. The CSVPDPWM with triangular carrier gives better total harmonic distortion of 11.65%. In the 7-level single phase CMLI contain three H-bridges with series connections with the output phase voltage is 7-level and line voltage is 13-level of the inverter and we can obverse CSVPODPWM and CSVAPODPWM contain apporximetely value of THD and fundmental output voltages.

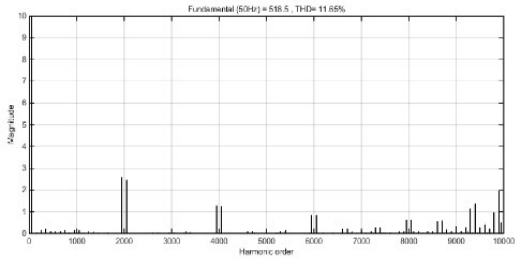

Figure 12. Seven level THD for CSV PDPWM

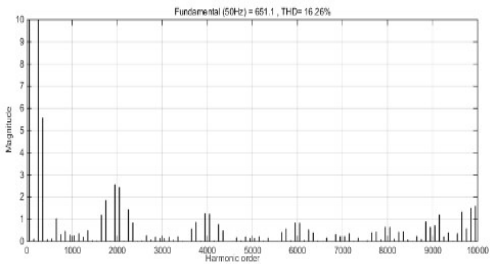

Figure 13. Seven level THD for CSV PODPWM

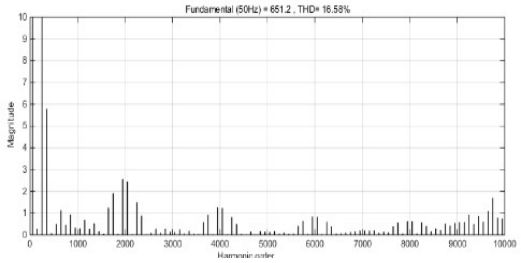

Figure 14. Seven level THD for CSV APODPWM

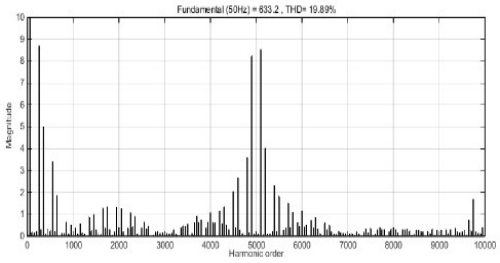

Figure 15. Seven level THD for CSV PSPWM

The harmonic analysis of 9-level CMLI for CSVPDPWM, CSVPODPWM, CSVAPODPWM and CSVPSPWM technique with triangular carrier wave is shown in Figure 16 to Figure 19. The magnitude of fundamental component in the CSVPDPWM with triangular carrier technique produces more value of 826.5V. The CSVPDPWM with triangular carrier gives better total harmonic distortion of 8.90%. In the 9-level single phase CMLI contain four H-bridges with series connections with the output phase voltage is 9-level and line voltage is 17-level of the inverter and we can obverse CSVPODPWM and CSVAPODPWM contain apporximetely value of THD and fundmental output voltages.

The harmonic analysis of 11-level CMLI for CSVPDPWM, CSVPODPWM, CSVAPODPWM and CSVPSPWM technique with triangular carrier wave is shown in Figure 20 to Figure 23. The magnitude of fundamental component in the CSVPODPWM and CSVAPODPWM with triangular carrier technique produces more value of 1017 V. The CSVPDPWM with triangular carrier gives better total harmonic distortion of 6.68%. In the 11-level single phase CMLI contain four H-bridges with series connections with the output phase voltage is 11-level and line voltage is 21-level of the inverter and we can obverse CSVPODPWM and CSVAPODPWM contain apporximetely value of THD and fundmental output voltages. This proposed modified down sampling factor-based clamping SVPWM signal generation does not involve region identification, sector identification or look up tables for switching vector determination required in the conventional multilevel SVPWM technique. This scheme is computationally efficient when compared to conventional multilevel SVPWM scheme. We can observe that nuber of level is increased the total harmonic distortion is reduced and fundementel output voltage is increases shown in Table 1. The comparison to other conventional SVPWM technique and all other SPWM technique.

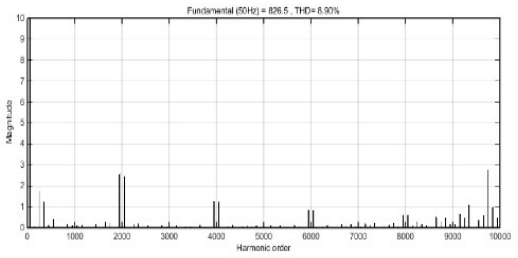

Figure 16. Nine level THD for CSV PDPWM

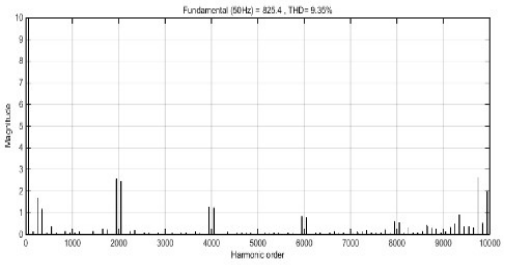

Figure 17. Nine level THD for CSV PODPWM

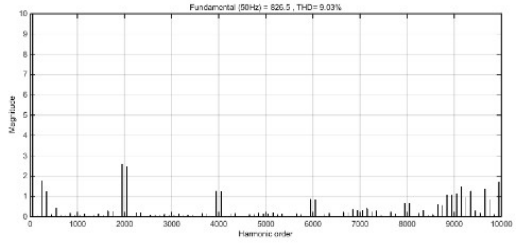

Figure 18. Nine level THD for CSV APODPWM

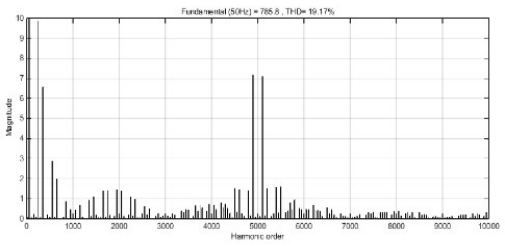

Figure 19. Nine level THD for CSV PSPWM

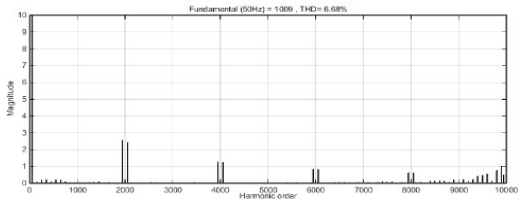

Figure 20. Eleven level THD for CSV PDPWM

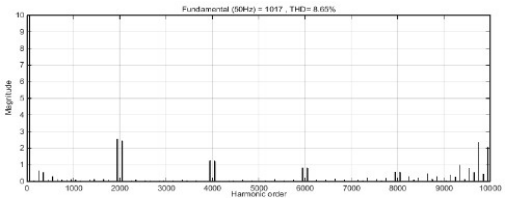

Figure 21. Eleven level THD for CSV PODPWM

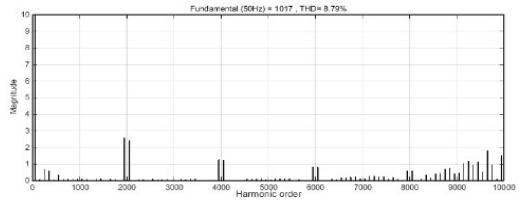

Figure 22. Eleven level THD for CSV APODPWM

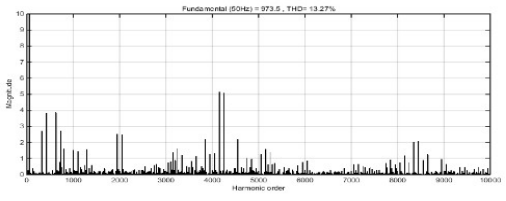

Figure 23. Eleven level THD for CSV PSPWM

Table 1. Comparison of THD for different level of the cascaded inverter fed induction motor

Output voltage levels	Techniques	THD (%) @ Fundamental Output Voltage
Five-level	CSV-PDPWM	17.10 (325.9)
	CSV-PODPWM	21.61 (390.3)
	CSV-APODPWM	21.54 (390.3)
	CSV-PSPWM	23.48 (430.4)
Seven-level	CSV-PDPWM	11.65 (518.5)
	CSV-PODPWM	16.26 (651.1)
	CSV-APODPWM	16.58 (651.2)
	CSV-PSPWM	19.89 (632.2)
Nine-level	CSV-PDPWM	8.90 (826.5)
	CSV-PODPWM	9.35 (825.4)
	CSV-APODPWM	9.03 (826.5)
	CSV-PSPWM	19.17 (785.8)
Eleven-level	CSV-PDPWM	6.68 (1009)
	CSV-PODPWM	8.65 (1017)
	CSV-APODPWM	8.79 (1017)
	CSV-PSPWM	13.27 (973.5)

4. CONCLUSION

In this paper dealy with a novel down sampling factor based modified SVPWM technique so called Clamping Space vector Pulse width modulation (CSVPWM) technique. The reference sine wave generated as in case of conventional off set injected SVPWM technique is modified by down sampling the reference wave by order of 10. The comparison of THD of the proposed control strategies for 5, 7, 9 and 11-level inverter. When compared, it is obvious that CSV-PDPWM is the most efficient control strategy with low THD and increases the fundamental output voltages. The THD analysis, line voltages, stator currents and speed and torque of the machine are calibrated and compared confirming the good-quality waveforms.

APPENDIX

Table 1. Specification of induction motor

Parameters	Specifications
Input voltage	400VRMS(PhasePhase)
Inverter voltage	100(Volts)
Rotor speed	1440(RPM)
Fundamentalfrequency	50(Hz)
Switching frequency	10K (Hz)
Reference speed	1500(RPM)
Frequency modulation	200
Amplitude modulation	0.866
Sampling factor order	10

ACKNOWLEDGMENT

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Mr. Ravi Kumar Bhukya was born in Mahabubabad (Warangal), Telangana, India. He obtained B.Tech. in Electrical and Electronics Engineering from JNTU University, Hyderabad in 2010 and M.Tech. in Power and induristal drives Engineering in 2013 from Jawaharlal Nehru Technological University, Hyderabad. His research interests include Power Electronics, Drives, Power converters and Multi level inverter. Presently he is pursuing Ph. D. in Osmania University, Hyderabad, INDIA.

Dr. Satish Kumar Peddapelli is an Associate Professor in the Department of Electrical Engineering, University College of Engineering, Osmania University, Hyderabad. He has completed his B.Tech in EEE from JNTU, obtained his M.Tech in Power Electronics from JNTUH and his Doctorate in the area of Multilevel Inverters in the year 2011 from JNTUH. His areas of interests are Power Electronics, Drives, Power Converters, Multi Level Inverters, Special Machines and Hybrid Power Systems. He is the Principal Investigator for three Major Research Projects funded by UGC, SERB, worth around 9 Lakhs, 21 Lakhs and Indo-Sri Lanka joint research project worth of around 25 lakhs from the Department of Science and Technology, New Delhi. He has more than 60 publications in International Journals and has attended and presented papers in 28 International Conferences. He authored one text book. He received the **"**Best Teacher award" from the state Government of Telangana on 5th September, 2014.