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A novel multilevel inverter with reduced switch count

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ABSTRACT

This paper presents a multilevel inverter with reduced number of switches to produce a five level output. PWM technique (pulse width modulation) has been used to trigger the MLI switches. It gives reduced harmonic. This proposed topology is connected with R-load and RL-load. Four signals are generated for switching on the multilevel inverter (MLI) switches by comparing four level triangular waveform with sine wave. In this proposed topology two switches are reduced from the conventional Cascaded five level inverter. The simulation analysis has been done by MATLAB/SIMULINK.

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1. INTRODUCTION

A multilevel inverter is capable of generating higher level in the output voltage waveform. It gives desired AC output voltage from several DC sources. MLI is used in high current and high voltage applications. When the level of output voltage increases, it reduces the total harmonic distortion in the output voltage waveform. Multilevel inverters are used in the areas where we need high power such as power conditioning, industrial motor drives and power grid. Surya Suresh [1] demonstrates the new topology has the advantage of its reduced number of devices compared to conventional topology and can be extended to any number of levels. The harmonic reduction is achieved by selecting proper switching angles. Divya subramaniyan [2] proposed inverter provides higher quality output with lower power loss compared to other conventionl inverters. Sivagamasundari [3] based on analysis of cascaded multilevel inverter using hybrid PWM method. The proposed topology reduces the number of power switches when compared to the conventional cascaded inveter. Vinod kumar, et al., [4] designed single phase five level inverter is simulated using multicarrier PWM and conventional method. The THD in output voltage of MLI using multicarrier PWM is less compared to conventional method. Panchal, et al., [5] proposed a three phase fivel level cascaded inverter and modified cascade inverter for asynchronous motor. From simulation analysis modified cascade multilevel inverter is very beneficial over the cascaded MLI. Praveen [6] proposed a new topology with low number of switches to increase the levels of output voltage. Proposed work of single phase cascade inverter output voltage total harmonic distortions is reduced and efficiency is improved. Dubey [7] presents design and analysis of cascade H-bridge multilevel inverter using sinusoidal pulse width modulation technique. From this analysis quality of power improved by using multilevel inverter. Lavanya Raj [8] proposed a five level inverter with multicarrier pulse width modulation technique and embedded matlab s-function. Total harmonic distortion is low for multicarrier PWM. The THD can be further reduced by using

s-function. Balamurugan, et al., [9] deals with different modulation strategies of MLI. Ankit Dubey [10] proposed a various multilevel inverter topologies and control methods.

2. CASCADED MULTILEVEL INVERTER

A single phase cascaded inverter is shown in Figure 1. It is proposed to develop a desired AC output voltage from several DC sources. This is the most common type of inverter and use separate DC source. Each separate DC source is connected to a H-bridge inverter. Each inverter can generate three different output voltage levels +Vdc, 0, -Vdc. +Vdc can be obtained by switching on S1 and S4. To obtain –Vdc switches S2 and S3 are turned on wheares 0 can be obtained by turning on four switchs S1, S2, S3 and S4. The number of voltage levels in a CHB inverter can be obtained from m= (2N+1). Where N is the number of H-bridge. In CHB inverter the voltage levels is always an odd number. It requires less number of components among all multilevel inverter to achieve the same number of voltage levels. Switching states of cascaded multilevel inverter is shown in Table 1.

Table 1. Switching states of cascaded five level inverter

Voltage (V0)	S1	S2	S3	S4	S5	S6	S7	S8
0	0	1	0	1	1	0	1	0
Vdc	1	0	0	1	0	1	0	1
2Vdc	1	1	0	0	1	1	0	0
-Vdc	0	1	0	1	1	0	0	1
-2Vdc	0	0	1	1	0	0	1	1

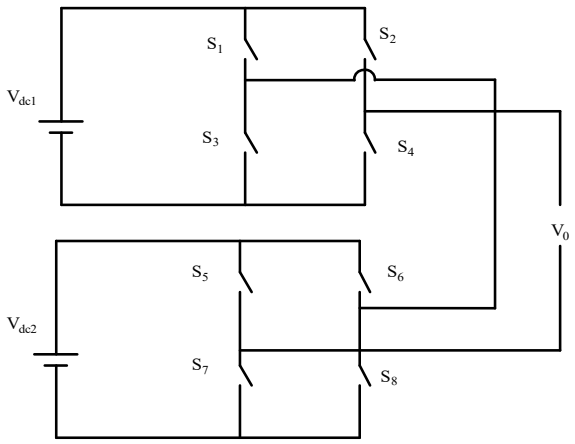

Figure 1. Cascaded multilevel inverter

3. PROPOSED MULTILEVEL INVERTER

Figure 2 shows the proposed five levels multilevel inverter. Due to higher number of switching devices, the inverter circuit size and cost also increases. In this paper the proposed topology provides higher number of output voltage levels with reduce number of switches. In this topology five levels of output +2Vdc, Vdc, 0, -Vdc and -2Vdc are obtained by one module. Here (m-1)/2 number of DC sources are used to produce m levels in the output voltage. In this inverter, PWM technique is employed to achieve high quality output voltage. Four signals are generated by comparing four level shifted triangular waveforms with single sine wave. Switching states of five level inverter with reduced number of switches is shown Table 2.

Table 2. Switching states of five level inverter with reduced number of switches

Voltage (V0)	S1	S2	S3	S4	S5	S6
0	0	0	0	0	0	0
Vdc	0	1	0	0	1	0
2Vdc	0	1	1	0	1	0
-Vdc	1	0	0	1	0	0
-2Vdc	1	0	0	0	0	1

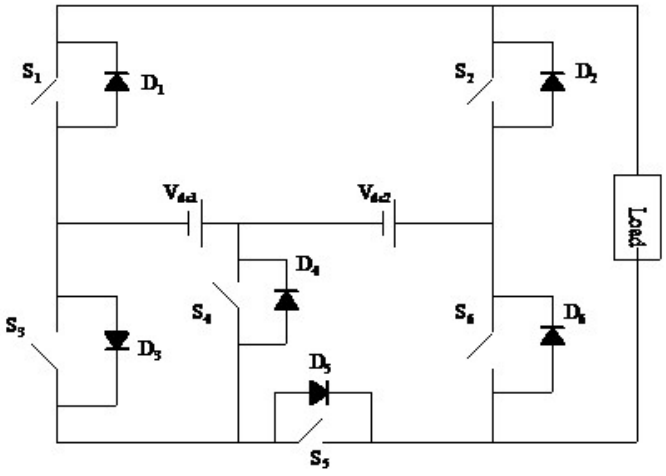

Figure 2. Proposed multilevel inverter with reduced number of switches

4. SIMUATION AND RESULT ANALYSIS

The simulation circuit was developed for proposed inverter with R and RL load. The simulated output voltage is shown for only one sample value of ma=1. For simulation analysis, the following parameter values are used: Vdc1=Vdc2=100V, R=100ohms, L=3mH F, fc=2000Hz and fm=50Hz.

4.1. Proposed circuit with R load

It consists of five switches with two DC sources. The load can be assumed as R-load. The proposed multilevel inverter with R-load circuit has been shown in Figure 3. Figure 4 and Figure 5 show the output voltage and harmonic spectrum of proposed inverter with R-load. Table 3 shows the measurement across multilevel inverter for R-load.

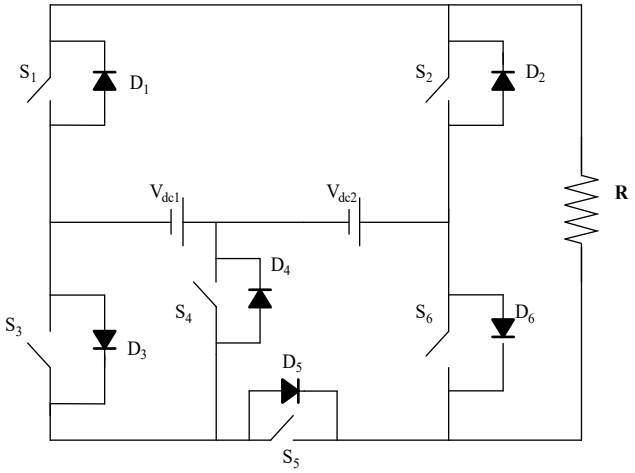

Figure 3. Proposed multilevel inverter with R-load

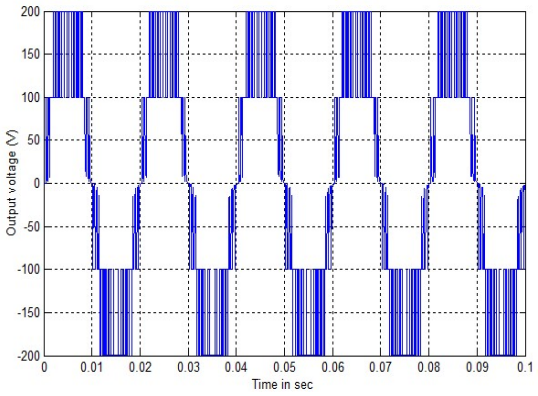

Figure 4. Output voltage of the proposed inverter with R-load

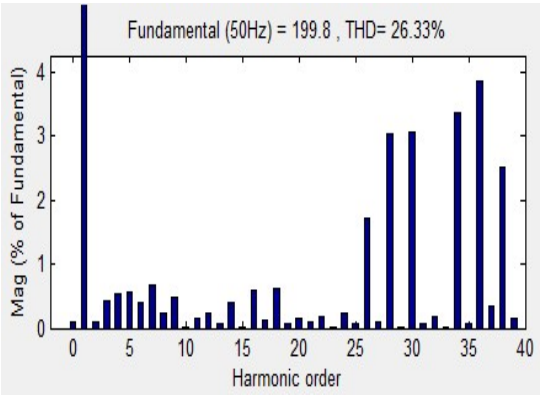

Figure 5. Harmonic spectrum of output voltage of the proposed inverter with R-load

Table 3. Measurement across multilevel inverter for R-load

ma	Peak value (V)	RMS value (V)	DC component	THD (%)
1	199.8	141.3	0.2137	26.33
0.9	180	127.3	0.2624	32.87
0.8	160	113.2	0.0098	37.38
0.7	140	98.96	0.4624	40.46
0.6	120.2	85.02	0.3832	41.65

FFT analysis has been done for generated output voltage by using MATLAB. Total harmonic distortion observed for this R-load to be 26.33% as shown in Figure 5.

4.2. Proposed circuit with RL load

The load can be assumed as RL-load. The proposed multilevel inverter with RL-load circuit has been shown in Figure 6. Figure 7 and Figure 8 display the output voltage and harmonic spectrum of proposed inverter with RL-load. For switching on the MLI switches PWM scheme has been used. Four signals are generated by comparing four level triangular waveform with sine wave. FFT analysis has been done in the MATLAB for generated output voltage waveform. Total harmonic distortion observed to be 29.40% as shown in Figure 8. Table 4 shows the measurement across multilevel inverter for RL-load.

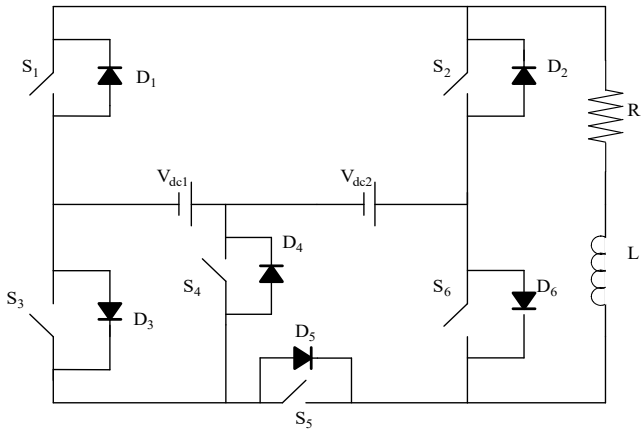

Figure 6. Proposed multilevel inverter with RL-load

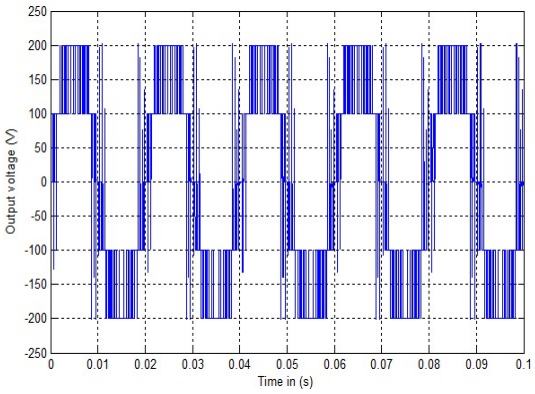

Figure 7. Output voltage of the proposed inverter with RL-load

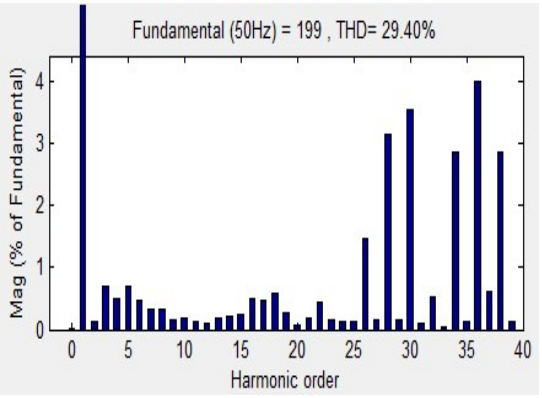

Figure 8. Harmonic spectrum of output voltage of the proposed inverter with RL-load

Table 4. Measurement across multilevel inverter for RL-load

ma	Peak value (V)	RMS value (V)	DC component	THD (%)
1	199	140.7	0.0556	29.40
0.9	179.1	126.6	0.1913	35.58
0.8	158.8	112.3	0.5075	41.39
0.7	137.9	97.49	0.4161	47.54
0.6	117.6	83.15	0.3341	51.47

5. CONCLUSION

In this paper the simulation results of single phase five level inverter with R and RL load are analysed by MATLAB/SIMULINK. The output voltage and THD spectrum of various load are obtained. From Table 3 and Table 4 the proposed inverter with R-load gives less %THD and its give better performance than RL-load.

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