PCB Embedding Technology for 5G mmWave Applications

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ABSTRACT

The roll out of 5G networks has already started worldwide and in the near future it is expected to dramatically reshape the wireless communication landscape. Nevertheless, a number of technical challenges still need to be addressed in the most recent packaging development approaches, such as the implementation of a large number of connections at high data rates, exhibiting high gain to compensate for the high free space loss at millimeter wave frequencies.

Within the European funded project SERENA, partners from academia, research and industry are collaborating to address these topics and develop an integration platform, based on PCB embedding technology, capable of reducing size, power consumption and design time and complexity, while at the same time achieving increased performance, energy efficiency and transmitted output power. In particular, PCB embedding technology offers the potential to realize an integrated RF electronics module containing ICs for RF signal generation and antennas with very short interconnects in a single package, thus minimizing the signal path losses. In the framework of the SERENA project, new RF materials suitable for the embedding of components are applied in combination with high gain GaN and SiGe dies for the first time to implement a scalable System-in-Package operating at 39 GHz.

Different concepts for the realization of RF modules with embedded GaN and SiGe dies were outlined and first demonstrators are currently being fabricated at Fraunhofer IZM to develop a process technology which allows 1) using RF laminate and prepreg materials to embed the dies for modularization and 2) handle non-standard die pad metallization, such as 3 µm thick Au pads, within the embedding process sequence. Test structures were also fabricated for the electrical assessment of the package configuration and the applied technology. Specifically, package interconnects and integrated patch antenna arrays were designed, simulated with the aid of a 3D full-wave simulator and measured after fabrication. It was shown that the interconnects realized in the PCB embedding technology have good RF properties in terms of insertion loss and return loss and are well suited for System-in-Package RF modules. The antennas also exhibit good radiation characteristics in terms of the gain and efficiency.

The paper will give a detailed description of the fabrication process development and will discuss the technological approaches in depth.

DEVELOPMENT OF EMBEDDING PROCESS OF NEW PACKAGING AND SYSTEM-INTEGRATION PLATFORM

The embedding of semiconductors into the build-up of printed circuit boards is an established process in principle. It is briefly depicted with the focus on a high power dissipating component in Figure 1. The chip is mounted onto the printed circuit board core using a thermal and electrical highly conducting interface. Preferentially power chips are sintered (low temperature silver sintering) to the dissipative copper structure of the core. Subsequently the chips are embedded into the build-up (epoxy resin & glass-compound and copper foil) of the circuit board by lamination. Contact pads of the chip are opened by laser drilling, followed by electroplating for electrical contact formation and final definition of the copper artwork.

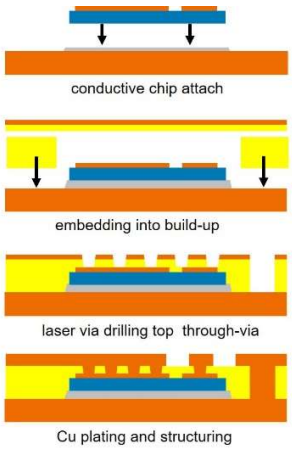

Figure 1: principle of the embedding process of chips into the build-up of the printed circuit board.

Revised version of original paper, containing acknowledgement of funding through H2020 programme and reference to patent for figure 6

In the frame of the SERENA, essential process steps had to be considerably adjusted and re-developed in order to meet technical specifications and to deal with the constraints given by the MMICs. In Table 1 typical specifications for the conventional embedding process are juxtaposed to those of SERENA.

Technical parameter	Standard	SERENA
Contact pad metal	Copper	Gold
Contact thickness [µm]	min. 10	3
Contact diameter [µm]	150	100
Power dissip. [W/mm]	0,8	1,5
Build-up material	High-T_g	High frequency
Compound build-up	No	Yes
Air bridge structures	No	Yes

Table 1: Comparison embedding specifications

For the mounting of highly dissipating chips onto the PCB substrate typically Ag-sintering is preferred. That requires high pressure to be applied onto the chips in order to compress the sinter paste. However, since the MMIC chips used in SERENA are equipped with air gap structures which are not compatible with the required bonding pressure, the conventional approach is excluded. Therefore a novel sinter glue (NAMICS H9890-7) was used, which requires only minor bonding pressure when placing the chip followed by glue curing (temperature load only). The trade-off is a lower thermal conductivity of the interconnection compared to conventional sintering.

The embedding into the build-up layer was adapted in two respects. First, a build-up material compatible with high frequency application was used (Megtron 7N, equipped with cavities to take up the MMICs). Second, a full area Ajinomoto-build-up film with a thickness of 10 µm was placed over the MMICs in order to provide a thin on-top encapsulation of the chips. The stack was layed-up and tacked together in a vacuum applicator and subsequently laminated according to PCB processing. The resulting build-up is schematically depicted in Figure 2.

Figure 2: Embedded MMICs in a build-up structure consisting of Megtron 7N (green) and Ajinomoto-build-up film (yellow).

Laser drilling through the build-up film onto 3 µm thick Au-contact pads is critical using an UV-laser for vias of 20 µm diameter. Since ablation of metal can't be prevented in the drilling process conventional processing typically requires 10 µm metal on the contacts in order allow reproducible and safe processing. Process parameters had to be considerable adjusted in order to be compatible with the thin contacts. Results of the explorative study were monitored by SEM and FIB. With a set of appropriately selected parameters reasonable results for the drilling were obtained, Figure 1.

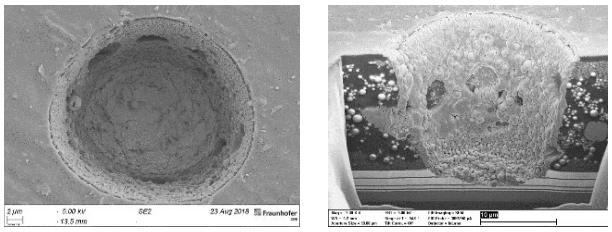

Figure 3: SEM top view and FIB cross section of laser-via through the build-up film onto the contact pad of the MMIC

The contacts of the MMICs are electrically interconnected by sputtering of a Ti-plating base (100 nm) and initial Cu (300 nm) followed by electroplating of 20 µm copper, see Figure 4.

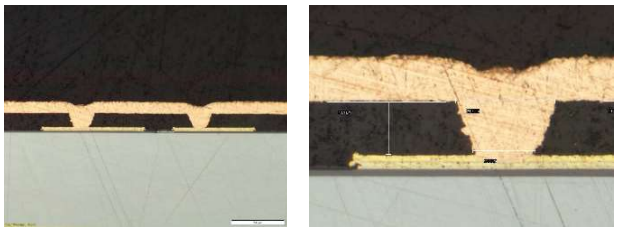

Figure 4: Cross sections through plated µ-vias. Bottom diameter 16 µm, top diameter 25 µm.

Copper is finally structured in a conventional subtractive photolithography process to yield the wiring architecture on top of the embedded chip, see Figure 5.

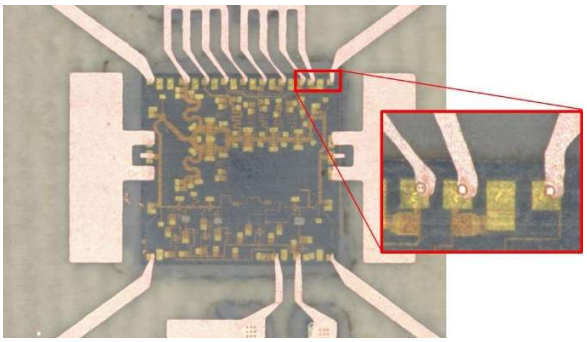

Figure 5: Top view of the embedded MMIC with connected by plated µ-vias to the copper circuitry

Using the adapted processes the module including embedded semiconductors, capacitors, thermal dissipation structures and antennas as depicted schematically in Figure 6 was realized. The build-up strategy consists of the following steps: First a PCB core (2 copper layers) is fabricated, with a circuity containing the bond pads for capacitors and the MMIC chips. Thermal vias to the

connecting layer on the reverse side are placed directly under the bond pads of the MMICs. Components are mounted onto the core, embedded into the build-up and electrically connected as described in the previous sections. By sequential lamination and structuring of further build-up layers antenna structures are integrated into the module: on top of the ABF-film and routing layer 100 µm Megtron7N and 25 µm copper is build-up and connected to the copper structures below by micro-vias. The copper layer is used as ground plane. Next, a thick build-up consisting of 300 µm Megtron7N and 25 µm copper for the antenna structures is added. Electrical connections to the copper structures in lower layers are mechanically drilled blind holes with conformal copper metallization.

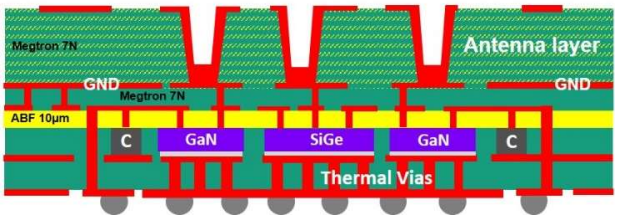

Figure 6: High frequency embedded and antenna module (European Patent EP3346548B1)

The module is mounted to the system board by a solder bump array, see Figure 7. Power supply, mixer, filter units and a heat sink are integrated in the system board.

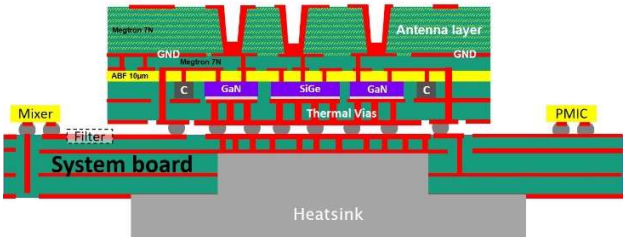

Figure 7: Schematics of the complete system with the embedded & antenna module mounted to the system board.

ELECTRICAL REQUIREMENTS FOR RF INTEGRATION

The developed embedding technology allows for component integration such as ICs and discrete passives as well as planar patch type antennas. 3D placement of components in the embedding package offers high integration density and the possibility of short electrical interconnects. For good RF performance the modules should offer good signal integrity (SI) and power integrity (PI), integration of antennas as well as the possibility for miniaturization and potentially low manufacturing cost. Good SI can be achieved by RF design of interconnects taking into account substrate and trace geometry, choice of material as well as control of process tolerances. Sufficient PI calls for the integration of decoupling capacitors close to the active components and low-impedance design of the power supply network of the package. Integration of millimetre-wave antenna benefits from low-loss substrate materials to achieve high radiation efficiency. SI, PI and mmWave antennas are therefore improved by a technology that is based on low loss substrate materials and allows for good control of metal trace geometry.

The Megtron 7N PCB used as substrate material in the embedding process offers low dielectric loss and low permittivity around 5G mmWave frequencies. The geometrical requirements of short interconnect length especially for the antenna feed, a low impedance power supply network and the integration of the antenna at the top lead to the design of the package cross section as shown in Figure 8.

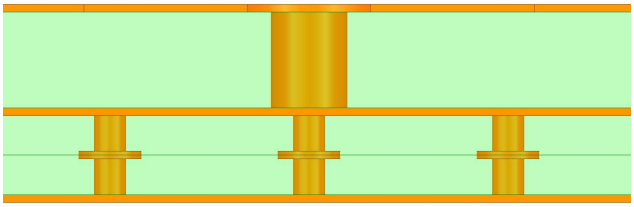

Figure 8 Cross section of RF front-end package using embedding technology

ANTENNA

For the realization of the package-integrated antenna a planar Microstrip patch array configuration was designed and realized. The antenna array is integrated in the top dielectric layer of the package (cf. Figure 8) with the antenna patches and the signal traces of the power splitter on the top layer and a ground plane in the layer below. The array is made up of two approx. $\lambda/2$ spaced patch antennas that are excited by inset feeds to achieve good impedance match to the feeding Microstrip line. The RF signal is routed along vias through the substrate layers to the RFICs in the embedding layer.

The antenna elements were designed using 3D EM field simulations in AnsysEM HFSS taking into account the dielectric material parameters of the substrate material and the geometry of the substrate cross section. Following the antenna design the feeding network including the via geometry and the RF signal traces were designed. The antenna array has overall dimensions of 6.9x21.9 mm^2 not including the feeding network.

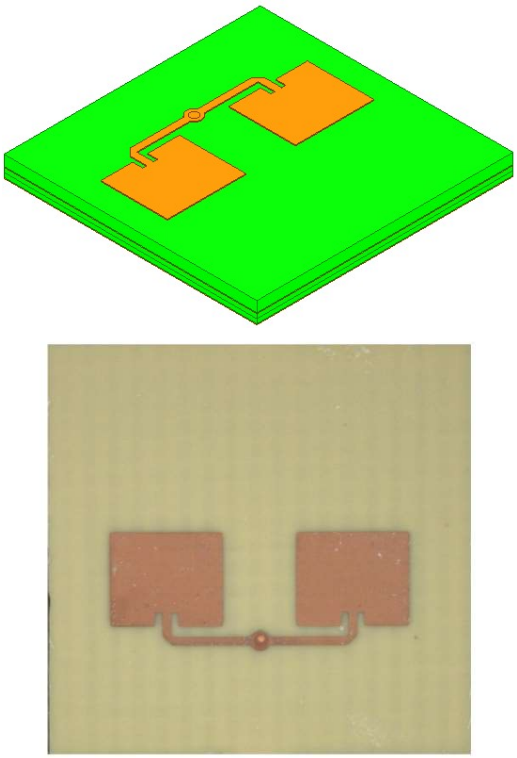

Figure 9 Developed integrated antenna for embedding package. Top: Simulation model including the two-element patch array and feeding network. Bottom: top view of fabricated antenna array

Test structures were derived from the antenna design by adding a coaxial connector to the backside. S-parameters were measured (Figure 10) using a network analyzer. The measurement set-up was calibrated to account for cable loss between instrument and antenna feeding point. The measurement results show good matching in the frequency range from 37-38.1 GHz. The simulation results show similar behavior with a slight frequency shift.

The radiation pattern of the antenna array was measured in an anechoic chamber with the antenna array (antenna under test – AUT) and a reference horn antenna connected to a vector network analyzer. Measurement and simulation of radiation pattern show good match (Figure 11).

Table 2 summarizes the performance characteristics of the antenna test structures.

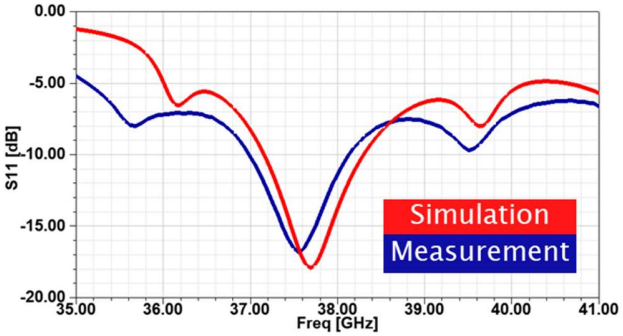

Figure 10 Return loss measurment and simulation results for two-element antenna array text structure.

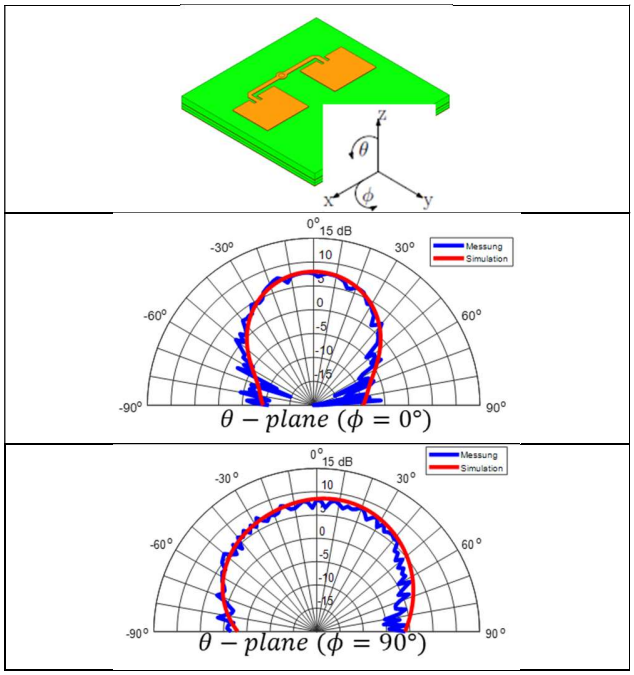

Figure 11 Radiation pattern of two-element antenna array test structure. Top: Coordinate system, middle: cut of radiation pattern in H-plane, bottom: cut of radiation pattern in E-plane

	Resonance frequency [GHz]	S11 [dB]	Bandwidth [GHz]	Peak Gain [dB] θ plane (ϕ=0)	Peak Gain [dB] θ plane (ϕ =90)
Simulation	37.71	- 17.8	1.14	7.9	8.5
Measurement	37.56	-16.8	1.15	7.6	8.25

Table 2 Key performance characteristics of antenna test structure

INTERCONNECTS

The electrical performance of the RF interconnects were characterized based on a strip transmission line embedded in the package consisting of the RF signal trace in the center of two ground planes above and below. The structure was designed for 50Ω RF characteristic impedance.

In order to characterize the interconnect technology a 15.2 mm strip transmission line was augmented with fixtures at the end to facilitate connection to the RF measurement set-up (Figure 12).

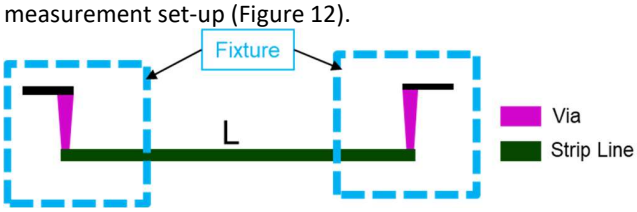

Figure 12 Sketch of RF interconnect test structure

The test structure was designed using 3D EM field simulations.

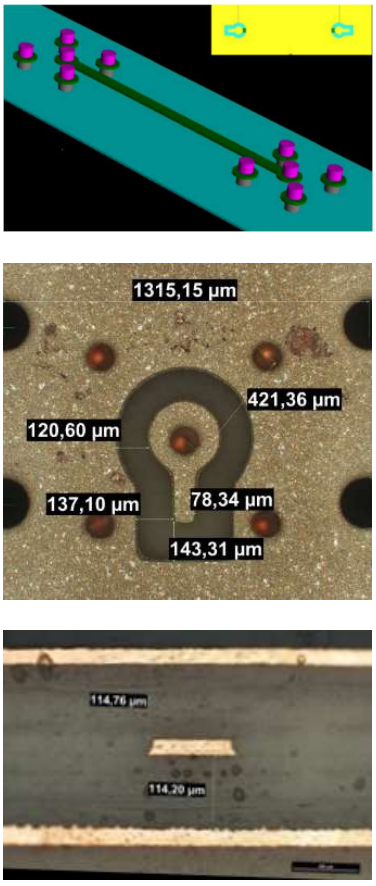

Figure 13 RF interconnect test structure for RF characterization of PCB embedding technology. Top: Simulation model of strip transmission line with fixtures, Middle: top view of RF pads, Bottom cross section through substrate

The test structure was measured using a vector network analyzer. The test structures were contacted using RF probes connecte to the instrument. The set-up was calibrated at the tip of the probes to account for insertion loss and return loss of the cables and the probes.

The comparison shows good match between measurement and simulation (Figure 14, Table 3).

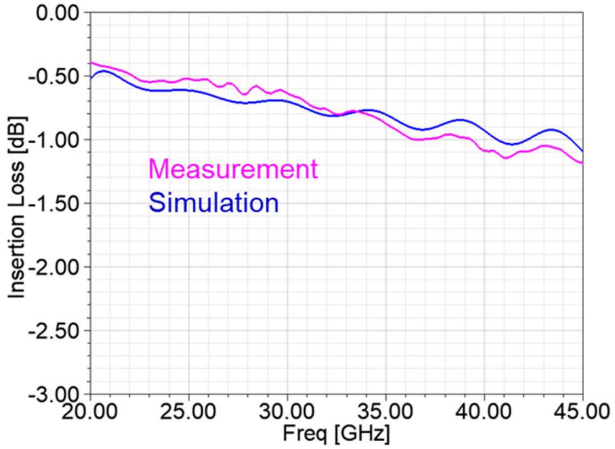

Figure 14 Insertion loss of embedding technology test structure

S-parameter at 39 GHz	Mag S_{11} [dB]	Mag S_{21} [dB]
Measurement	-23.90	-0.99
EM-Simulation	-33.43	-0.85

Table 3 S-parameter of interconnect test structure

SUMMARY AND CONCLUSION

A PCB embedding technology was developped for 5G communication applications was developped and the RF characteristics of package integrated antennas and RF interconects were investigated using test structures. The characterization of the test structures show good RF performance in terms of antenna radiation characteristics and interconnect performance.

The developped embedding technology is suited for realization of integrated 5G communication modules including RFICs and antenna arrays.

ACKNOWLEDGEMENT

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