International Journal of Reconfigurable and Embedded Systems (IJRES)
Vol. 8, No. 3, November 2019, pp. 185~193
ISSN: 2089-4864, DOI: 10.11591/ijres.v8.i3.pp185-193

Design and implementation of reduced power energy efficient binary coded decimal adder

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Article Info

Article history:

Received Jul 25, 2019
Revised Sep 15, 2019
Accepted Sep 27, 2019

Keywords:

Constant correction
Binary to Excess Six Conversion
Ripple carry adder
Terahertz optical asymmetric demultiplexer

ABSTRACT

This paper presents a novel architecture for low power energy binary represented decimal addition. The proposed BCD adder uses Binary to Excess Six Converter (BESC) block for constant correction to adjusts binary outputs exceeding 9 to correct decimal values and exploits the inherent advantage of reduced delay and switching, due to elimination of long carry propagation in second stage addition as in conventional design and switching OFF of the BESC block for decimal outputs less than 9. The proposed BESC-BCD adder has been designed using VHDL code and synthesized using Altera Quartus II. Experimental results demonstrates that the proposed decimal adder can lead to significant power savings and delay reduction compared to existing BCD adders which is realised in better power-delay product(PDP) performance. For example the PDP saving of the proposed BESC-BCD adder for a 1 digit and 2 digit addition implementations are 11.6% and 16.05% respectively, compared to the best of the designs used for comparison.

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1. INTRODUCTION AND RELATED WORK

The binary numbering system is mostly followed in computer systems today. But in earlier days, computer systems were merely based on the decimal (base 10) numbering system rather than the binary numbering system. Decimal based computer systems are popular in systems targeted for business/commercial applications. In case of applications related to money transactions decimal arithmetic is better than binary arithmetic. Therefore, many software systems still specify the use of decimal arithmetic in their calculations. The need for efficient decimal arithmetic and its ever increasing applications in micro/minicomputers and microprocessor based equipment and appliances have been increasing.

The significance of BCD representation over binary representation is that it is fairly trivial to convert between the string representation of a decimal number and its BCD representation. This is particularly beneficial when working with fractional values, since fixed and floating point binary representations cannot exactly represent many commonly used values between zero and one (e.g., 1/10). Thus, BCD operations can be efficient when reading from a BCD device, doing a simple arithmetic operation (e.g., a single addition) and then writing the BCD value to some other device. Architectures and algorithms proposed to date on decimal arithmetic include: A novel BCD adder using redundant BCD addition [1]. The design involves simple conversion of a BCD number to redundant form, perform addition and reconvert the result back to BCD form. The extra conversion circuit used adds huge delay and increases complexity. Adder for decimal addition proposed in use speculative addition technique at the first stage [1]. The feature of the design is that it has a regular structure and the design of correction unit is independent

of the number of input operands. In another technique, used non-speculative addition which have lesser delay [2]. Some researches use reversible logic for the design of BCD adders [3-5]. The feature of reversible logic adders is that it performs well in terms of power dissipation and logic count, however it is prone to higher delay. In a pioneer work on BCD addition, used multiplexer for the addition of correction bits [6]. The use of multiplexers for constant correction reduces delay compared to the state of art approaches.

Proposed a BCD adder using analyzer circuit for carry generation [7]. The reduced number of gates in the critical path of correction circuit reduces the total delay of the circuit. In a novel architecture for BCD addition and subtraction using three major blocks viz [8]. PG block, prefix block and the correction block. Since the correction circuit is embedded within the pre-computing blocks the design complexity is less compared to the BCD adder in [9]. proposed a novel design for decimal (BCD) adder using Terahertz Optical Asymmetric Demultiplexer (TOAD) [10].

Proposed an architecture for decimal arithmetic which can also perform binary addition [11]. The circuit has lower delay, however the design of post correction circuitry poses problems for multi-bit operands. In a pioneer work, used Carry Look Ahead(CLA) addition for the first stage being followed by carry network and correction logic in the second and third stages [12]. The architecture in demonstrate better delay reduction compared to the architecture in [11, 12], however the first stage CLA adder increases hardware complexity. A two stage correction free adder for BCD addition is proposed [13]. In stage 1, the MSB three bits of a four bit BCD number are added. In second stage the result from stage 1 is added with the LSB. Since the circuit doesn't have any extra circuit for constant correction the latency is very less compared to the previous approaches. Implemented a new architecture of BCD adder using 6-input LUTs and fast carry chains [14]. The proposed design demonstrates better critical path delay reduction however the circuit is prone to more power dissipation. Proposed a new architecture for BCD addition using flag bit generation [15]. The architecture uses flag bit computation and flag inversion logic to generate the decimal equivalent for outputs exceeding 9. The speed of the architecture is high due to use of Carry Select Adder (CSLA) [16] and CSK adder [17] for first stage addition, however it is prone to high power dissipation.

The basic objective of this work is to reduce power and latency in BCD addition by using BESC instead of 4-bit Ripple Carry Adder (RCA) as in conventional design for the correction constant addition for decimal outputs exceeding 9. The main advantage derived is realization of BESC with lesser number gates compared to a 4 bit RCA. The output of first stage adders and BESC block are passed through a multiplexer. The select signal for the multiplexer is generated from a control logic which produces 1 for sum values exceeding 9 and 0 else. The rest of the paper is organized as follows. Section 2 gives a brief description of BCD addition and the architecture of conventional BCD adder. Section 3 discusses about the design of proposed low power and energy efficient BESC-BCD adder. Section 4 presents the BESC logic and its detailed structure. The area and delay evaluation of the proposed and conventional decimal designs are discussed in section 5. In section 6, performance of the proposed BCD adder are discussed and compared with the previous approaches through experimental results. The implementation detail of the proposed design for a 2 digit addition is discussed in section 7. Section 8 gives a brief conclusion of the work done.

2. OVERVIEW OF BCD ADDITION

The addition operation of two decimal digits in BCD, together with a possible carry from previous least significant digits (assuming maximum value for input digits) viz, 9+9+1 would result in 19. The equivalent representation for the sum in the range 0 to 19 in binary is 0000 to 10011 and in BCD is 0000 to 1 1001(MSB 1 is carry and next four LSBs is BCD digit sum) and is shown in Table 1. It is seen from Table 1, that for the binary sum equal to or less than 1001 the corresponding BCD digit is the same. However, when the binary sum exceeds 1001, the result is invalid BCD and needs correction. The addition of $6(0110)_2$ to the binary sum converts it to the correct digit and a carry [3]. Based on the above methodology, the architecture of a 1digit BCD adder [3] is shown in Figure 1.

The input digits in binary are $A(A_3A_2A_1A_0)$ and $B(B_3B_2B_1B_0)$. S_3' S_2'S_1'S_0'are the sum outputs of the first stage 4 bit adder. The carry output C_N shown in Equation (1) will be one for sum exceeding 9 or else it will be 0. When C_N is 1, a correction constant 0110(6) will be added with S_3'S_2'S_1'S_0' by the second stage adder to produce the decimal adjusted output $S_3S_2S_1S_0$ and its realisation is shown in (2)-(5) :

$$C_N = C_{OUT} + S_3'S_2' + S_3'S_2' \quad (1)$$

$$S_0 = S_0' \quad (2)$$

$$S_1 = S_1' \oplus C_N \oplus C_1 \quad (3)$$

$$S_2 = S_2' \oplus C_N \oplus C_2 \quad (4)$$

$$S_3 = S_3' \oplus C_3 \quad (5)$$

Table 1. Binary and BCD equivalent representation for possible outputs of decimal addition

Decimal output	Binary Equivalent	BCD Equivalent
0	0000	0000
1	0001	0001
	-	
	-	
9	1001	1001
10	1010	1 0000
	-	
	-	
15	1111	1 0101
16	1 0000	1 0110
17	1 0001	1 0111
18	1 0010	1 1000
19	1 0011	1 1001

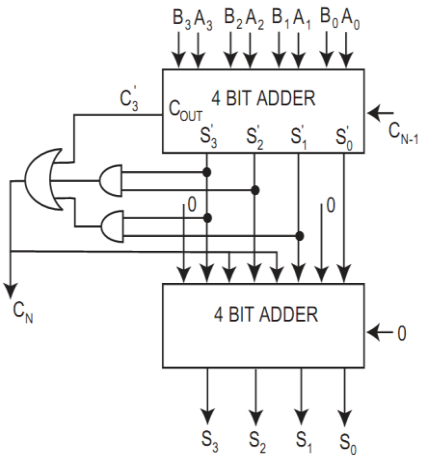


Figure 1. Block diagram of conventional BCD adder

3. PROPOSED BESC-BCD ADDER

The structure of the proposed BCD adder using BESC for constant correction addition is shown in Figure 2. In addition to the BESC unit, the proposed design consists of a 4 bit RCA, Carry generator and four 2:1 multiplexer (mux). The schematic of Carry generator is shown in Figure 3. When the output from first stage 4 bit RCA exceeds 9, Carry generator produces 1. The Carry generator output is used as the control/select signal for the four 2:1 multiplexer group shown as 8:4 mux in Figure 2. One input to the four 2:1 mux are the output bits of first stage adder ($S_3S_2S_1S_0$) and the other input is the BESC output ($M_3M_2M_1M_0$). The mux selects either of the inputs based on the control signal from Carry generator (C_{out}) to produce the output ($O_3O_2O_1O_0$) with C_{out} being the carry out bit. The main feature of the proposed decimal adder is the BESC unit which shows significant reduction in delay and switching due to elimination of carry propagation in second pair of RCA as in conventional design.

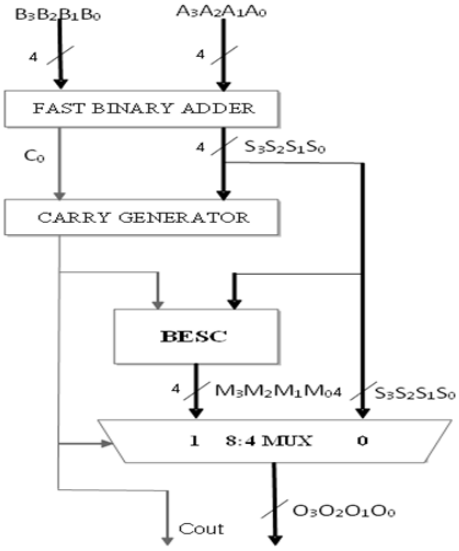


Figure 2. Block diagram of proposed BESC-BCD adder

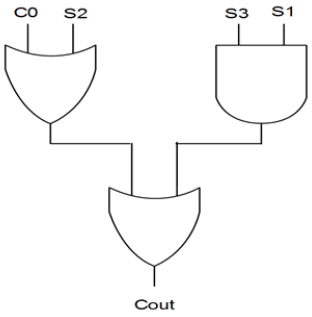


Figure 3. Schematic of carry generator

4. BESC

As stated in section 1, the objective of the work is to introduce BESC instead of a separate RCA for adding correction constant (0110:6) to adjust outputs exceeding 9 to correct decimal. A 4 bit BESC is used to replace 4 bit RCA for correction constant addition. The logic table which realises the binary to excess six conversions is shown in Table 2 and its schematic in Figure 4. **X–**represents don't care state.

Table 2. Logic table for binary to excess 6 conversion

C_0	S_3	S_2	S_1	S_0	M_3	M_2	M_1	M_0
0	0	0	0	0	X	X	X	X
0	0	0	0	1	X	X	X	X
0	0	0	1	0	X	X	X	X
-	-	-	-		X	X	X	X
-	-	-	-		0	0	0	0
0	1	0	0	0	0	0	0	0
0	1	0	1	1	0	0	1	1
0	1	0	1	1	0	0	1	1
0	1	1	0	0	0	1	0	0
0	1	1	0	0	0	1	0	0
0	1	1	1	1	0	1	1	1
0	1	1	1	1	0	1	1	1
1	0	0	0	0	1	0	0	0
1	0	0	0	0	1	0	0	0
1	0	0	1	1	X	X	X	X
1	0	0	1	1	0	0	0	0

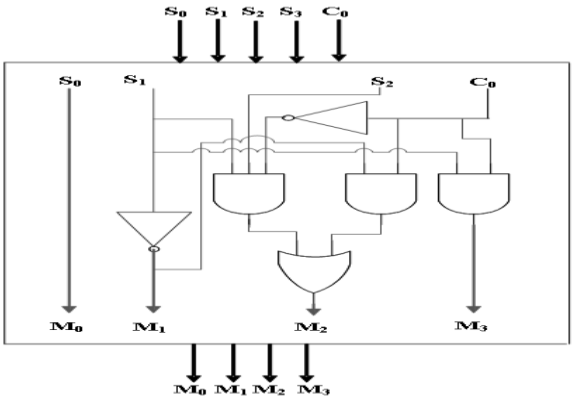


Figure 4. Schematic of BESC

$$M_0 = S_0 \quad (6)$$

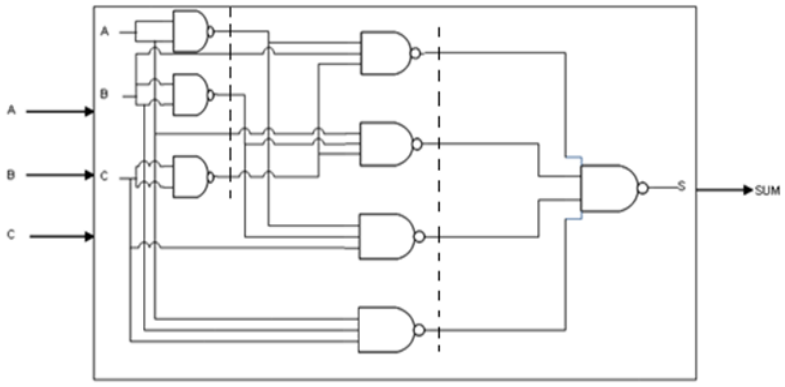
$$M_1 = \overline{S_1} \quad (7)$$

$$M_2 = C_0 \,\&\, S_1 \,\&\, S_2 + C_0 \,\&\, S_1 \quad (8)$$

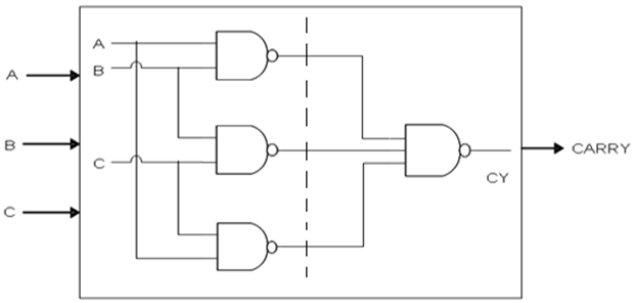
$$M_3 = C_0 \,\&\, S_1 \quad (9)$$

5. AREA AND DELAY EVALUATION OF PROPOSED BESC-BCD ADDER AND CONVENTIONAL BCD ADDER

Area and delay evaluation of the proposed and conventional designs are done based on their equivalent NAND implementation. The NAND implementation of basic elements viz., Full Adder (FA), NOT, AND and OR gates used in the proposed and conventional BCD adder designs are shown in Figure 5. We assume the delay of NAND gate to be 1 unit and area equal to 1 count. The gates in parallel between dotted lines perform parallel operation and we use only one gate delay in these cases for calculation of worst case delay of circuit/element. Based on the above approach, the delay and area of the individual elements that make up the proposed design is shown in Table 3. The area count and worst case delay of the proposed and conventional BCD adder designs are calculated as follows. The worst case delay is found by counting the number of NAND gates in the critical path and the area is evaluated by counting the total number of NAND gates that make up the circuit.



(a)



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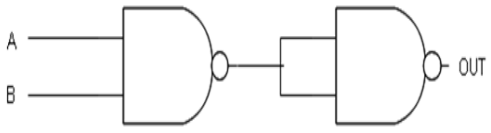

(c)

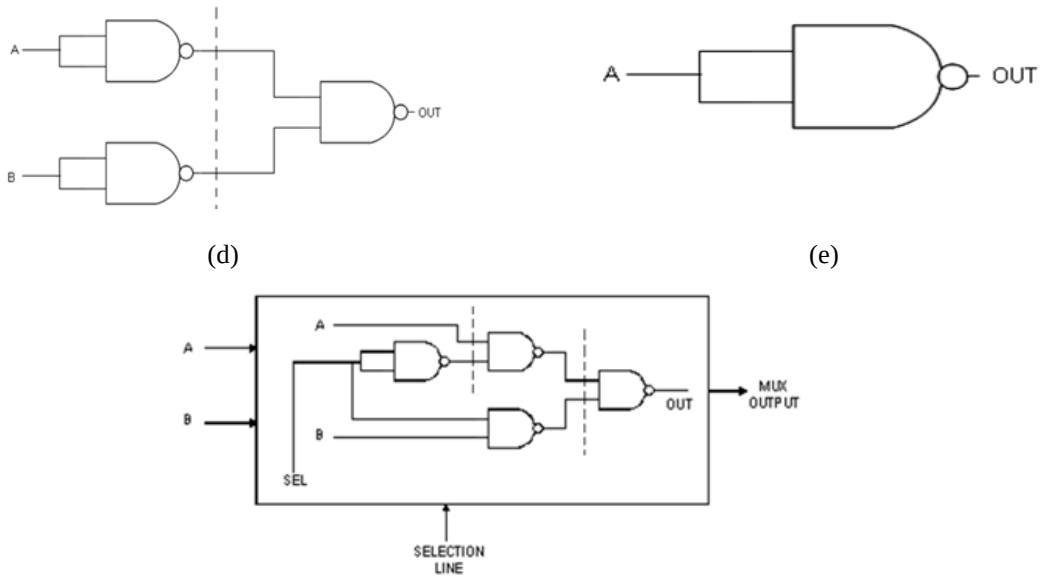

Figure 5. NAND implementation of, (a) Full adder sum, (b) Full adder carry, (c) NOT logic, (d) AND logic, (e) OR logic, (f) 2:1 Mux

Table 3. Area and delay of basic elements of BCD adder implemented using NAND logic

Element	Area	Worst case delay
Full adder	Sum:8 + Carry:4 =12	3
NOT	1	1
AND	2	2
OR	3	2
2:1 Mux	4	3

5.1. Area count evaluation

The steps that lead to the area count evaluation for the BCD adder designs shown in Figure 1 and Figure 2 are as follows. From Figure 1 it can be seen that 4 FA(1^{st} stage adder)+2 AND and 1 OR (Correction circuit)+4 FA (2^{nd} stage adder) make up the conventional BCD adder. Using Table 3 the NAND equivalent gate count of the decimal adder in Figure 1 is found to be (48+4+3+8) 103. Using a similar approach,the area count of the proposed BESC-BCD adder shown in Figure 2 is evaluated as 4 FA (1^{st} stage adder)+1 AND and 2 OR (Carry generator)+2 NOT and 3 AND and 1 OR(BESC)+16 NAND (4–2:1 mux) with corresponding NAND equivalent count being 83. The results of the evaluation are shown in Table 4. It is seen from Table 4 that the NAND equivalent Gate count of the proposed BESC-BCD adder decreases by 20 compared to the conventional BCD adder. Worst case delay estimates (in NAND equivalent) of Conventional and proposed BESC-BCD adders as shown in Table 5.

Table 4. Area count (in NAND equivalent) of the proposed BESC-BCD adder and conventional design

Basic Blocks	Conventional design	Area count	BESC-BCD design	Area count
1st stage adder	4 FA	48	4 FA	48
Correction circuit/Carry generator	2 AND+1 OR	7	1 AND +2 OR	8
2nd stage adder	4 FA	48	-	-
BESC	-	-	2 NOT+3 AND+1 OR	11
2:1 mux	-	-	4 NAND	16
Total		103		83

Table 5. Worst case delay estimates (in NAND equivalent) of Conventional and proposed BESC-BCD adders

Basic Blocks	Conventional design	NAND equivalent delay	BESC-BCD design	NAND equivalent delay
1st stage adder	4 FA	12	4 FA	12
Correction circuit/ Carry generator	1 AND+1 OR	4	2 OR or (1 OR+1 AND)	4
2nd stage adder	4 FA	12	-	-
BESC	-	-	1 NOT+1 AND+1 OR	5
2:1 mux	-	-	3 NAND	3
Total		28		24

5.2. Delay evaluation

We have evaluated the worst case delay of the proposed and conventional BCD adder designs as follows. The delay of conventional BCD adder shown in Figure 1 is 4 FA carry (1^{st} stage addition)+1 AND and 1 OR (correction circuit)+4 FA carry (2^{nd} stage addition). Based on the consideration of the delay values for individual elements (in NAND equivalent implementation) shown in Table 3, the worst case delay of conventional BCD adder is estimated to be (12+4+12) 28. Using a similar approach the delay of proposed BESC-BCD adder shown in Figure 2 is 4 FA carry (1^{st} stage addition)+1 AND/1 OR and 1 OR (Carry generator)+1 NOT and 1 AND and 1 OR(BESC)+3 NAND (2:1 Mux) with the corresponding NAND equivalent delay to be (12+4+5+3) 24. The results of the evaluation are shown in Table 5. It is seen from Table 5 that the delay of the proposed BESC-BCD adder decreases by 4 units compared to the conventional BCD adder [18].

6. EXPERIMENTAL RESULTS

The proposed BESC-BCD adder is designed using VHDL and synthesized using Altera Quartus II with EP2C35F672C6 device. Conventional BCD adder [19], Correction free BCD adder [13], Carry skip BCD adder [20] and Flagged BCD adder [15] are used for comparison. The designs used for comparison are also described using VHDL and synthesized using Altera Quartus II with the same device. The area, delay and total power dissipation results of proposed and previous designs are shown in Table 6. It is seen from Table 6, that the proposed BESC-BCD adder has lower power dissipation and reduced delay.

Table 6. Comparison of area, delay, power dissipation and PDP of proposed BESC-BCD adder and state-of the art designs

Parameters BCD Adders	Area (Number of LEs)	Delay (ns)	Static power dissipation (mW)	Total power dissipation (mW)	Energy dissipation-PDP (mW-ns)
Conventional design[3]	11	15.230	80.04	144.06	2194.03
Correction free[16]	29	13.326	80.05	147.02	1959.19
Carry skip[9]	15	17.100	80.02	138.36	2365.96
Flagged BCD-Using CSLA[20]	13	12.303	80.04	146.43	1800.7
Flagged BCD -Using CSK[20]	9	12.984	80.04	146.31	1899.1
Proposed-BESC BCD (RCA in 1^{st} stage)	11	11.815	80.01	134.75	1592.1
Proposed-BESC BCD (CSLA in 1^{st} stage)	13	11.657	80.01	137.32	1600.73
Proposed-BESC BCD (CSK in 1^{st} stage)	11	11.815	80.01	134.53	1589.47

Compared to all other architectures used for comparison, thanks to the BESC unit which realises constant correction addition with minimal switching and has fewer gates in the critical path. The energy dissipation represented as product of power and delay (PDP) of the Proposed BESC-BCD adder is 11.6% lower compared to the best of the previous designs used for comparison. The area of the proposed BCD adder represented in Logic Element (LE) count is low compared to Correction free [13] and Carry skip [20] BCD designs. However the proposed BESC-BCD adder show high LE count compared to the Flagged BCD design (with CSK in the first stage addition) [15].

7. IMPLEMENTATION OF PROPOSED BCD-BESC ADDER FOR TWO DIGIT ADDITION

To determine the functionality of the proposed BCD adder an implementation in 2 digit addition is done and is shown in Figure 6. The carry out of the first digit adder (C_{out}) is used as the carry input for 4 bit RCA in second digit addition. The performance parameters of 2 digit adder implemented with proposed BESC-BCD adder and other approaches are shown in Table 7. From the Altera Quartus II results, it is seen that 2 digit addition using proposed BESC-BCD adder designs exhibit lower delay and reduced total power dissipation compared to all other architectures used for comparison. The reduction in delay is due to realisation of second stage constant correction with 1 NOT+1 AND+1OR which eliminates the long carry propagation path as in Conventional BCD adder[3], Correction free [13], Carry skip [20] and Flagged BCD adder [15] designs. The better delay and power dissipation performance of the proposed BESC-BCD design demonstrates better PDP product of the proposed design compared to all other architectures used for comparison.

Table 7. Comparison of area, delay and power dissipation and their products of proposed BESC-BCD adder and state-of the art designs

Parameters BCD Adders	Area (Number of LEs)	Static power dissipation (mW)	Static power dissipation (mW)	Total power dissipation (mW)	Energy dissipation (PDP) (mW-ns)
Conventional[3]	24	89.05	89.05	172	3167.38
Correction free [16]	58	89.34	89.34	173.06	2825.38
Carry skip[9]	32	91.56	91.56	174.27	3680.58
Flagged BCD-Using CSLA[20]	25	80.14	80.14	175.39	2744.85
Flagged BCD -Using CSK[20]	21	86.83	86.83	169.22	2791.11
Proposed-BESC BCD (RCA in 1st stage)	21	80.09	80.09	158.75	2304.26
Proposed-BESC BCD (CSLA in 1st stage)	26	80.10	80.10	163.66	2323.32

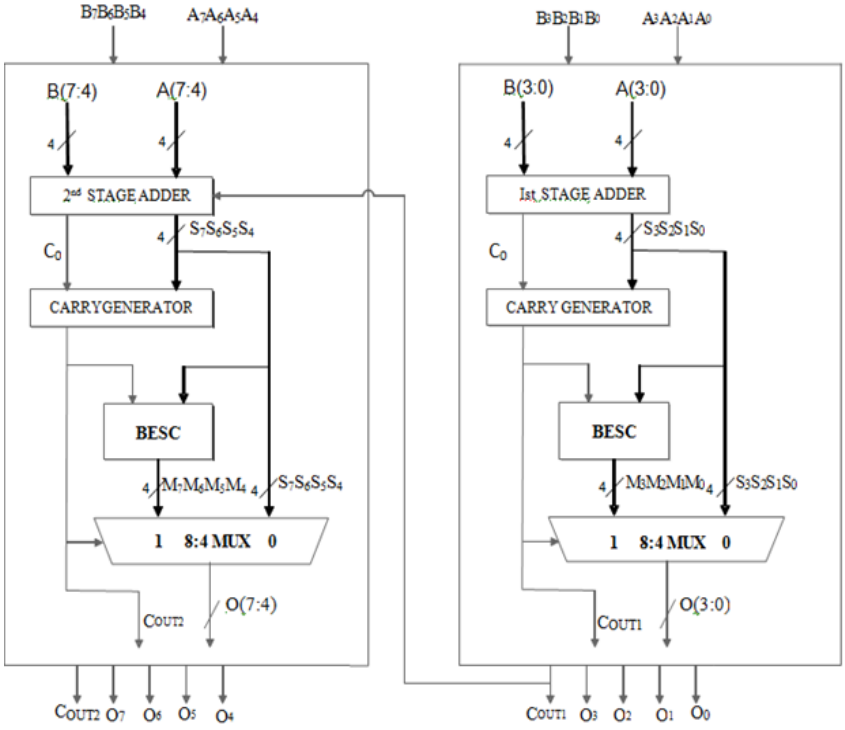

Figure 6. Block diagram of 2 digit adder implemented with proposed BESC-BCD adder

8. CONCLUSION

We have proposed a new adder for decimal addition using the concept of binary-excess six conversions for constant correction, to adjust outputs exceeding 9 to equivalent decimal. An extensive evaluation of area and worst-case delay of the proposed decimal adder with conventional design, fair better results which proves the novelty of the proposed methodology. Extensive comparison using synthesis results shows that the proposed BESC-BCD adder outperformed all other previous designs in terms of power dissipation and delay performances. The potential benefits of reduced delay and power dissipation of our proposed BESC-BCD adder can be realized in fair PDP saving performance. This suggests the suitability of our design for portable VLSI implementation. Moreover, the proposed methodology for decimal addition can be easily extended to multi digits.

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