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Verilog based efficient convolution encoder and viterbi decoder

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Article Info	ABSTRACT
	In thetoday'sdigital communication Systems,transmission of data with more reliability and efficiency is the most challenging issue for data communication through channels. In communication systems, error correction technique plays a vital role. In error correction techniques, The capacity of data can be enhanced by adding the redundant information for the source data while transmitting the data through channel. It mainly focuses on the awareness of convolution encoder and Viterbi decoder. For decoding convolution codes Viterbi algorithm is preferred.

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1. INTRODUCTION

In the today's digital Communication, data transmitting through the systems play a crucial role. As the growth of the technology is increasing every day, the usage of Viterbi is also increasing. This usage leads to major issues in digital communication systems and it results errors in data. It is necessary for the telecommunications to reduce the data corruption by finding suitable solutions to the errors occurred in Viterbi the communication process. One of such method is Viterbi Algorithm. It decodes the process by correcting it effectively. To decode the convolution codes, Viterbi algorithm is the most popular recognizable algorithm. This algorithm can be implemented with both software and hardware implementations. An efficient data should be required in digital systems to engage well organized communications. Data corruption is the important thing confronted by the digital communication systems. Error correcting codes are the best technique to decrease the data corruption. In fact every communication systems followed a technique of this kind as it has the better decoding efficiency, even for Viterbi algorithm very typical hardware is needed. The functioning obstructions will be eliminated when the decoding operation is in advance; it makes an improvement in designing Viterbi Algorithm. This algorithm is very effective in high-speed functions which help decoding of codes at a very faster rate. Convolution codes are used to gain a possible code sequence. Adaptive viterbi algorithm uses maximum likelihood decoding process. Hardware description language (HDL) was used to evaluate the desired outcome where it is one of the hardware descriptive languages. This language is employed in designing the electronic systems to semiconductor and electronic design industries as well as for assuring the analog and mixed signal circuit [1]. Convolutional encoder and Viterbi decoder as shown in Figure 1.
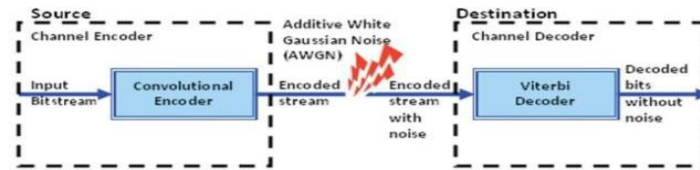
Figure 1. Convolutional encoder and Viterbi decoder

2. CONVOLUTIONAL ENCODER

Encoding or decoding is a process of modifying the message that can be understood easily. Decoding a message is the process of reconverting the meaning of that message from codeword to words which can be easily understood. It has both verbal and non-verbal means of communication. Nonverbal decoding doesn't make use of words, but other gestures or signs. One can easily decode the human gestures based on their emotions. For example, some gestures of humans when they are upset, anger, or stressed would be a use of excessive hand/arm movements, red in the face, crying, and even sometimes silence. Different massages can be interpreted differently from one person to the other person. Decoding is the process of understanding the information which someone already knows, depending on the information that is being given in the message being which is received. Even in case of broadcasting or communicating with one person, decoding is the process of obtaining, absorbing, understanding the information that was given throughout a verbal or non-verbal message. Convolution code is an error correcting code which generates parity bits through a sliding application of a Boolean polynomial function of a stream of data bits. This sliding application is composed of convoluting of the data bits in an encoder, which results in naming the process as convolution coding. The sliding nature of the convolution codes has a prominent attribute in trellis decoding using a time-invariant trellis. The Time invariant trellis decoding helps the convolution codes for having maximum likelihood besides the soft decision decoding with minimal complexity. Convolution codes are generally specified by the base code rate and the depth (or memory) of the encoder [n, k, K]. The b, K code rate is typically given as n/k. Here n is data rate of input bits and k is the symbol rate of output data stream. The depth is also referred as "constraint length" 'K'; here output is a function of the earlier K-1 inputs. The depth can also be given as number of memory elements 'v' in polynomial or the maximum possible states of the encoder (especially 2^v) [2]. Input Bit stream for Encoder is 1011 then output (y1y0) of encoder is 1110 0001.
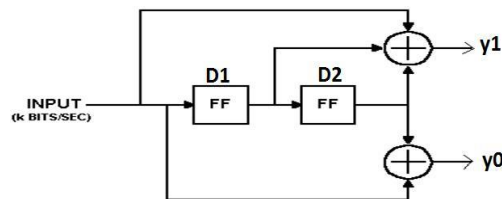

Figure 2. Convolutional encoder

3. VITERBI DECODING ALGORITHM

Decoder is a device which converts from code to plain text or any format that is useful for subsequent processes. Decoding is nothing but the reverse Process of encoding. Most computers use encoding for transfer of data, saving it then retrieving and using it. Data is transformed by an encoding mechanism like Binary Hexadecimal or American Standard Code for Information Interchange (ASCII) and then it is transmitted through a communication medium. For example, while sending an email, complete data including attachments will be encoded with Multipurpose Internet Mail Extensions (MIME) format. After receiving the data, decoder converts attachment contents to its original form. Viterbi algorithm can be used in such applications for decoding a bit stream which is encoded with convolution code. Many other algorithms are also available for decoding a convolution encoded stream of data. Shanon-Fano coding/algorithm is a method which can be used in such cases. Viterbi algorithm is the most resource-consuming coding technique, but it does the maximum likelihood decoding, which helps in perfect reconstruction of data. Viterbi decoder is most prominent for decoding convolution codes with constraint lengths k<=10, but in practice up to k=15 can be used. Decoding a message is nothing but extracting the meaning of that message such that it can be understood [1].

4.   PERFORMANCE OF VITERBI DECODER

The main stages in the Viterbi decoding process are having the following stages;
a. Branch Metric Unit, BMU
b. Path Metric Unit, PMU
c. Trace back Unit, TU

The Figure 3 Block diagram consists of the proposed Viterbi decoder. This section discusses about different blocks of the Viterbi decoder. Initially Analog signals are quantized and then they are converted into digital form at the quantization block. Synchronization block detects the frame boundaries of code words and symbol boundaries. At the end Viterbi decoder receives number of parallel successive code symbols, in which the boundaries of the symbols and the frames will be identified [3]. Figure 4 shows convolution code trellis tree and Viterbi algorithm.
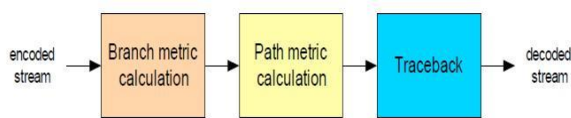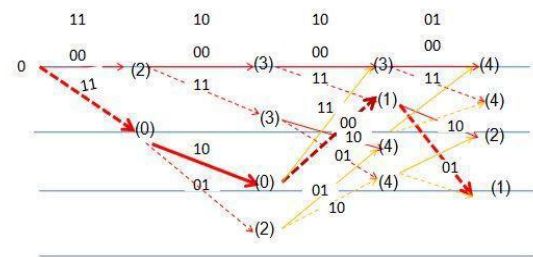

Figure 3. Block diagram of a Viterbi decoder

Error Encoded Bits: 11 10 10 01
Original Encoded Bits: 11 10 00 01
Input: 1011

Figure 4. Convolution code trellis tree and Viterbi algorithm

4.1. Branch Metric Unit

The Branch metric unit is used to generate the branch metrics, by calculating the hamming distances of input code word from 11, 10, 00 and 01. The Branch Metric unit is also used to measure the branch metric for the corresponding all trellis branches from the input codeword. At last we will choose certain difference as a measure for branch metric. These branch metrics are considered to be equal the weights of the branches [4].

4.2. Path Metric Unit

Memory is needed to store the survivor Path Matrix Unit (PMU). The word length of memory depends on the number of the ACS sub-blocks which are used in the design or the number of states in the decoder or k^2. Here k is the constraint length, (5 in this case). The range of memory depends on the trellis length [5]. In general, the memory range should be kept twice the trellis length or two blocks of memory equal to trellis length. In this proposed algorithm k=5 and trellis length equal to 32 is assume. Hence, the block of memory used will be 64x16. For this reason a dual port memory is used. However in this dual port memory, One of the port is for writing the data and the second port is for reading the data, which is will be convenient for writing and reading the data simultaneously from various memory addresses. Memory must write the data in parallel while reading the data is asynchronous in order to maintain the lower latency or for better management of synchronous behavior in the entire system [6].

4.3.Traceback Unit

Results of these are written to the memory of traceback unit. It Traces back from the end of any survivor paths to the beginning [2].

5.   SIMULATION AND SYNTHESIS RESULTS

5.1. Synthesis Report

Synthesis is the process of converting a RTL model of circuits into a gate level enlists which are described in Verilog code. Because of this there will be an increase in the design size and complexity as well. Because of this design complexity there is a scope to improve the design using synthesis and simulation

tools. These factors make Hardware Description Languages (HDLs) the preferred design languages for most of the integrated circuit designers. The two major Hardware Description Languages for synthesis and simulation are Verilog and VHDL.
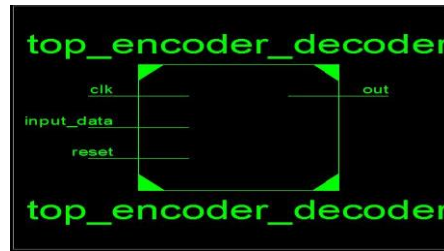

Figure 5. Encoder decoder (RTL1)

Figure5 is the simulation representation of convolution encoder and Viterbi decoder at the circuit level. The entire code developed for this work on Xilinx ISE and can be realized on the hardware. Viterbi algorithm implementation for encoder and decoder can be explained as a step by step process by analyzing the results of implemented system. Figure 5 and 6 shows the RTL schematic of convolution encoder and Viterbi decoder which consists of different modules like branch metric unit, encoder unit, path metric unit, survival path tracing unit and path metric store unit. Device utilization of viterbi decoder as shown in Table 1 and Table 2.
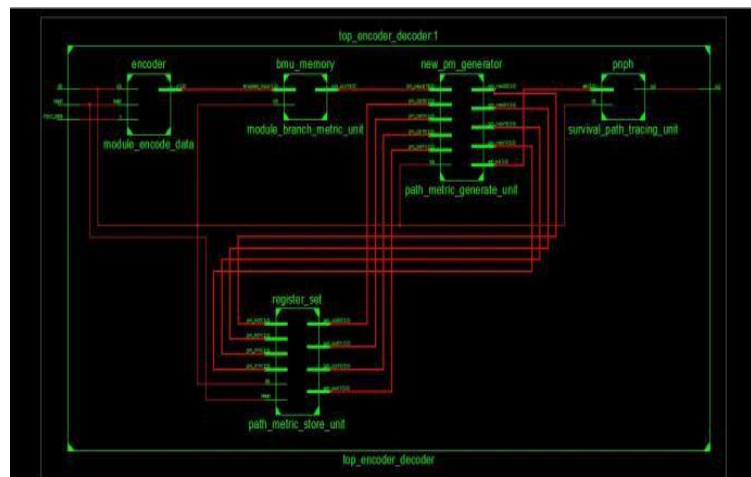

Figure 6. Encoder_decoder(RTL2)

Table 1. Device Utilization of Viterbi Decoder

Device Utilization Summary (estimed values)		[-]
Logic Utilization	Used	Aviable	Utilization
Number of Slices	84	3584	2%
Number of Slice Flip Flops	78	7168	1%
Number of 4 input LUTs	124	7168	1%
Number of bonded IOBs	4	141	2%

Table 2. Device Utilization of Viterbi Decoder

Device Utilization Summary (estimed values)		[-]
Logic Utilization	Used	Aviable	Utilization
Number of Slices	287	5472	5%
Number of Slice Flip Flops	217	10944	1%
Number of 4 input LUTs	558	10944	5%
Number of bonded IOBs	12	240	5%
Number FIFO 15 RAMB 16s	2	36	5%
Number of GOLKs	1	32	3%

5.2. SimulationWaveforms of Convolution Encoder

The Simulation Waveform for a Convolution Encoder with an input 1011 is shown in Figure 7. Here the data Rate ½ and K=9 and it Encodes the data and the output is given as 11 10 00 01. The simulation results for the implemented system can be observed by using Modelsim simulator or Xilinx ISE simulator. The speed and resource utilization were produced and synthesized using Xilinx Synthesis Tool (XST).
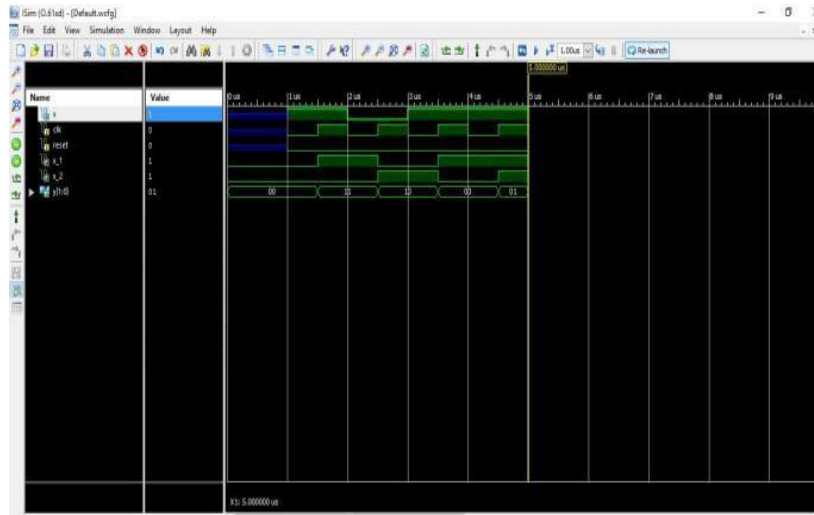

Figure 7. Xilinx simulation results for convolution encoder

5.3. SimulationWaveforms of Viterbi Decoder

The Simulation results of the Viterbi decoder is shown in Figure 8. Viterbi decoder decoded the encoded bit stream (11 10 00 01) and gives the output (1011) in the second half of the cycle.
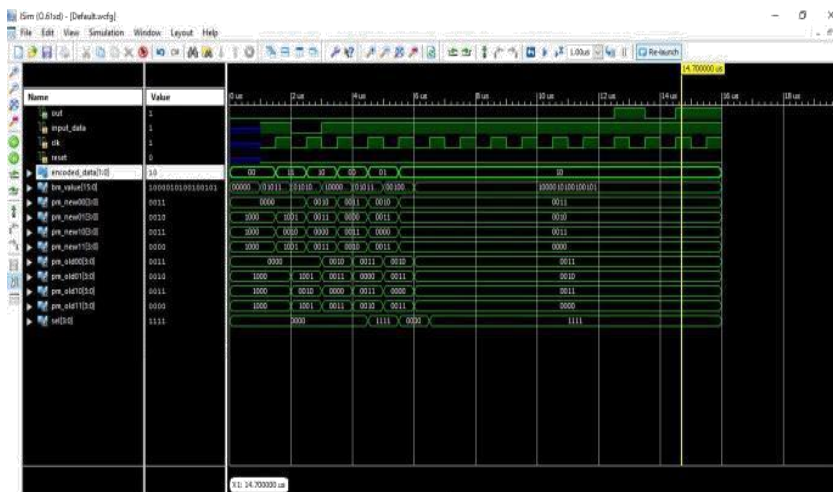

Figure 8. Xilinx simulation results for convolution encoder and Viterbi decoder

6. CONCLUSION

Now a day the Viterbi algorithm becomes more interesting and challenging for the researchers in the field of communications. It also has a broader range of applications in the digital communications field in this modern era of communications. This work helps in making use of efficient coding and decoding techniques wsith help of Viterbi algorithm. Also Viterbi algorithm can be easily understood and can be implemented easily. This work presents the implementation of the Viterbi algorithm using Verilog coding. Unlike other algorithms the proposed Viterbi algorithm has many advantages such as power consumption and the major advantage is error correction using Verilog.

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