High speed graphene-silicon electro-absorption modulators for the O-band and C-band

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In the past few years, graphene has drawn interest for applications in optoelectronic devices. Due to its extraordinary properties, i.e. wide optical bandwidth, tunable absorption, high carrier mobility, and CMOS compatibility, it is a candidate to improve current state-of-the-art high speed optoelectronic devices, such as modulators. In this work, we present a model that describes the DC and high-speed behaviour of single-layer graphene-oxide-silicon electro-absorption modulators (EAM). We compare the theoretical analysis with experimental results, and we find that p-doped graphene combined with p-doped silicon enables high speed operation at low DC bias. Using this configuration, we demonstrate 75 μ m-long TM EAMs operating in the O-band and in the C-band. The O-band EAM exhibits 3.1dB extinction ratio and 16.0GHz 3dB-bandwidth at 1V DC bias. With the C-band EAM we achieve 6.5dB extinction ratio and 14.2GHz 3dB-bandwidth at 0V DC bias. Open eye diagrams up to 50Gbit/s are measured using 2.5V_{pp} and -0.5V DC bias at a wavelength of 1560nm.

1. Introduction

Electro-optical modulators are key components in optical communication systems. Important requirements for modulators are low insertion loss (IL), high extinction ratio (ER), high operation speed and low energy consumption.

In the past few years, graphene, a two-dimensional network of sp²-hybridised carbon atoms, has attracted a lot of interest due to its unique optoelectronic properties [1–3]. Graphene is a zero bandgap material, with an optical bandwidth from visible to infrared (up to 180 nm in the C-band) [4, 5]. It absorbs 2.3% of the perpendicularly incident light, which can be enhanced further by integrating graphene on a waveguide to increase the interaction length between light and graphene. Graphene's absorption can be easily tuned through capacitive charging by applying an electric field [2], and has therefore the potential to enable active optoelectronic functionality onto passive optical waveguides, such as Si and low-loss SiN

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waveguides [6]. In addition, graphene is CMOS compatible and can be integrated into CMOS processes in the back end of line (BEOL). These properties, together with the high carrier mobility (e.g. more than $300,000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ with hBN encapsulation [7]), make graphene a candidate for applications in high-speed optoelectronic devices, such as photodetectors [8–13] and modulators [4, 5, 13–21].

High-speed graphene modulators have been reported in literature in single-layer graphene (SLG) [4, 5, 15, 19] or double-layer graphene (DLG) [13, 14, 20, 21] configuration on top of the waveguide. DLG modulators are based on a graphene-oxide-graphene capacitor, while SLG modulators are based on a graphene-oxide-silicon capacitor. Due to the presence of two graphene layers, DLG modulators offer potential for higher extinction ratio than SLG modulators, but they suffer from higher insertion loss. In addition, SLG modulators have a simpler fabrication process compared to DLG modulators, requiring the transfer of only one graphene layer. A DLG ring modulator with 30 GHz 3 dB frequency response and open eye diagrams at 22 Gbit/s was demonstrated by reducing the capacitance of the device using a 65 nm-thick Al₂O₃ as spacer between the two graphene layers [14]. However, employing a thick Al_2O_3 comes at the expense of the high drive voltage (7.5 V_{pp}) and high DC bias (-30 V) necessary to operate the device. In addition, the device has limited optical bandwidth, due to the resonant nature of the ring modulator. A more recent work reports a 120 µm-long DLG electro-absorption modulator (EAM), built on top of a silicon waveguide with a 20 nm-thick SiN spacer between the two graphene layers, exhibiting 20 dB IL and 3 dB ER for 9 V_{pp} [21]. The device shows 29 GHz 3 dB frequency response and open eye diagrams at 50 Gbit/s using $3.5~V_{pp}$, at a high DC bias of 8 V. Among SLG modulators, in [5] a broadband SLG EAM with a n-doped Si waveguide was demonstrated, achieving a 3 dB frequency response of 5.9 GHz and open eye diagrams at 10 Gbit/s using 2.5 V_{pp} at 1.75 V DC bias in the wavelength range between 1530 nm and 1565 nm. In [15], a 50 µm-long SLG EAM with a p-doped Si waveguide was demonstrated, exhibiting an improved 3 dB frequency response of 16 GHz at 0 V DC bias and open eye diagrams up to 25 Gbit/s using 2.5 V_{pp} at 2 V DC bias.

In this paper, we present a theoretical model that describes the DC and high speed performance of SLG EAMs. The model is used to identify the optimal combination of graphene doping and silicon waveguide doping, in order to optimise the DC performance and the total device RC for high-speed operation around 0 V DC bias. We compare experimental results from three samples, fabricated by transferring graphene on waveguides with different type and level of silicon doping, to corroborate the theoretical analysis. After transfer, graphene on waveguides exhibits p-doping behaviour. We employ a thin SiO₂ layer with a thickness of 5

nm as spacer between graphene and Si, in order to achieve a low operating bias. The best static and high speed performance is obtained on TM SLG EAMs fabricated with p-doped silicon waveguides. O-band and C-band operation with more than 14 GHz 3 dB frequency response is demonstrated across a total wavelength range of 140 nm. On a 75 μ m-long O-band TM SLG EAM, we achieve 4.0 dB insertion loss, 3.1 dB extinction ratio using 8 V_{pp} and 16.0 GHz 3 dB frequency response at 1 V DC bias at 1300 nm wavelength. In the C-band, we demonstrate a 75 μ m-long broadband SLG EAM with 4.2 dB insertion loss, 6.5 dB extinction ratio using 8 V_{pp} and 14.2 GHz 3 dB frequency response at 0 V DC bias and 1560 nm wavelength. Open eye diagrams are obtained up to 50 Gbit/s at 1560 nm wavelength for the first time on a SLG EAM, using 2.5 V_{pp} and -0.5 V DC bias, thus showing potential for graphene integration in high-speed photonics applications.

2. Device design and fabrication

The single-layer graphene-silicon electro-absorption modulator is based on a 220 nm-thick silicon (Si) waveguide, fabricated on a silicon-on-insulator (SOI) wafer with 2 μ m buried oxide in imec's 200 mm Si photonics platform (Fig. 1(a)) [22]. The waveguide is partially etched on one side, creating a rib structure that allows to contact the Si waveguide through the 70 nm-thick slab layer. The waveguide is embedded in SiO₂ to ensure a planar surface for the

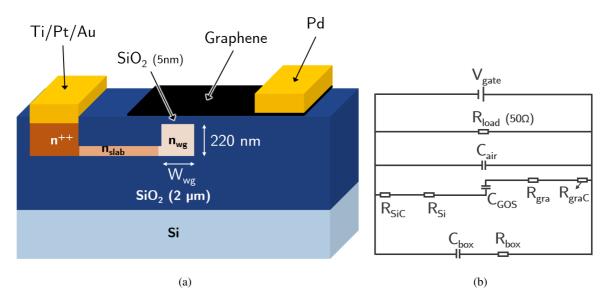


Fig. 1. (a) Schematic cross section of the SLG EAM. The three doped silicon regions are either p- or n-doped: waveguide (n_{wg}/p_{wg}) , slab (n_{slab}/p_{slab}) and contact (n^{++}/p^{++}) . The graphene, oxide and silicon layers form a GOS capacitor. (b) Equivalent electrical circuit of the SLG EAM. The RC constant limits the 3dB frequency response.

subsequent graphene transfer. Three separate doping levels (n^{++} or p^{++} for the contact region, n_{slab} or p_{slab} for the slab region, n_{wg} or p_{wg} for the waveguide region) are used to minimise the Si contact and sheet resistance, without significantly increasing the waveguide loss. After Si waveguide patterning, a chemical-mechanical planarisation (CMP) step is performed to planarise the waveguides. Through thermal oxide growth the desired SiO₂ thickness of 5 nm is obtained on top of the Si waveguide. After wafer dicing, subsequent processing is performed at coupon level in a cleanroom lab environment. Graphene grown by chemical vapour deposition (CVD) is transferred on top of the Si waveguides. Both growth and transfer processes were carried out by Graphenea (www.graphenea.com). Subsequently, graphene is patterned to cover part of the Si waveguide and to define the length of the EAM. Contacts are made to graphene (50 nm Pd) and to the doped Si (10 nm Ti/20 nm Pt/50 nm Au) based on a standard lift-off process. These contact metals were selected to minimise the contact resistance to graphene and to Si respectively [23]. The contacts are placed 2 µm away from the waveguide and therefore have no impact on transmission loss. The graphene and silicon contacts are used to apply an electric field across the device, which modulates the Fermi level in graphene.

3. Device modeling

3.1 Static electro-optical behaviour of the SLG EAM

The static electro-optical behaviour of the SLG EAM is defined by the relation between the absorption and graphene's Fermi level μ . Graphene's absorption is derived from the 2D complex optical conductivity σ_g (ω , Γ , T, μ), calculated from the Kubo formula [2]. This formula takes into account interband and intraband transitions, and it depends on the angular frequency ω , the charged particle scattering rate $\hbar\Gamma$, the temperature T, and most importantly graphene's Fermi level μ . The latter can be shifted by sweeping the voltage V_g across the graphene-oxide-silicon (GOS) capacitor [2], according to

$$V_g = \frac{q (n_0 + n_s)}{C_{GOS}} = \frac{q}{\pi (\hbar v_F)^2} \frac{\mu^2}{C_{GOS}}$$
 (1)

where q is the elementary charge, \hbar is the reduced Planck constant, v_F is the Fermi velocity of carriers in graphene and C_{GOS} is the capacitance of the GOS capacitor. The Fermi level μ is the sum of two contributions:

$$\mu = \mu_0 + \Delta \mu \tag{2}$$

 μ_0 is the initial Fermi level position due to the fixed number of charges n_0 (graphene's intrinsic doping), and $\Delta\mu$ is the Fermi level shift caused by the number of charges n_s accumulated on

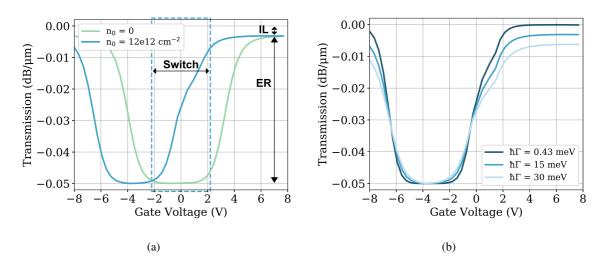


Fig. 2. Simulated transmission as a function of gate voltage at $\lambda = 1560$ nm of a TE SLG EAM with 5 nm oxide, 500 nm-wide waveguide and $p_{wg} = 1.0e18$ cm⁻³: (a) for neutral ($n_0 = 0$ cm⁻²) and p-doped ($n_0 = 12e12$ cm⁻²) graphene, with graphene's scattering rate $\hbar\Gamma = 15$ meV; (b) for p-doped graphene ($n_0 = 12e12$ cm⁻²) and scattering rates $\hbar\Gamma = 0.43$, 15, 30 meV. When graphene is p-doped the switch between on- and off-state occurs between -2 V and 2 V. Higher scattering rate results in lower ER and higher IL.

graphene when we apply V_g across the capacitor.

The static electro-optical behaviour of the SLG EAM as a function of applied voltage is mainly affected by two parameters: graphene's intrinsic doping (n_0) and the scattering rate $\hbar\Gamma$. The intrinsic doping n_0 affects the position of minimum transmission as a function of applied voltage. Fig. 2(a) shows the simulation, performed using Lumerical MODE Solutions, of the optical transmission as a function of gate voltage for a TE SLG EAM with 5 nm-thick SiO_2 and 500 nm-wide waveguide operating at 1560 nm, for neutral ($n_0 = 0 \text{ cm}^{-2}$) and p-doped ($n_0 = 12e12 \text{ cm}^{-2}$) graphene, for scattering rate $\hbar\Gamma = 15 \text{ meV}$. For neutral graphene, the minimum is at 0 V, therefore switching between high transmission (on-state) and low transmission (off-state) requires ~ 3.5 V or ~ -4 V DC bias. For p-doped graphene, the minimum transmission point is shifted to negative bias. In this case, switching occurs between -2 V and 2 V, which is compatible with current CMOS technology. The scattering rate $\hbar\Gamma$, which is inversely proportional to the mobility μ [24], affects the extinction ratio of the modulator. As shown in Fig. 2(b), a lower scattering rate, implying higher graphene quality, results in higher extinction ratio for a given V_{pp} because graphene can reach full transparency. For example, a 75 μ m-long SLG EAM would show 0.5 dB higher extinction ratio for $\hbar\Gamma$ = 0.43 eV compared to $\hbar\Gamma = 30$ eV. In real applications, graphene's scattering rate is often more than 10 meV [24], resulting in a reduced extinction ratio and increased insertion loss.

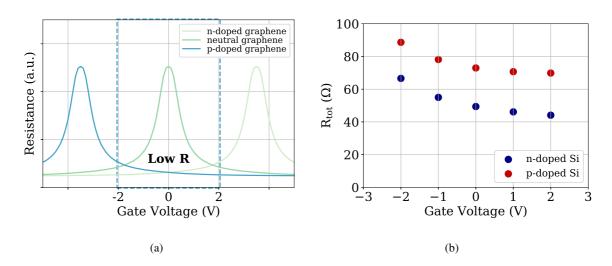


Fig. 3. (a) Graphene resistance as a function of gate voltage for n-doped, neutral and p-doped graphene. For p-doped graphene there is a low resistance region for voltage values around or greater than 0 V. The plotted graph is a visualisation modified from an experimental curve. (b) Simulated total resistance as a function of gate voltage of a 75 μ m-long SLG EAM with p-doped graphene ($n_0 = 12e12 \text{ cm}^{-2}$), for p-doped ($p_{wg} = 1.9e18 \text{ cm}^{-3}$, $p_{slab} = 3.2e19 \text{ cm}^{-3}$) and n-doped silicon ($n_{wg} = 2.3e18 \text{ cm}^{-3}$, $n_{slab} = 2.7e19 \text{ cm}^{-3}$). P-doped silicon exhibits higher sheet resistance than n-doped silicon. The voltage-dependent behaviour is caused by R_{graC} and R_{gra} .

3.2 RC limited high-speed behaviour of the SLG EAM

The 3 dB frequency response of a SLG EAM is limited by the RC constant of the device, and can be explained using the equivalent electrical circuit in Fig.1(b).

Device resistance The device total resistance (R_{tot}) is the sum of graphene's contact and sheet resistance (R_{graC} and R_{gra}) and the Si contact and sheet resistance (R_{SiC} and R_{Si}). Graphene's resistance is affected by the scattering rate $\hbar\Gamma$, which is proportional to the impurity density n^* , caused by local potential fluctuations and electron/hole puddles on the graphene layer [25, 26]. Higher scattering rate corresponds to lower mobility and therefore higher resistance. When the mobility is higher (lower $\hbar\Gamma$ and n^*), the peak in graphene's resistance corresponding to the neutrality point is higher. As a consequence, the resistance experiences a more abrupt change when the gate voltage is increased or decreased to move away from the neutrality point [24]. The values of R_{graC} and R_{gra} at a fixed DC voltage bias are also affected by graphene's intrinsic doping n_0 . For $n_0 = 0$, graphene's resistance reaches its peak value at 0 V voltage bias, and decreases for increasing (or decreasing) voltage bias. When applying V_{gate} as indicated in Fig. 1(a), p-doped (n-doped) graphene shows a peak value at negative (positive) voltage bias due to the shift of graphene's charge neutrality point (Fig. 3(a)). The resistance then decreases as the voltage increases (decreases). In case of p-doped

graphene, there is therefore a low resistance region for voltage values around or greater than 0 V. The Si contribution to R_{tot} depends on the doping level of the three Si regions: contact, slab and waveguide areas. To properly estimate how the silicon doping impacts the resistance, we perform a process simulation using Sentaurus TCAD, which accurately emulates the real processing performed in the fab. Afterwards we extract the values of silicon resistance (R_{Si} and R_{SiC}) for the three doped regions together (contact, slab and waveguide) by performing a transient device simulation at different voltage values. Fig. 3(b) shows the values of R_{tot} as a function of gate voltage for a 75 μ m-long device with p-doped graphene (mobility μ_c = 800 cm²/Vs; R_{graC} = 880 Ω μ m and R_{gra} = 340 Ω / \square at 0 V) and a waveguide width of 500 nm, for p-doped (p_{wg} = 1.9e18 cm⁻³, p_{slab} = 3.2e19 cm⁻³) and n-doped (n_{wg} = 2.3e18 cm⁻³, n_{slab} = 2.7e19 cm⁻³) Si. P-doped silicon exhibits higher sheet resistance than n-doped silicon, due to the lower mobility of holes compared to electrons. The variation of R_{tot} with gate voltage is influenced by the voltage-dependent behaviour of $R_{graC}(V)$ and $R_{gra}(V)$ only. GOS capacitance The total GOS capacitance C_{GOS} is given by the series of graphene's quantum capacitance C_q , the oxide capacitance C_{ox} and the Si depletion capacitance C_{Si} :

$$\frac{1}{C_{GOS}} = \frac{1}{C_q} + \frac{1}{C_{ox}} + \frac{1}{C_{Si}} \tag{3}$$

Graphene's quantum capacitance is given by the following equation [27, 28]:

$$C_q = \frac{2q^2}{\hbar v_F \sqrt{\pi}} \sqrt{|n_s + n_0|} = \frac{2q^2}{\hbar^2 v_F^2 \pi} |\mu| \tag{4}$$

where μ is graphene's Fermi level as defined in Eq. 2. The quantum capacitance is characterised by a minimum when $\mu = 0$ ($\Delta \mu = -\mu_0$, according to Eq. 2) and it increases linearly for $|\mu| > 0$ (Fig. 4(a)). For intrinsic (undoped) graphene, the Fermi level is at the Dirac point, $\mu_0 = 0$ and therefore $C_q = 0$ for $\Delta \mu = 0$ (Fig. 4(b)). In p-doped (n-doped) graphene, $\mu_0 < 0$ ($\mu_0 > 0$) and, as a consequence, the minimum of C_q is located at $\Delta \mu = -\mu_0$ (Fig. 4(b)). When graphene is not pristine, the additional impurity carrier density n^* should be included in the calculation, The quantum capacitance becomes [26]

$$C_q = \frac{2q^2}{\hbar v_F \sqrt{\pi}} \sqrt{|n_s + n_0| + |n^*|}$$
 (5)

If we compare C_q with C_{ox} calculated for 5 nm of SiO₂ (Fig. 4), we see that the latter is significantly smaller for each value of μ away from the neutrality point. When n*>0, the minimum of the quantum capacitance increases and C_q becomes significantly higher than C_{ox} for any value of chemical potential, as shown by the dotted lines in Fig. 4. For this reason, when placed in series with C_{ox} , the contribution of C_q is minor.

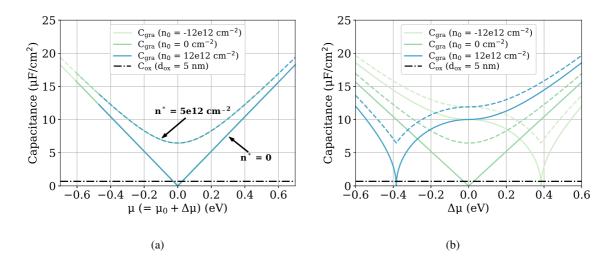


Fig. 4. (a) Calculated graphene quantum capacitance as a function of graphene's Fermi level μ , for n-doped $(n_0 = -12e12 \text{ cm}^{-2})$, neutral $(n_0 = 0 \text{ cm}^{-2})$ and p-doped $(n_0 = 12e12 \text{ cm}^{-2})$ graphene, compared with the capacitance of 5 nm-thick SiO₂. The full lines are calculated for $n^* = 0$ and the dotted lines for $n^* = 5e12 \text{ cm}^{-2}$. (b) Same as (a), but the capacitance is plotted as a function of Fermi level shift $(\Delta \mu = \mu - \mu_0)$.

The analytical model used to calculate C_{GOS} as a function of applied voltage V_g is based on the MOS capacitor model [29], with the difference that for the GOS capacitor graphene's quantum capacitance C_q is included in the calculation. The voltage is applied on the graphene contact, while the silicon contact is grounded. In accumulation, when $V_g < V_{FB} < 0$ for p-doped Si and $V_g > V_{FB} > 0$ for n-doped Si, with V_{FB} being the commonly known flatband voltage of a MOS capacitor [29], the silicon layer is not yet depleted, so the quantities that play a role are C_q and C_{ox} . To calculate the amount of charges n_s accumulated on the graphene layer for each $V_g < V_{FB}$, we need to solve the following system

$$\begin{cases} V_g - V_{FB} = Q_{acc} \left(\frac{1}{C_{ox}} + \frac{1}{C_q} \right) = n_s \left(\frac{1}{C_{ox}} + \frac{1}{C_q} \right) \\ C_q = \frac{2q^2}{\hbar v_F \sqrt{\pi}} \sqrt{|n_s + n_0| + |n^*|} \end{cases}$$
 (Eq. 5)

where Q_{acc} is the accumulation charge. The resulting equation for n_s is

$$\frac{q}{C_{ox}}n_s + \left(\frac{\hbar v_F^2 \sqrt{\pi}}{2q}\right) \frac{n_s}{\sqrt{|n_s + n_0| + |n^*|}} + \left(V_{FB} - V_g\right) = 0 \tag{7}$$

Once the value of n_s for each V_g is known, we can calculate C_q through Eq. 4 and therefore the total accumulation capacitance $C_{GOS,acc} = \left(\frac{1}{C_{ox}} + \frac{1}{C_q}\right)^{-1}$. Graphene's natural doping n_0 is considered in the calculation as an initial condition and it will automatically affect the position of graphene's charge neutrality point in the final result. In fact, n_s and n_0 in Eq. 4 are summed up before applying the absolute value, which is necessary to make a distinction

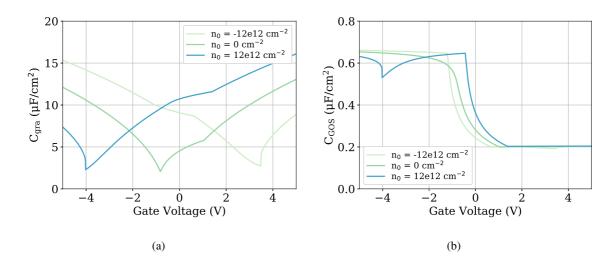


Fig. 5. (a) Graphene quantum capacitance as a function of gate voltage for n-doped ($n_0 = -12e12 \, \mathrm{cm}^{-2}$), neutral ($n_0 = 0 \, \mathrm{cm}^{-2}$) and p-doped ($n_0 = 12e12 \, \mathrm{cm}^{-2}$) graphene ($n^* = 5e11 \, \mathrm{cm}^{-2}$). The minimum of C_q shifts depending on the graphene doping. (b) GOS capacitance as a function of gate voltage with fixed p-type silicon waveguide doping ($p_{wg} = 1.0e18 \, \mathrm{cm}^{-3}$), for n-doped ($n_0 = -12e12 \, \mathrm{cm}^{-2}$), neutral ($n_0 = 0 \, \mathrm{cm}^{-2}$) and p-doped ($n_0 = 12e12 \, \mathrm{cm}^{-2}$) graphene ($n^* = 5e11 \, \mathrm{cm}^{-2}$). C_q affects C_{GOS} only in proximity of its minimum.

between n-doped ($n_0 < 0$) and p-doped graphene ($n_0 > 0$). In inversion ($V_g > V_T > 0$ for p-doped Si and $V_g < V_T < 0$ for n-doped Si, where V_T is threshold voltage [29]) the silicon layer has reached maximum depletion and the quantities to be considered are C_q , C_{ox} and $C_{Si,max}$. Eq. 7 becomes

$$\frac{q}{C_{ox}}n_s + \left(\frac{\hbar v_F^2 \sqrt{\pi}}{2q}\right) \frac{n_s}{\sqrt{|n_s + n_0| + |n^*|}} + \left(V_g - V_{FB} - 2\phi_F\right) = 0$$
 (8)

where the bulk potential ϕ_F takes into account the voltage drop due to $C_{Si,max}$. The total inversion capacitance can be calculated as $C_{GOS,inv} = \left(\frac{1}{C_{ox}} + \frac{1}{C_q} + \frac{W_{dep,max}}{\varepsilon_0 \varepsilon_{Si}}\right)^{-1}$, where $W_{dep,max}$ is the maximum width of the depletion region in the silicon layer.

To calculate the total capacitance $C_{GOS,dep}$ in depletion ($V_{FB} < V_g < V_T$ for p-doped Si and $V_{FB} > V_g > V_T$ for n-doped Si), a different approach is necessary. The width of the depletion region in silicon W_{dep} has to be calculated for values of the surface potential ϕ_s ranging from 0 to $2\phi_F$. From W_{dep} , the depletion charge Q_{dep} and therefore the number of charges on graphene n_s can be calculated. The total GOS capacitance in depletion is given by $C_{GOS,dep} = \left(\frac{1}{C_{ox}} + \frac{1}{C_q} + \frac{W_{dep}}{\varepsilon_0 \varepsilon_{Si}}\right)^{-1}$. All the quantities that have been calculated as a function of ϕ_s can then be expressed as a function of the applied voltage through $V_g = V_{FB} + \phi_s - Q_{dep} \left(\frac{1}{C_{ox}} + \frac{1}{C_q}\right)$.

Throughout the calculation of C_{GOS} , the values of $V_g(n_s)$, and therefore $V_g(\mu)$, are ex-

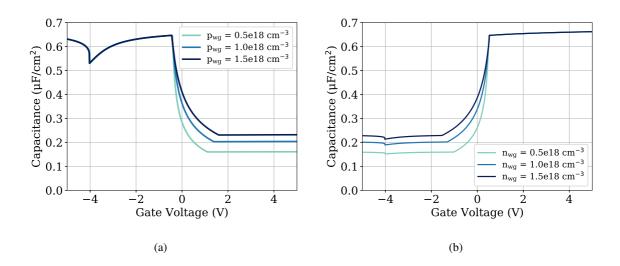


Fig. 6. Calculated GOS capacitance with p-doped graphene ($n_0 = 12e12 \text{ cm}^{-2}$), for varying p-type (a) and n-type (b) Si waveguide doping levels. The capacitance in depletion decreases for lower doping level.

tracted step by step, and are used to obtain graphene's absorption (and therefore transmission) as a function of the applied voltage V_g through Eq. 1, as shown in Fig. 2.

The results of the calculation of C_{GOS} for a GOS capacitor with p-doped silicon (p_{wg} = $1.0e18 \text{ cm}^{-3}$) for n-doped ($n_0 = -12e12 \text{ cm}^{-2}$), neutral ($n_0 = 0 \text{ cm}^{-2}$) and p-doped ($n_0 = -12e12 \text{ cm}^{-2}$) 12e12 cm⁻²) graphene is shown in Fig. 5(b). As expected, graphene's quantum capacitance affects C_{GOS} only where C_q reaches its minimum (Fig. 5(a)). This effect is clearly visible only when the GOS capacitor is in accumulation mode, and therefore C_{GOS} is higher. As a consequence, reducing C_q by reducing the impurity density n^* would only have a small effect on C_{GOS} as a whole. In order to decrease C_{ox} , we could use an oxide with a lower permittivity or increase the oxide thickness. However, both solutions would increase the field necessary to accumulate charges on the capacitor plates in the whole range necessary to operate the device. In other words, the lower capacitance would allow to obtain a higher 3 dB frequency response, but the extinction ratio for the same voltage range would be significantly reduced. The device capacitance can therefore be optimised by focusing on how C_{Si} changes when varying the type and level of doping, and on how this affects C_{GOS} . Fig. 6 shows the calculation of C_{GOS} performed for p-doped graphene ($n_0 = 12e12 \text{ cm}^{-2}$) for different levels of p-type and n-type silicon doping. The capacitance in accumulation is not affected by the variation in silicon doping level. A reduction in capacitance is achieved in depletion for lower silicon doping, as expected due to the lower silicon depletion capacitance C_{Si} when the silicon doping is decreased. Due to this characteristic MOS behaviour, it is preferable to operate the device in depletion in order to obtain lower capacitance.

Table I. Summary of the level and type of Si doping used for the theoretical calculation shown in Fig. 7.

Doping type	Slab doping (cm ⁻³)	Wg doping (cm ⁻³)	
n-doped	2.7e19	2.3e18	
p-doped	3.2e19	1.9e18	

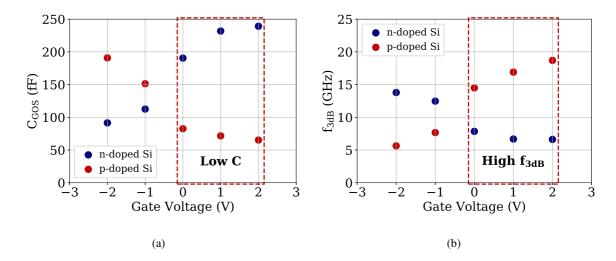


Fig. 7. Calculated GOS capacitance (a) and simulated 3 dB frequency response (b) as a function of gate voltage of a 75 μ m-long SLG EAM, for p-doped ($p_{wg} = 1.9e18 \text{ cm}^{-3}$, $p_{slab} = 3.2e19 \text{ cm}^{-3}$) and n-doped silicon ($n_{wg} = 2.3e18 \text{ cm}^{-3}$, $n_{slab} = 2.7e19 \text{ cm}^{-3}$). P-doped Si allows to operate the SLG EAM in depletion in the operating region of interest (0-2 V), thus achieving more than double f_{3dB} compared to n-doped Si.

3.3 Device optimisation

To optimise the SLG EAM for high-speed operation, the 3 dB frequency response of the device has to be maximised. This figure of merit is limited by the device RC constant, therefore the total resistance and capacitance of the device have to be minimised in the desired operating region in order to obtain the lowest possible RC. In fabricated devices, graphene is most often p-doped, due to dangling oxygen bonds in the SiO₂ below and also due to environmental and polymer contamination during processing [30, 31]. In terms of static electro-optical performance, as seen in Section 3.1, this means that the switching between on and off states takes place in the region between -2 V and 2 V voltage bias. This region corresponds to the low resistance region in case of p-doped graphene, as shown in Fig. 3. In order to have low capacitance in the same voltage range, p-doped Si is preferable because it allows to operate the device in depletion for voltage bias higher than 0 V. As a result, when p-doped graphene is combined with p-doped silicon, the total RC is reduced in the region between 0 V and 2 V. Likewise, in case of n-doped graphene, the situation would be reversed and the best choice

would be a device with n-doped silicon operating at low reverse bias. This is better visualised in the example in Fig. 7. Fig. 7(a) shows the values of C_{GOS} as a function of gate voltage for a 75 μ m-long device with p-doped graphene ($n_0 = 12e12 \text{ cm}^{-2}$) and a waveguide width of 500 nm, for p-doped and n-doped Si (doping values in Table I). Using these values of C_{GOS} and values of R_{tot} from Fig. 3(b), the 3 dB frequency response is then extracted by simulating the electrical equivalent circuit in Fig. 1(b). Even though p-doped silicon exhibits higher sheet resistance than n-doped silicon, the considerably lower GOS capacitance of the EAM with p-doped silicon in the 0 V - 2 V region allows to achieve a two-fold improvement in 3 dB frequency response at 0 V (Fig. 7(b)).

Patterning graphene under the contact area, e.g. with holes, to increase the edge contact perimeter between graphene and the metal can lead to a significant reduction in graphene's contact resistance [32]. Improved values of graphene contact and sheet resistance ($R_{graC} = 100 \, \Omega$ µm and $R_{gra} = 60 \, \Omega/\square$) would allow to achieve a 3 dB frequency response of 17 GHz (18% improvement) at 0 V DC bias for a 75 µm-long EAM and 25 GHz for a 25 µm-long EAM. With reduced doping in the waveguide ($p_{wg} = 4e17 \, \mathrm{cm}^{-3}$) this values could be further improved up to 23 GHz and 31 GHz for $L_{device} = 75 \, \mu \mathrm{m}$ and $L_{device} = 25 \, \mu \mathrm{m}$ respectively.

4. Experimental results and discussion

In the first part of this experimental section, we compare the performance of four C-band SLG EAMs on TE waveguides between three samples, fabricated with different type and level of doping in Si. In Section 4.2, we select the sample with p-type Si doping and we compare the performance of C-band SLG EAMs on TE and TM waveguides, showing the benefit of using TM waveguides. In section 4.3, on the same sample with p-type Si and using TM waveguides, we show uniform performance of SLG EAMs in the O-band, thus demonstrating broadband operation. In section 4.4, we conclude that the best performance is given by SLG EAMs on TM waveguides in the C-band, and we measure open eye diagrams up to 50 Gbit/s.

Table II. Summary of the level and type of Si doping on the three samples used for the experiment.

	Doping type	Slab doping (cm ⁻³)	Wg doping (cm ⁻³)
Sample A	n-doped	2.51e18	1.16e18
Sample B	n-doped	2.67e19	2.33e18
Sample C	p-doped	3.20e19	1.85e18

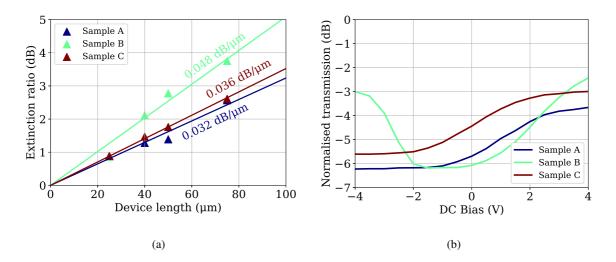


Fig. 8. (a) Extinction ratio as a function of device length of TE SLG EAMs, obtained by measuring the transmission at 1560 nm from -4 V to 4 V DC bias on three samples with different type and level of Si doping. The ER scales linearly with device length. (b) Transmission, normalised to the reference waveguide, as a function of applied DC bias, measured on TE SLG EAMs with $L_{device} = 75$ μm. Graphene is p-doped on all the samples.

4.1 Effect of Si waveguide doping on the performance of C-band TE SLG EAMs

We fabricated three samples with different type and level of doping in Si (summary in Table II). Sample A was fabricated with n-doped Si, with average carrier concentrations of $n_{slab}=2.5e18~{\rm cm}^{-3}$ and $n_{wg}=1.2e18~{\rm cm}^{-3}$ for the slab and the waveguide regions respectively. Sample B was fabricated using higher n-doping in the Si slab and waveguide regions than sample A ($n_{slab}=2.7e19~{\rm cm}^{-3}$ and $n_{wg}=2.3e18~{\rm cm}^{-3}$), with the purpose of reducing the total parasitic resistance without significantly impacting the GOS capacitance. Sample C was fabricated using p-doped Si ($p_{slab}=3.2e19~{\rm cm}^{-3}$ and $p_{wg}=1.9e18~{\rm cm}^{-3}$). The characterisation of the samples was carried out under ambient conditions.

The three samples were first characterised by performing unbiased fiber-to-fiber transmission measurements on SLG EAMs with waveguides optimised for TE mode propagation (TE waveguides, $W_{wg} = 500$ nm) and with four different device lengths ($L_{device} = 25$, 40, 50 and 75 µm). The transmission scales linearly with the device length, and the extracted average and standard deviation values of absorption are 0.08 ± 0.01 , 0.08 ± 0.01 and 0.05 ± 0.01 dB/µm for samples A, B and C respectively.

We then performed biased fiber-to-fiber transmission measurements on the same EAMs, by sweeping the wavelength from 1510 nm to 1600 nm, while applying a DC bias ranging from -4 V to 4 V. Fig. 8(a) shows the extracted extinction ratio (ER) versus device length (L_{device}) for the three samples at the peak transmission wavelength of 1560 nm. The values

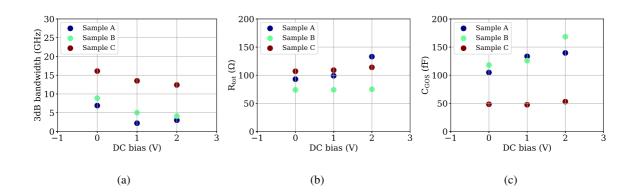


Fig. 9. (a) 3 dB frequency response, (b) total resistance R_{tot} and (c) GOS capacitance C_{GOS} as a function of DC bias of TE SLG EAMs with $L_{device} = 75 \, \mu m$ on the three samples. The values of R_{tot} and C_{GOS} were extracted from S₁₁ parameters fitting. Sample C exhibits higher f_{3dB} due to the lower C_{GOS} .

of ER scale linearly with the device length, reaching up to 2.6 dB for Samples A and C and 3.8 dB for sample B for $L_{device} = 75 \mu m$. An example of the extracted transmission as a function of DC bias at 1560 nm for $L_{device} = 75 \, \mu \text{m}$ is reported in Fig. 8(b). All three samples show minimum transmission of the modulation curve located at reverse bias. which indicates p-type doping in graphene. Sample B exhibits lower p-type graphene doping than the other two samples, which translates into the minimum transmission being shifted towards lower reverse bias. As a consequence, when the reverse bias on sample B is increased, graphene approaches again transparency, resulting in a more symmetrical transmission curve compared to the other two samples. The average and standard deviation values of modulation efficiency $(ME = ER/L_{device})$ across the four devices at 1560 nm are 0.03 ± 0.01 , 0.05 ± 0.01 and 0.04 ± 0.01 dB/µm for samples A, B and C respectively. The higher modulation in sample B is attributed to higher mobility in graphene compared to the other two samples. This is confirmed by the values of graphene's mobility extracted from transfer length measurements (TLM) of graphene's electrical test structures fabricated on the same sample (1610 $cm^2V^{-1}s^{-1}$ for sample B and 1490 $cm^2V^{-1}s^{-1}$ for sample C). The lower p-type graphene doping and the higher graphene mobility in sample B are attributed to sample-to-sample variations of graphene's properties, caused by uncontrolled variations in processing conditions.

The electro-optical S_{21} frequency response of the modulators was measured between 100 MHz and 30 GHz at DC bias ranging from 0 V to 2 V with a vector network analyser, using -8 dBm RF power and a 50 Ω load resistor. Fig. 9(a) compares the extracted 3 dB frequency response (f_{3dB}) of the three samples as a function of DC bias for $L_{device} = 75 \mu m$. Fig. 9(b) and 9(c) compare the extracted R_{tot} and C_{GOS} from the fitting of the S_{11} frequency response

Table III. Values of measured 3 dB frequency response (f_{3dB}) at 0 V DC bias on TE SLG EAMs for $L_{device} = 25, 40, 50$ and 75 μ m. The f_{3dB} is higher for sample C (p-doped Si) and for smaller device lengths.

	Measured f _{3dB} (GHz)				
	L = 25 μm	$L = 40 \mu m$	$L = 50 \mu m$	L = 75 μm	
Sample A	10.9	7.7	8.2	6.9	
Sample B	12.9	10.6	9.6	8.9	
Sample C	22.8	21.6	14.2	16.1	

measured on the three samples, performed using the equivalent electrical circuit shown in Fig. 1(b). Among the n-doped samples, sample B exhibits the highest 3 dB frequency response at any forward voltage bias, with a maximum value of 8.9 GHz at 0 V DC bias for $L_{device} = 75$ µm. The decrease in R_{tot} (20% at 0 V DC bias) achieved in sample B with the higher doping in the slab and waveguide regions, counteracts the slight increase in C_{GOS} caused by the higher waveguide doping (13% at 0 V DC bias). This allows to improve the f_{3dB} from sample A to sample B at any forward voltage bias, e.g. with a gain of 2 GHz (29%) at 0 V DC bias (Table III). As expected from the theoretical analysis, the sample fabricated using p-doped Si (sample C) shows a substantial increase in 3 dB frequency response compared to sample B, with values up to 22.8, 21.6, 14.2 and 16.1 GHz at 0 V DC bias for $L_{device} = 25$, 40, 50 and 75 µm respectively (Table III). Even though the Si sheet resistance is higher, the lower C_{GOS} obtained by operating the device in depletion mode instead of accumulation mode allows to significantly reduce the total RC constant, and thus enhance the 3 dB frequency response at any forward voltage bias. The values of f_{3dB} decrease with higher device length, due to the increase in the total RC constant related to the 50 Ω load resistor (Table III).

4.2 Performance comparison of C-band TE and TM SLG EAMs

Despite the high 3 dB frequency response achieved with the sample with p-doped Si (sample C), the ER of the SLG EAMs remains limited when using TE-polarised light, with values ranging from 0.9 dB for $L_{device} = 25 \, \mu m$ to 2.6 dB for $L_{device} = 75 \, \mu m$. The performance with TE-polarised light can be improved by using an optimised waveguide thickness [33, 34]. However, in our case this approach is not possible due to specific waveguide height requirements of the fab used to fabricate the substrate. Using waveguides optimised for TM mode propagation (TM waveguides) can increase the ER for a given device length, due to the bigger overlap between the TM optical mode and the graphene layer compared to TE when the waveguide thickness is 220 nm (see inset of Fig. 10(a)). To maximise the overlap with graphene but still ensure mode confinement in the waveguide, we use a waveguide width of

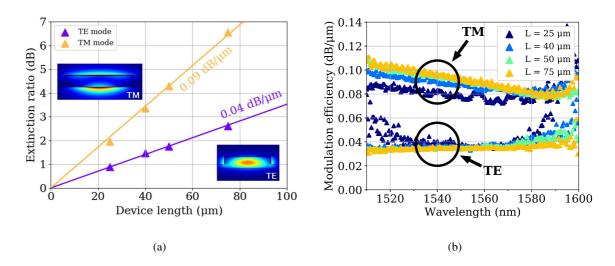


Fig. 10. (a) Comparison of measured extinction ratio on sample C between TE mode and TM mode SLG EAMs. TM EAMs exhibit higher ER due to the bigger mode overlap with the graphene layer. (b) Modulation efficiency as a function of wavelength of the four TE and four TM C-band SLG EAMs on sample C. All the devices are broadband and the ME is consistent across the C-band spectrum.

750 nm [5]. Unbiased transmission measurements performed on sample C (p-doped Si) from 1510 nm to 1600 nm on SLG EAMs with TM waveguides, equivalent to the ones performed on TE waveguides, showed that graphene's absorption is 0.09 ± 0.01 dB/ μ m, which is 2.3 times higher than the 0.04 ± 0.01 dB/ μ m measured on TE waveguides, in agreement with the value of 2.2 extracted from Lumerical MODE simulations. The ME of the four SLG EAMs is consistent across the measured C-band spectrum for both TE and TM devices (Fig. 10(b)). The drawback in using TM waveguides comes from the wider waveguide width, which leads to higher sheet resistance and GOS capacitance, resulting in a 1.1 \sim 1.5 times lower 3 dB frequency response compared to TE waveguides (Fig. 11). Nevertheless, due to the low C_{GOS} at forward bias on the SLG EAMs with p-doped Si, TM waveguides exhibit 3 dB frequency response at 0 V DC bias of 20.7, 18.0, 15.7 and 14.2 GHz for $L_{device} = 25$, 40, 50 and 75 μ m respectively.

4.3 Performance of O-band TM SLG EAMs

To demonstrate the broadband operation of graphene devices, we measured TM graphene-Si EAMs fabricated on sample C with exactly the same processing steps and cross section, but designed to operate in the O-band. We characterised four devices, with same lengths as the TM C-band devices demonstrated earlier ($L_{device} = 25$, 40, 50 and 75 μ m) and waveguide width of 380 nm. Fiber-to-fiber transmission measurements from 1260 nm to 1330 nm, resulted in an average absorption across the four devices of 0.10 ± 0.01 dB/ μ m. The biased transmission

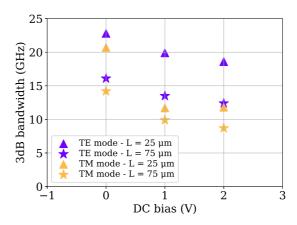


Fig. 11. Comparison of 3 dB frequency response between TE and TM SLG EAMs measured on sample C as a function of applied DC bias for different device lengths. TM SLG EAMs have lower f_{3dB} than TE SLG EAMs.

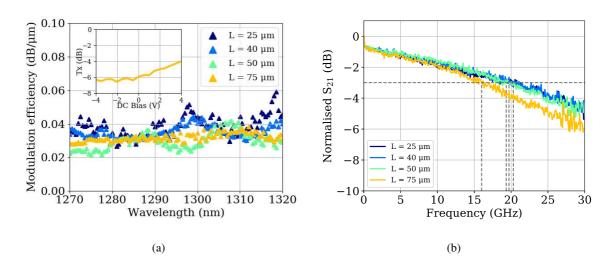


Fig. 12. (a) Modulation efficiency as a function of wavelength of the four TM O-band SLG EAMs. The devices are broadband and the ME is consistent across the O-band spectrum. Inset: normalised transmission as a function of applied DC bias measured on the 75 m-long EAM. (b) S_{21} parameters measured on the four TM O-band SLG EAMs at 1 V DC bias.

measurements were performed sweeping the DC bias from -4 V to 4 V and the wavelength from 1270 nm to 1320 nm. The average and standard deviation values of ME at the peak of the fiber grating couplers (1300 nm) across the four devices are 0.041 ± 0.005 dB/ μ m. The lower modulation efficiency compared to C-band TM devices is due to the higher energy of the photons in the O-band. As a consequence, it's necessary to apply a higher voltage in order to achieve full transparency in graphene, which may result in oxide breakdown. The extracted ME of the four TM O-band SLG EAMs is consistent across the O-band spectrum, as shown in Fig. 12(a). The 3 dB frequency response of the O-band SLG EAMs, extracted

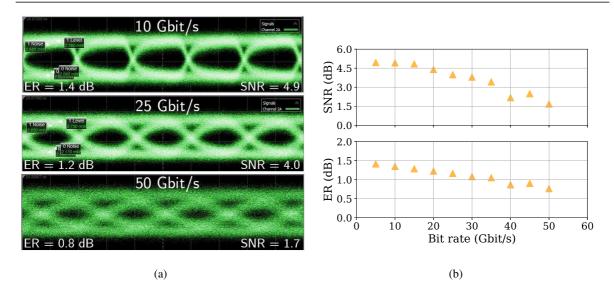


Fig. 13. (a) Eye diagrams measured at 10, 25 and 50 Gbit/s on the SLG EAM with p-doped Si, TM waveguide and $L_{device} = 75 \mu m$ (sample C). (b) SNR and large-signal extinction ratio plotted as a function of the bit rate for the same device. The SNR and the ER remain higher than 3.0 and 1.0 dB respectively up to 35 Gbit/s.

from electro-optical S₂₁-parameters measurements at 1300 nm wavelength, reaches values of 19.7, 20.3, 19.3 and 16.0 GHz at 1 V DC bias for L_{device} = 25, 40, 50 and 75 μ m respectively (Fig. 12(b)).

4.4 Large signal high speed performance

A summary of the performance of the C-band TE, C-band TM and O-band TM SLG EAMs on sample C is reported in Table IV for $L_{device} = 75 \, \mu m$. The FOM is defined as ER/IL and should therefore be as high as possible. The C-band TM EAM represents the best compromise between IL and ER, as shown by the high value of FOM, while also exhibiting a 3 dB frequency response of 14 GHz. Eye diagrams were measured on the C-band SLG EAM with p-doped Si (sample C), TM waveguide and $L_{device} = 75 \, \mu m$ at 1560 nm using 2^{23} -1 PRBS, 2.5 V_{pp} , 14 dBm input optical power and a 50 Ω terminated probe. Open eye diagrams were generated

Table IV. Summary of the main figures of merit measured on the three types of SLG EAMs on sample C (p-doped Si). The values reported are for 75 μ m-long devices. The FOM is calculated as ER/IL. The C-band TM SLG EAM offers the best trade-off.

	IL (dB)	ER (dB)	FOM	\mathbf{f}_{3dB} (GHz)	λ (nm)
C-band TE	3.0	2.6	0.9	16.1	1510 - 1600
C-band TM	4.2	6.5	1.5	14.2	1510 - 1600
O-band TM	4.0	3.1	0.8	16.0	1270 - 1320

from 5 Gb/s up to 50 Gbit/s, thus demonstrating potential for high speed data transmission using graphene technology. Examples at 10 Gbit/s, 25 Gbit/s and 50 Gbit/s are shown in Fig. 13(a). The large-signal ER and the signal-to-noise ratio (SNR) are reported in Fig. 13(b) as a function of bit rate. The dynamic energy consumption ($E_{bit} = CV^2/4$) of the SLG EAM is calculated to be ~ 112 fJ, while the static power consumption is < 10^{-8} mW, due to the low leakage current flowing through the GOS capacitor (< 10 pA).

5. Conclusion

In this paper we analysed the DC and high-speed performance of single-layer graphene-silicon EAMs. Three samples were fabricated by transferring p-doped graphene on Si waveguides with different type and level of silicon doping. By means of a theoretical model, the influence of the waveguide doping on the total parasitic resistance and capacitance of single-layer graphene-silicon electro-absorption modulators was discussed and compared to experimental results from the three samples. We found that the best static and high speed performance is obtained on SLG EAMs fabricated using p-doped silicon waveguides. We demonstrated high speed performance on SLG EAMs in the O-band and in the C-band, for a total wavelength range of 140 nm. On a 75 μ m-long O-band TM SLG EAM, we achieved 3.1 dB extinction ratio and 16.0 GHz 3 dB frequency response at 1 V DC bias at 1300 nm wavelength. In the C-band, we demonstrated a 75 μ m-long broadband SLG EAM with 6.5 dB extinction ratio and 14.2 GHz 3 dB frequency response at 0 V DC bias at 1560 nm wavelength. Open eye diagrams were obtained up to 50 Gbit/s using 2.5 V_{pp} and -0.5 V DC bias at 1560 nm, thus showing potential for the integration of single-layer graphene modulators in high-speed integrated photonics.

Acknowledgment

We deeply thank Antonino Contino for useful discussions regarding the modeling of graphene. The authors acknowledge imec's industrial affiliation Optical I/O program. This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No. 785219.

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