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Simplified Space Vector Pulse Width Modulation Based on Switching Schemes with Reduced Switching Frequency and Harmonics for Five Level Cascaded H-Bridge Inverter

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Article Info	ABSTRACT
	This paper presents a simplified control strategy of SVPWM with a three segment switching sequence and 7 segment switch frequency for high power multilevel inverter. In the proposed method, the inverter switching sequences are optimized for minimization of device switching sequence frequency and improvement of harmonic spectrum by using the three most derived switching states and one suitable redundant state for each space vector. The proposed 3-segment sequence is compared with conventional 7-segment sequence similar for five level Cascaded H-Bridge inverter with various values of switching frequencies including very low frequency. The output spectrum of the proposed sequence design shows the reduction of device switching frequency and states current and line voltage. THD this minimizing the filter size requirement of the inverter, employed in industrial applications. Where sinusoidal output voltage is required.

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1. INTRODUCTION

With ever increasing demand, of electrical energy and depleting fossil fuel reserves, the efficiency utilization of existing resources have become compelling requirement. High efficiency power electronic converter topologies with optimized control strategies are required to minimize the energy waste and improve the power quality. The design of controlled medium voltage drives is faced with challenges that relate to the topologies and control of the and motor side converters .The voltage and currents wave forms are effected by factors like topology used the control algorithm the filter size, choice of switching frequency and the application .The switching on of medium voltage semi conductor devices also make up the major part of device losses, their reduction allows the maximum output power while the other side the reduction of switching frequency causes the increased harmonic distortion of motor side waveforms. Thus the area need careful consideration for efficient drive system [1]. Multi level converter after many advantages like good power quality, low switching losses, high voltage capability, and low dv/dt stress [2].

The three bench mark topologies for high power medium voltage applications are neutral point clamped, series cascaded H-bridge, flying capacitor converter cascaded H bridge VSC has been applied for high power and power quality industrial requirement due to it series expansion capabilities in industrial main applications include, active filter, reactive power compensation, electric vehicles photo voltaic power conversion, ups etc. this topology can be operated at different switching frequencies for different application [3]. The H-bridge is supplied by isolated d.c. sources, composed of multiphase diode rectifiers.

Among the various switching algorithms. Proposed in the literature for multi level converters, SVM is the most promising one, which offers greatest flexibility in optimizing the switching pattern design and also well suited for digital implementation.SVM with 7-segment sequence is generally used for 2-level and 3-level inverter topologies. For higher level inverter because of difficulty due to overwhelming complexity of switching sequence design and heavy relative compilation load.The compilation load have been successfully reduced by simplifying the required calculation of reference vector location duty cycle calculation [4]. These are number of publications in the literature covering various aspects such as neutral point stabilization over modulation common mode voltage reduction SVM [5-6]. The main focus of this paper is on the implementation of switching sequence design. This paper presents simplified and generalized SVM algorithm with 3-segment and 7-segment switching sequence inducing over modulation operation to improve the output voltage spectrum by minimizing the device switching frequency. The performance of the proposed sequence design is analyzed through extensive simulations for five levels. Cascaded H-bridge inverter.

2.   SPACE VECTOR MODULATION METHOD

For a typical three, five, and seven-level cascaded H-bridge inverter, with a separate dc power supply is used for each H- Bridge. Its corresponding space voltage vector diagram is illustrated in Figure 1. For the 5-level inverter, there are 96 small triangles and the vertex of each triangle represents a space vector. The hexagonal vectors can be divided into six major triangular sectors (I to VI). Only the first sector of the coordinate is used because the vectors located in the other sectors can be transformed to first sector by clockwise rotating by an angle of $k*pi/3$, k=(1,2,3,4,5 for sector 2 to 6). As all the sectors are identical, only details of sector 1 is given in Figure 2.
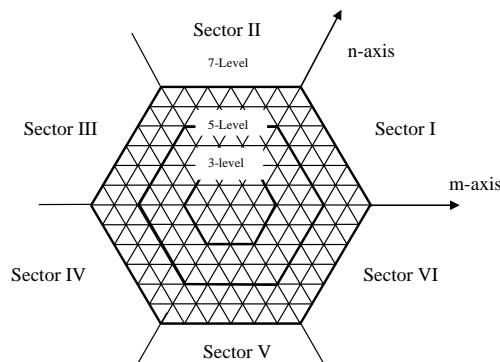

Figure 1. Voltage vectors of 3,5 and 7-level voltage source inverters

For N-level inverter there are N3 switching states that lie over $6(N-1)^2$ triangles. Figure 2 gives the representation of all the space vectors of the inverter in 60° co-ordinate system, the location of the reference vector is identified according to the condition given in Table 1 and all the coordinates are obtained and dwell times are calculated based on volt-second balance principle. After identifying all the switching states ,out of many redundant states desired and suitable redundant states are utilized for the sequence, in the implementation of the proposed switching sequence the most desired switching state along with suitable redundant state are utilized based on the nature of the co-ordinates (g ,h) of the reference vector the triangles are classified asType-I,Type-II and Type-III.
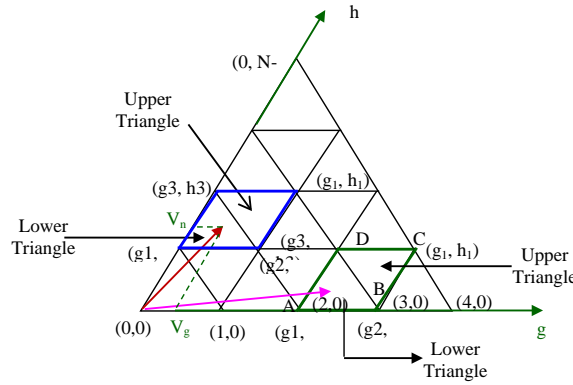
Figure 2. Voltage vectors in 60° co-ordinate system of five level inverter

Table 1. Determination of Triangle of Reference Vector

$(V_g + V_h) > (g + h + 1)$	$(V_g + V_h) \leq (g + h + 1)$
Reference Vector lies in triangle BDA	Reference Vector lies in triangle CBD
$g_1 = g + 1; \, h_1 = h + 1$	$g_1 = g; \, h_1 = h$
$g_2 = g + 1; \, h_2 = h$	$g_2 = g + 1; \, h_2 = h$
$g_3 = g; \, h_3 = h + 1$	$g_3 = g; \, h_3 = h + 1$

$$g_1 \, T_1 + g_2 \, T_2 + g_3 \, T_3 = T_{ref} V_g \tag{1}$$

$$h_1 \, T_1 + h_2 \, T_2 + h_3 \, T_3 = T_{ref} V_h \tag{2}$$

$$T_1 + T_2 + T_3 = T_{ref} \tag{3}$$

All the triangles of the space vector diagram are classified based on the integer coordinates of the reference vector in 60° axis and are given as:

Type-I: where both (g, h) are odd or even the three most desired states for the three vertices of (g1,h1) (g2,h2) (g3,h3) are $\left([\mathrm{SRi}, \mathrm{SYi}, \mathrm{SBi}]_{i=1,2,3} \right)$ and one redundant state $S'_{jr} = \left[S'_{Rr}, S'_{Yr}, S'_{Br} \right]_{r=2}$ that exists for space vector (g2,h2).

Type-II: for the location of reference vector Vr is g1 is even and h1 is odd, the three most desired states are $\left([\mathrm{SRi}, \mathrm{SYi}, \mathrm{SBi}]_{i=1,2,3} \right)$ and the redundant state $S'_{jr} = \left[S'_{Rr}, S'_{Yr}, S'_{Br} \right]_{r=1}$ for the space vector (g1,h1).

Type-III: if g1 is odd and h1 is even the most desired state $\left([\mathrm{SRi}, \mathrm{SYi}, \mathrm{SBi}]_{i=1,2,3} \right)$ and the redundant state $S'_{jr} = \left[S'_{Rr}, S'_{Yr}, S'_{Br} \right]_{r=1}$ for the space vector (g1,h1).

Switching sequence design:

The unique switching stator in each triangle are determined using three most desired switching states $\left([S_{ji}]_{i=1,2,3} \right)$ and one switching redundant state $\left(S'_{jr} = \left[S'_{Rr}, S'_{Yr}, S'_{Br} \right]_{r=1,2,3} \right)$ are utilized for implement 7 segment and 3-segment switching sequence.

7-segment switching sequence:

In conventional SVM 7 segment switching sequence is implemented for two level or 3-level SVM for real time implementation because of increased computational burden because of large number of switching states of multilevel inverter for higher level becomes overwhelming.

In the proposed SVPWM method the optimum switching states are selected for the sequence such that there will be only one voltage level charges per commutation.

The 7 segment switching sequence for different types of triangles are:

Type-I: triangle are

$$\left[S_{j2}\left(\frac{T_2}{4}\right)\right] \to \left[S_{j1}\left(\frac{T_1}{2}\right)\right] \to \left[S_{j3}\left(\frac{T_3}{2}\right)\right] \to \left[S_{j2}'\left(\frac{T_2}{2}\right)\right] \to \left[S_{j3}\left(\frac{T_3}{2}\right)\right] \to \left[S_{j1}\left(\frac{T_1}{2}\right)\right] \to \left[S_{j2}\left(\frac{T_2}{4}\right)\right]$$

(4)

Type-II: triangle are

$$\left[S_{j1}\left(\frac{T_1}{4}\right)\right] \to \left[S_{j2}\left(\frac{T_2}{2}\right)\right] \to \left[S_{j3}\left(\frac{T_3}{2}\right)\right] \to \left[S_{j1}'\left(\frac{T_1}{2}\right)\right] \to \left[S_{j3}\left(\frac{T_3}{2}\right)\right] \to \left[S_{j2}\left(\frac{T_2}{2}\right)\right] \to \left[S_{j1}\left(\frac{T_1}{4}\right)\right]$$

(5)

Type-III: triangle are

$$\left[S_{j1}\left(\frac{T_1}{4}\right)\right] \to \left[S_{j3}\left(\frac{T_3}{2}\right)\right] \to \left[S_{j2}\left(\frac{T_2}{2}\right)\right] \to \left[S_{j1}'\left(\frac{T_1}{2}\right)\right] \to \left[S_{j2}\left(\frac{T_2}{2}\right)\right] \to \left[S_{j3}\left(\frac{T_3}{2}\right)\right] \to \left[S_{j1}\left(\frac{T_1}{4}\right)\right]$$

(6)

Generalized three or five segment switching sequence consisting of three most desired states [Sji]i=1,2,3 of three types of triangle is expressed as
Type-1:

$$\left[S_{j2}\left(\frac{T_2}{2}\right)\right] \to \left[S_{j1}\left(\frac{T_1}{2}\right)\right] \to \left[S_{j3}(T_3)\right] \to \left[S_{j1}\left(\frac{T_1}{2}\right)\right] \to \left[S_{j2}\left(\frac{T_2}{2}\right)\right]$$

(7)

Type-2:

$$\left[S_{j1}\left(\frac{T_1}{2}\right)\right] \to \left[S_{j2}\left(\frac{T_2}{2}\right)\right] \to \left[S_{j3}(T_3)\right] \to \left[S_{j2}\left(\frac{T_2}{2}\right)\right] \to \left[S_{j1}\left(\frac{T_1}{2}\right)\right]$$

(8)

Type-III:

$$\left[S_{j1}\left(\frac{T_1}{2}\right)\right] \to \left[S_{j3}\left(\frac{T_3}{2}\right)\right] \to \left[S_{j2}(T_3)\right] \to \left[S_{j3}\left(\frac{T_3}{2}\right)\right]\left[S_{j1}\left(\frac{T_1}{2}\right)\right]$$

(9)

In 3-segment switching sequence the leading and trailing state over a switches period is same as 7-segment switching sequence.

Calculation of switching frequency:
For any multilevel inverter the switching devices may not have the same device switching frequencies.
The average switching frequency is defined as total number of switching of all the switches per second to the number of active devices of the inverter (F avg = sw)
$f_{(avg = sw)} = F_{(ideal -avg-sw)}$
If leading state of the next sequence is equal to trailing state of the proceeding sequence.

$$F_{ideal-Avg-Sw} = \frac{(N_{ph})(N_s)fs}{N}$$

10)

Nph – Number of commutating phases
Ns – Number of complete switching actions ('on' and 'off' transition) per phase
a/d – Number of devices per commutation
fs = switching frequency

Table3. Frequency Components for 7-segment and 3-segment Switching Patters
for Five Level Cascaded Inverter

| Frequency | Frequency components of different switching patterns | |
	7-segment	3-segment
$F_{(ideal\text{-}avg\text{-}sw)}$	$$\frac{(3 \times 1) \times 2\,fs}{24} = \frac{fs}{4}$$	$$\frac{2 \times \left(\dfrac{1}{2}\right) \times 2\,fs}{24} = \frac{fs}{12}$$
Equivalent inverter frequency	$fs = 4F_{(ideal\text{-}Avg\text{-}sw)}$	$fs/2 = 6F_{(ideal\text{-}Avg\text{-}sw)}$

For the some ideal average switching frequency the inverter equivalent frequency for 3-segment will be double that of 7-segment sequence (50% more)

For the same inverter equivalent frequency, the ideal average switching frequency for three segment is equal to two third of the corresponding 7-segment sequence number of extra commutations also increases the device frequency and average switching frequency.

3. RESULTS AND DISCUSSIONS

The performance of the above switching sequences is evaluated for Five level cascaded H- Bridge Inverter with DC input voltage of 100V. corresponding to the modulation index of 0.87.The parameters of simulation are, Figure 1 gives the line voltage spectrum over broder range (12500Hz) with inverter switching frequency of 2100Hz. The harmonics appear as first side band around inverter equivalent frequency. The ideal average device switching frequency being 525Hz.The THD obtained for 7-seg is 19.41. For the same ideal average device switching frequency, the inverter is simulated for 3-segment switching frequency. The harmonics appear as first side band around inverter equivalent frequency of 3150Hz.The magnitude of harmonics is reduced to larger amount giving lesser value of THD which is 16.32.
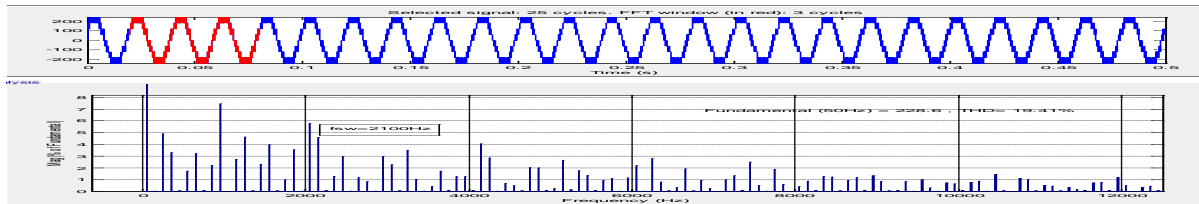

Figure 3. Line voltage spectrum of five level cascaded inverter over 12.5KHz with seven-segment switching sequence
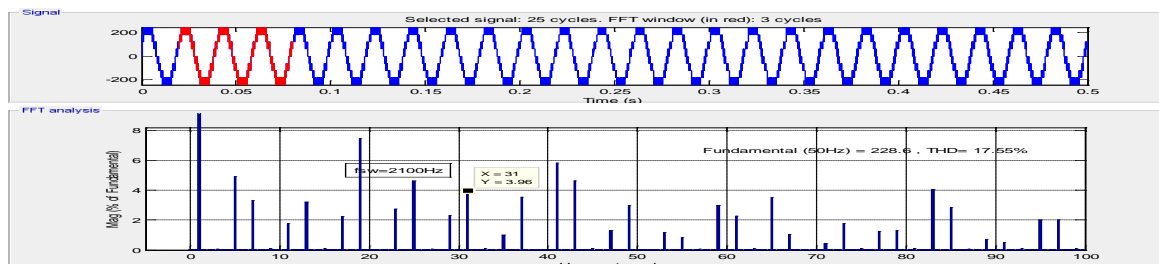

Figure 4. Line voltage spectrum of five level cascaded inverter over 5KHz with seven-segment switching sequence
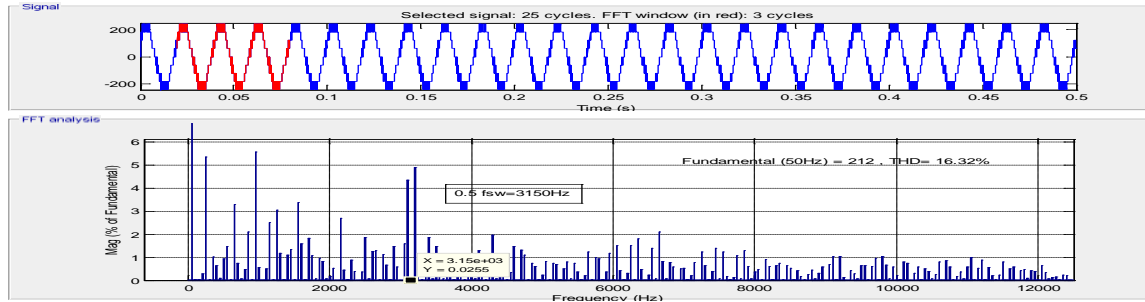
Figure 5. Line voltage spectrum of five level cascaded inverter over 12.5KHz with
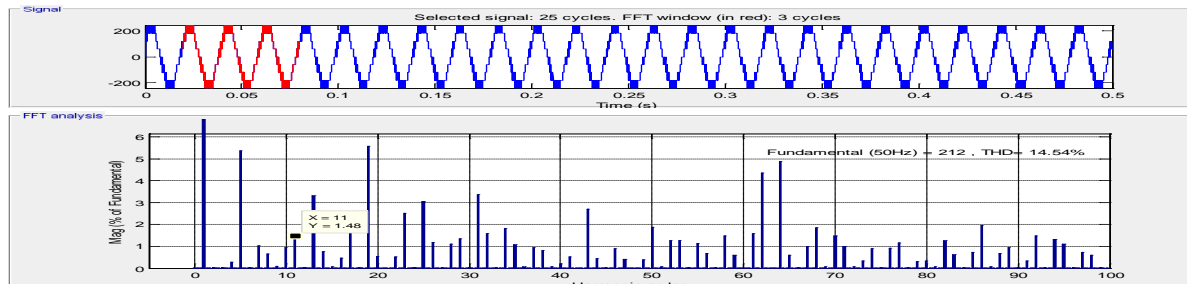three-segment switching sequence

Figure 6. Line voltage spectrum of five level cascaded inverter over 5KHz with
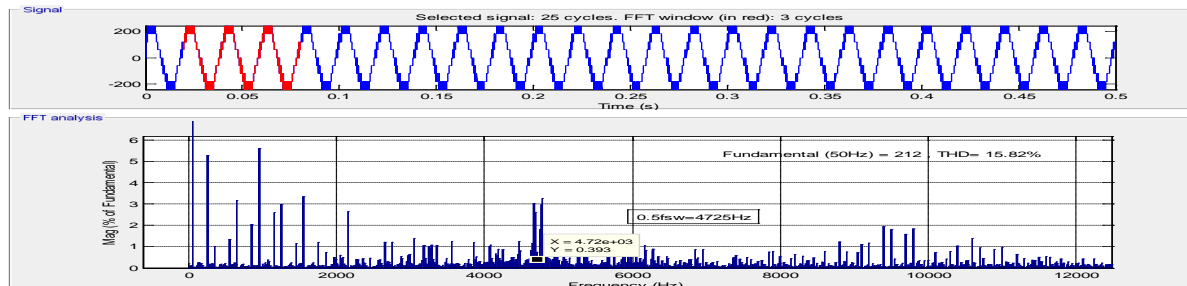three-segment switching sequence

Figure 7. Line voltage spectrum of five level cascaded inverter over 12.5KHz with three-segment switching
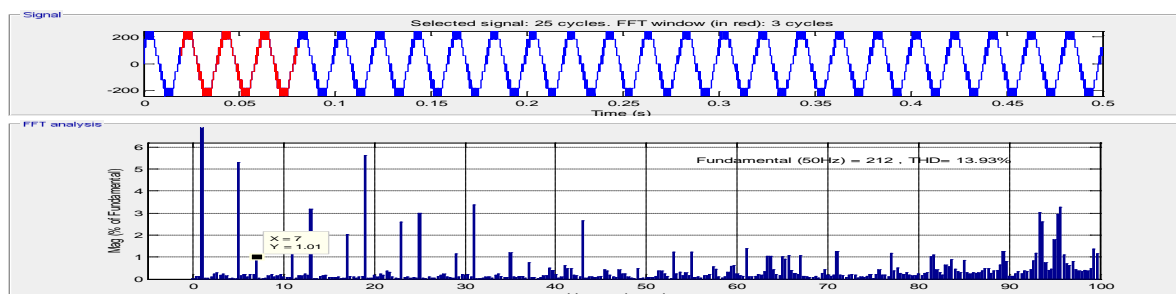sequence with switching frequency of 4745Hz

Figure 8. Line voltage spectrum of five level cascaded inverter over 5KHz with three-segment switching
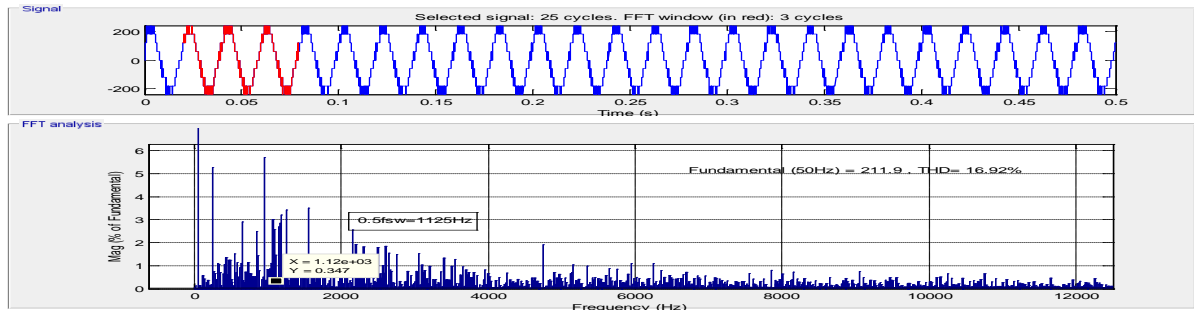sequence with switching frequency of 4725Hz

Figure 9. Line voltage spectrum of five level cascaded inverter over 12.5KHz with three-segment switching sequence with switching frequency of 750Hz
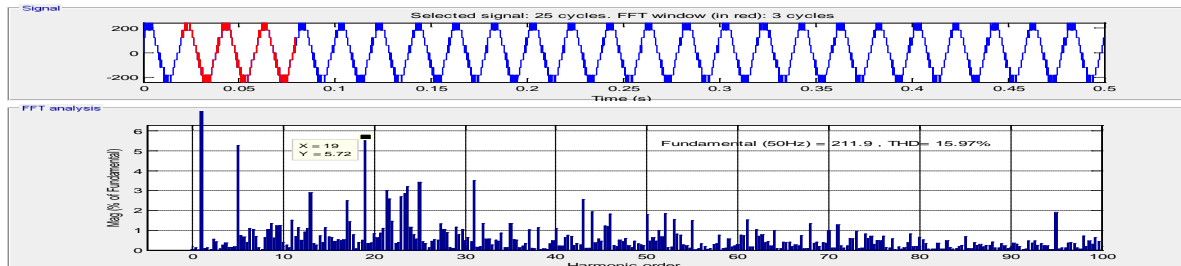
Figure 10. Line voltage spectrum of five level cascaded inverter over 5KHz with three-segment switching sequence and switching frequency of 750Hz
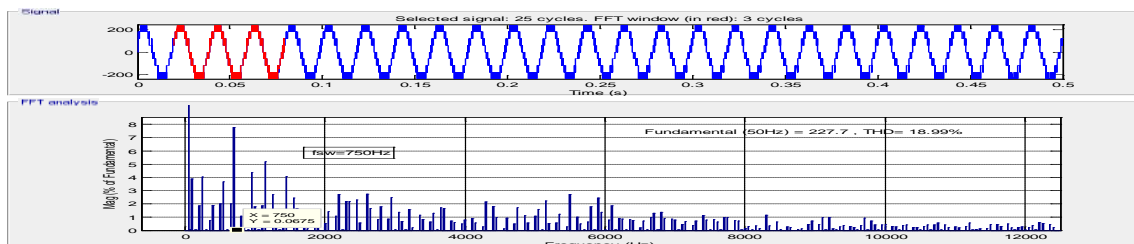
Figure 11. Line voltage spectrum of five level cascaded inverter over 12.5KHz with seven-segment switching sequence with switching frequency of 750Hz
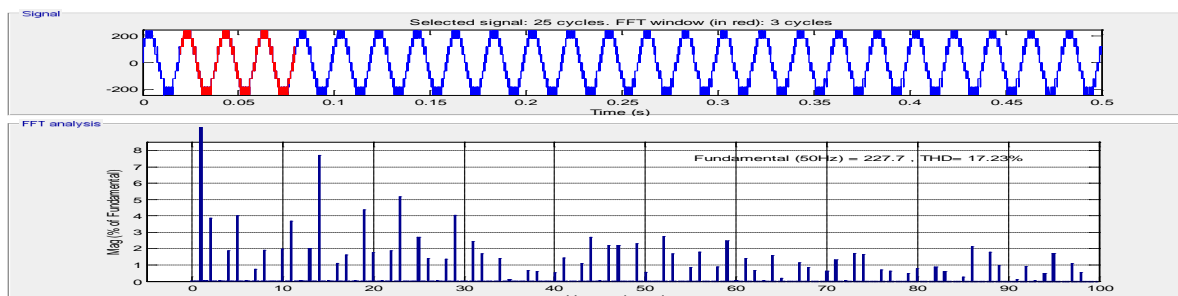
Figure 12. Line voltage Spectrum of Five level cascaded inverter over 5KHz with seven-segment switching sequence with switching frequency of 750Hz

4. CONCLUSION

       This paper presents general SVPWM based seven –segment and three-segment online switching scheme for N-level inverter. The two sequences are simulated for five level cascaded inverter. One of the

important feature of this technique is that,out of large number of switching states of the five level inverter , the desired switching states and most suitable redundant states are selected for the both sequences such that the technique is implemented online with no need of lookup table. In the three-segment switching sequence, the inverter equivalent frequency is 50% higher than that of seven-segment, harmonics appear as sideband around high inverter frequency, and the magnitude of lower order harmonics is reduced for three segment giving lesser value of THD when compared to that of sevens-segment.

REFERENCES

[1]   J. Rodríguez, J. Lai, and F. Peng, "Multi level converters: a survey of topologies, controls and applications," *IEEE Trans. Ind. Electron.*, Vol. 49, No.4, pp. 724-738, Aug. 2002.

[2]   P.Satish Kumar, J.Amarnath, S.V.L. Narasimham, "A fast space-vector pulse with modulation method for diode-clamped multi-level inverter fed induction motor" *Asian Power Electronics Journal*, vol.4, No..1, April 2010.

[3]   P.Satish Kumar , "A New General Topology for Cascaded Multilevel Inverters with Increased Number of levels Based on Diagonal DC Source H-Bridge", *International Journal of Advances in Electrical and Electronics Engoneering*,Vol.3,No.3,pp.175-184,2014.

[4]   A.Nabae, I. Takahashi, cd H.Akagi, "A new neutral-point clamped pwm inverter". *IEEE Trans. Ind. Appl.*, vol.1A-17, no.5, pp.518-523, sept/oct 1982.

[5]   l. yiqiao, and c.o. nwankpa, "a new type of statcom based on cascading voltage source inverters with phase-shifted unipolar spwm," *IEEE trans. on industry applications*, vol.35, no.5, 1999, pp.1118-1123.

[6]   d.w. kang, y.h. lee, b.s. suh, c.h. choi, and d.s. hyun, "a carrier wave-based svpwm using phase-voltage redundancies for multilevel h-bridge inverter," International conference on Iindustrial Electronics, control, and instrumentation (iecon), vol.1, 1999, pp.324-329.