Depletion induced depolarization field in $Hf_{1-x}Zr_xO_2$ Metal-Ferroelectric-Semiconductor capacitors on germanium.

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ABSTRACT

Germanium Metal-Ferroelectric-Semiconductor (MFS) capacitors based on ferroelectric $Hf_{1-x}Zr_xO_2$ (HZO) with clean, oxide free Ge/HZO interfaces emerge as an interesting layer structure for the fabrication of FeFET non-volatile memory devices. It is shown that, at low temperature (<160 K), a semiconductor depletion forms in Ge near the interface resulting in an increase of coercive voltage by about 2 V, accompanied by a distortion of the ferroelectric hysteresis with subloop asymmetric behavior, which becomes more severe at higher frequencies of measurement. At higher temperatures, the Ge surface near the ferroelectric is easily inverted due to low energy gap of Ge, providing sufficient screening of the polarization charge by minority free carriers, in which case, nearly ideal, symmetric hysteresis curves are recovered. The depolarization field is experimentally extracted from the coercive voltage and the capacitance measurements and is found to be ~ 2.2 MV/cm in the low temperature range, comparable to the coercive field, then rapidly decreasing at higher temperatures and effectively diminishing at room temperature. This makes Ge MFS good candidates for FeFETs for low voltage non-volatile memory with improved reliability.

Metal-Ferroelectric-Metal capacitors made of Si-compatible $Hf_{1-x}Zr_xO_2$ with x~0.5 (HZO) ferroelectric (FE) have been extensively studied[1-5] for low power 1T-1C non-volatile embedded memories integrated in the back-end-of-line (BEOL) of CMOS[6]. A different device layer structure, namely Metal-Ferroelectric-Semiconductor (MFS) is the main building block of 1T ferroelectric field effect transistor (FeFET) non-volatile memories[7] which have potential advantages in terms of scaling, non-destructive reading and front-end-of-line (FEOL) integration with CMOS. Moreover, they can be used to realize artificial ferroelectric integrate-and-fire neurons[8] and analog synapses[9, 10] for neuromorphic computing[11]. Si MF(I)S draw a lot of attention but the presence of Si bottom electrode in direct contact with the HZO produces interfacial SiOx or Hf(Zr) silicate insulating layers which cause reliability problems for FeFETs[12]. Depolarization fields in particular can severely affect the hysteresis loop[11, 12] at room temperature (RT) by reducing the attainable switchable polarization as well as the memory window, thus directly impacting memory performance.

FeFETs on technologically important Ge[13] is an interesting alternative device that has already been successfully used for the fabrication of non-volatile analog memristive synapses functioning as accelerator for on-line learning in neuromorphic circuits[14]. Moreover, negative capacitance FETs with subthermionic steep slopes have been demonstrated in Ge/HZO FETs[15-17] suitable for low power/high performance applications.

Germanium MFS and FeFETs could help overcome some of the shortcomings of Si FeFETs. Notably, Ge/HZO interfaces are reported to be sharp and clean[18-20], free of interfacial oxides, which could mitigate some of the reliability issues. Despite the absence of an interfacial insulating layer, when the MFS is biased in depletion, the screening of polarization charge weakens, potentially creating a depolarization field in the ferroelectric which could adversely impact retention and imprint of memory states. This has motivated us to systematically investigate, as a function of temperature, the build-up of a depolarization field originating from depletion of Ge semiconductor near the interface. Our studies show that the formation of depletion in Ge at low temperatures (<160 K) creates a strong depolarization field which

severely distorts the hysteresis characteristics. However, at higher temperatures and especially at RT, due to its low energy gap (E_g), Ge has high minority carrier population, sufficient to screen the polarization charges in Ge MFS, essentially diminishing the depolarization field. As a result, nearly ideal, symmetric polarization curves are obtained[20-24].

TiN/HZO/Ge (100) MFS device layer structures were produced by plasma assisted atomic oxygen deposition in a molecular beam epitaxy chamber as described elsewhere (Ref [20]). In this work, three different samples are studied: a 12-nm-thick HZO film on a p-Ge substrate with resistivity ρ=(0.03-0.07) Ω·cm, a 13-nm-thick HZO on a highly doped n^+-Ge (0.004-0.006 Ω·cm) and a 13-nm-thick HZO on a lightly doped n-Ge (0.34-0.35 Ω·cm), all with Zr composition x~ 0.6.

As in our previous work[20], HZO is polycrystalline with grain size 15- 20 nm, comparable to the thickness as seen in Fig. 1(a). The HZO/Ge interface is crystalline and clean (Fig. 1(b)), free of interfacial oxide or germanate layers as expected[18-20].

Polarization (P) and displacement current (I) of the ferroelectric capacitors were measured using an aixAcct Systems TF Analyzer 1000. The capacitors showed robust and symmetric pristine hysteresis curves at RT with no wake-up effects and good electrical endurance of 10^5 cycles similar to those previously reported[20]. Temperature measurements from RT to 77 K were performed using a micromanipulator in high vacuum conditions.

Temperature and frequency data are presented in figures 2 and 3. In the case of MFS on n^+-Ge substrate (Fig. 2(a)-(b)), as temperature decreases, a slight shift of coercive voltage V_c to higher values is observed (ΔV~0.6V), which is nearly the same for both V_c^+ and V_c^-. This weak variation is attributed to a temperature dependence of the coercive field E_c as predicted by Landau-Ginzburg mean-field theory[25] and previously reported[26]. For the MFS on n-Ge substrate (Fig. 2(c)-(f)), V_c^+ is slightly increased (only by ~ 0.4 V), whereas V_c^- shows a significant shift of about 2 V to higher negative values as the temperature is lowered. The polarization loop gradually becomes non-ideal and asymmetric with reduced P_r, similar to the one observed in Si

based MF(I)S capacitor[11, 12]. It is worth noting that at higher frequencies (Fig. 2(c)-(f)), the degradation of hysteresis loop is more pronounced and the V_c^- shift is larger as the temperature is reduced (see detailed discussion later).

The opposite behavior is observed for the capacitor on p-Ge substrate (Fig. 3 (a)-(b)) where V_c^+ shows considerable shift of about 1.4 V as the temperature is lowered, while V_c^- remains nearly unchanged (maximum shift of ~0.5 V). For an in-depth investigation, high frequency capacitance-voltage (C-V) measurements were performed for p-Ge/HZO/TiN MFS capacitor (Fig. 3 (c)). At RT the characteristic "butterfly" ferroelectric peak configuration appears, indicating that the device essentially behaves like an MFM capacitor. With decreasing temperature, the gradual transition to a typical p-type MIS behavior is clearly seen which can be correlated with the evolution of the polarization curve.

Figure 4 presents the comparison between inverse total capacitance measured at depletion (+ 3.5 V) C_{dep}^{-1} and V_c^+, as obtained by displacement current measurements at two different frequencies (1 kHz and 100 Hz), at each temperature. Notably, both quantities follow the same trend, which indicates that the origin of the significant V_c^+ increase is the creation of a depletion region in the Ge semiconductor at low temperatures. More specifically, when positive voltage is applied on TiN top electrode at RT, the conduction band is populated, as dictated by the Fermi Dirac distribution, by a large number of electrons (minority carriers), due to low E_g of Ge, resulting in surface inversion (Fig. 5 (a)). Therefore, the free negative charge in inversion screens efficiently the positive polarization charge in such a way that the Ge bottom electrode behaves like a metal, yielding symmetric nearly ideal hysteresis as in MFM capacitors. At low temperatures, the Fermi Dirac distribution narrows so the population of the conduction band by minority carriers is diminished, while majority carriers are repelled from the interface (Fig. 5b). Therefore, the region near the interface is depleted from free carriers so the electric field penetrates the semiconductor depletion region causing an additional voltage drop and an associated depolarization field in the ferroelectric. This voltage drop explains the larger V_c^+ required to attain the E_c in the HZO ferroelectric. In contrast, in accumulation at negative bias,

the majority carrier concentration (holes) is not affected at lower temperatures, so V_c^- remains nearly the same. Similar description holds for n-type substrates where the role of V_c^+ and V_c^- is interchanged.

As already mentioned above, the effect of the depletion at low temperatures is more pronounced at higher frequencies of measurement. This is understood as follows: the few minority carriers do not respond fast enough to the electric field since electron-hole generation by interband transitions, typically mediated by mid-gap states near the interface, is a slow process. As a result, the inversion layer does not easily form at high frequencies, leaving the interface depleted from free carriers. The frequency effect could be mitigated or avoided by using highly doped substrates which show metallic behavior so the hysteresis remains near ideal at high frequency even at low temperatures (see n^+ Ge MFS in Fig. 2a).

For a quantitative analysis, the variation of V_c with the inverse total capacitance C per unit area at depletion is calculated as follows: The free charge per unit area Q_c stored in the capacitor can be expressed as $Q_c=CV_c$. On the other hand, from Gauss's law, $Q_c=D=\varepsilon_{FE}E_{FE}$, where D is the electric displacement, ε_{FE} is the dielectric constant and $E_{FE}=E_c+E_{dep}$ is the total electric field in the ferroelectric expressed as the sum of the E_c and the depolarization field E_{dep}. Then,

$$V_c = \varepsilon_{FE} C^{-1}\left(E_c + E_{dep}\right) \qquad (1)$$

which explains the similar behavior exhibited by V_c and C^{-1} in Fig. 4 as a function of temperature.

Equation (1) can be used to extract E_{dep} as a function of temperature from experimental data of V_c and C^{-1} as displayed in Fig. 4. This is particularly useful given that an estimate of E_{dep} is not easy to make. For example, the typically used expression $E_{dep}= -P/\varepsilon_{FE}(1+C_s/C_{FE})$[27] for the depolarization field requires the knowledge of the semiconductor capacitance C_s which is not easy to extract experimentally (P is the remanent polarization and C_{FE} is the ferroelectric capacitance).

In order to extract E_{dep} from eqn (1), $\varepsilon_{FE}=\varepsilon_0\cdot\varepsilon_r$ is estimated from the accumulation capacitance C_{acc}=1.94 μF/cm^2 at -3 V (Fig. 3 (c)) and the ferroelectric thickness d_{FE}=12 nm using $\varepsilon_{FE}= C_{acc}\cdot d_{FE}=23.3\cdot10^{-11}$ F/m. This calculation yields a relative dielectric constant ε_r=26.3, which is in fair agreement with reported[3] values of ~27 for the orthorhombic crystalline phase of HZO. Moreover, E_c in eqn (1) is obtained at each temperature from $E_c= V_c^-/d_{FE}$ by measuring V_c^- in accumulation (negative bias).

The absolute value of E_{dep} as a function of temperature is plotted in Fig. 6 along with E_c for comparison. E_c varies weakly and increases roughly linearly with decreasing temperature following the linear temperature dependence previously predicted[28] on the basis of Ginzbourg-Landau theory[25]. On the other hand, $|E_{dep}|$ is nearly zero at RT which is expected considering the efficient screening of polarization charges and increases slightly as the temperature drops to about 160 K. At lower temperatures, $|E_{dep}|$ increases sharply, essentially following the rapid increase of C^{-1} in Fig. 4 which signifies the formation of a depletion region. At the lowest temperature range, $|E_{dep}|$ reaches high values ~2.2 MV/cm which is comparable to the E_c value of 2.55 MV/cm (Fig. 6).

It should be noted that the formation of an inversion layer (Fig. 5a) may not be a roadblock for FeFET operation since the modulation from inversion to depletion can be controlled by the gate bias turning the transition from ON to OFF state as already demonstrated in the literature[15-17]. Any non-idealities such as low I_{ON}/I_{OFF} ratio may not affect the FeFET operation since the memory window depends mainly on the threshold voltage shift controlled by the ferroelectric state at the gate.

Although the present analysis has been performed based on Ge MFS which serves here as a model case study, the expression (1) is of general validity and holds for other semiconductor devices including Si MF(I)S, albeit with an additional complication in the analysis due to the presence of the insulating (I) layer. However, in the case of Si MF(I)S, due to the larger E_g of Si (~ 1.1 eV), a depletion layer and an associated finite E_{dep} are expected at RT, adversely affecting

the P-E characteristics which show subloop behavior and increased operation voltages, as previously reported[11, 12, 24]. Therefore, compared to Si devices, Ge MFS offer advantages: The absence of an insulating interfacial layer and the low E_g of Ge which prevents depletion, make depolarization fields insignificant at RT. This allows a symmetric and robust P-E hysteresis loop of Ge MFS at RT with effectively zero E_{dep}, which is essential for FeFET performance at low voltages with improved reliability.

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Data Availability Statement: The data that support the findings of this study are available from the corresponding author upon reasonable request.

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FIGURE CAPTIONS:

Figure 1: HRTEM cross-sectional images of HZO on p-Ge (100) substrate. (a) Microstructure of 13 nm ferroelectric HZO layer and (b) the sharp HZO/Ge interface, free of interfacial amorphous oxide layers.

Figure 2: Polarization and displacement current vs voltage measurements for MFS capacitors on (a)-(b) highly doped n^+-Ge and low doped n-Ge substrate at (c)-(d) 100 Hz and (e)-(f) 1 kHz. The arrows show the shift in the coercive voltages V_c^+ and V_c^- in accumulation and depletion/inversion, respectively.

Figure 3: (a) Polarization, (b) displacement current (at 100Hz) and (c) capacitance vs voltage measurements (1 kHz) at different temperatures for MFS capacitor on p-Ge substrate. The arrows in (b) show the shift of the coercive voltages V_c^+ and V_c^- in depletion/inversion and accumulation, respectively.

Figure 4: Temperature dependence of positive coercive voltage V_c^+ at 100 Hz (circles) and 1 kHz (triangles) and inverse capacitance C_{dep}^{-1} (squares) measured at +3.5 V in depletion for p-Ge MFS.

Figure 5: Schematic energy band diagrams of TiN/HZO/p-Ge device layer structure corresponding to high frequency measurements at positive applied bias V at (a) high temperature (inversion), (b) low temperature (depletion). ***E*** denotes the electric field vector which is largely confined in the HZO ferroelectric except in (b) where it penetrates the Ge depletion region giving rise to an additional voltage drop. ***P*** denotes the polarization vector in the ferroelectric. f_{FD} vs E is a schematic illustration of the Fermi Dirac distribution.

Figure 6: Temperature dependence of experimentally determined absolute value of the depolarization field E_{dep} and coercive field E_c for p-Ge MFS.

FIGURES

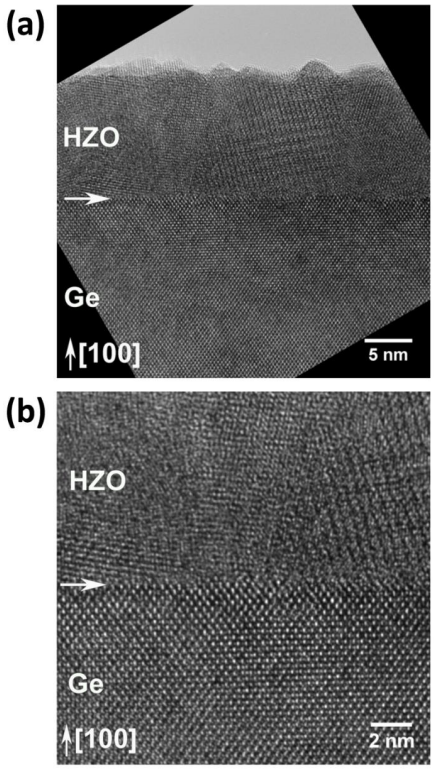

FIGURE 1

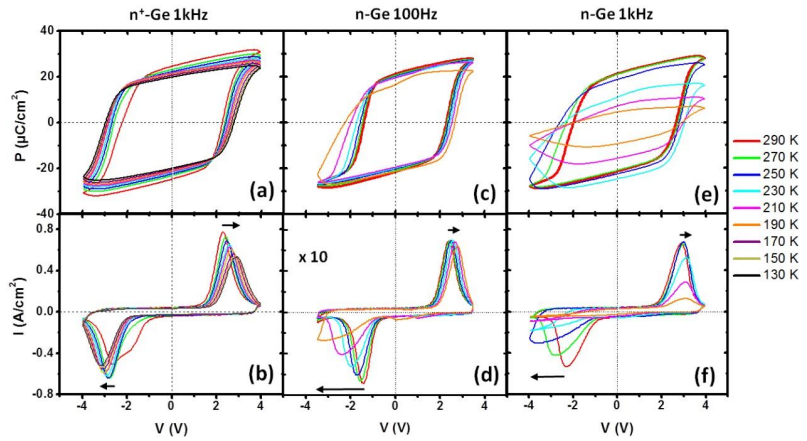

FIGURE 2

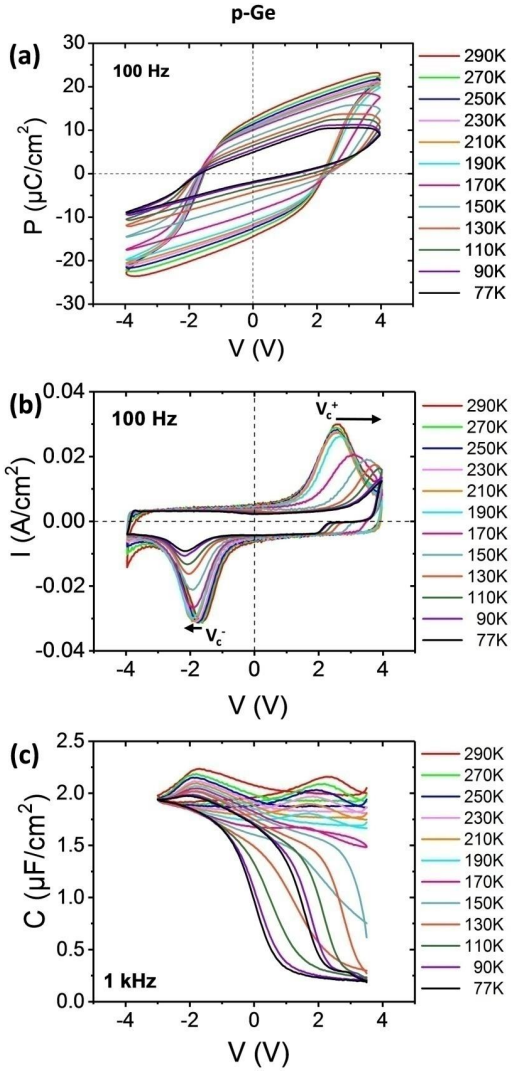

FIGURE 3

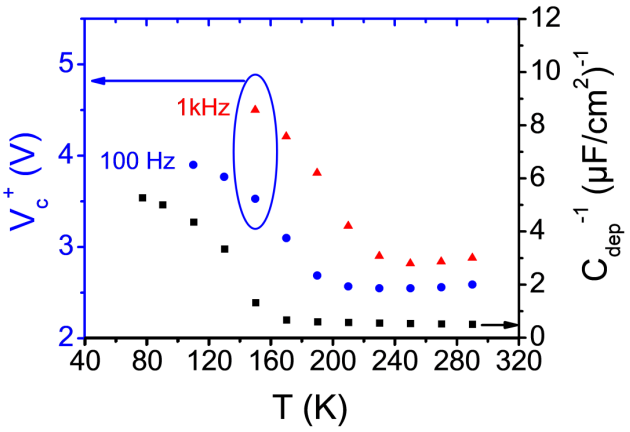

FIGURE 4

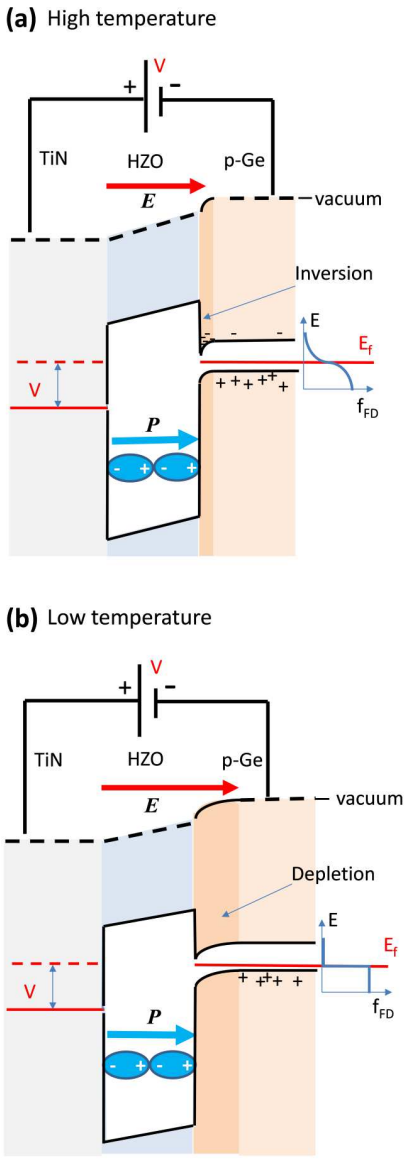

FIGURE 5

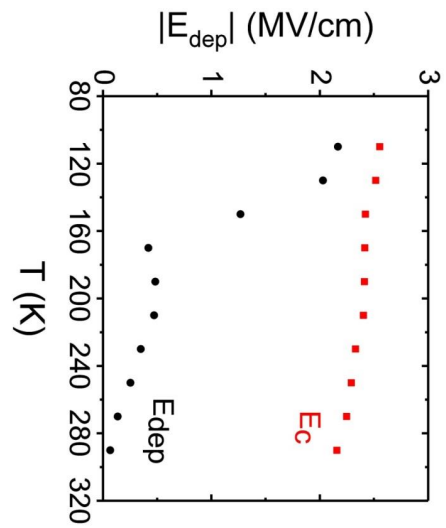

FIGURE 6

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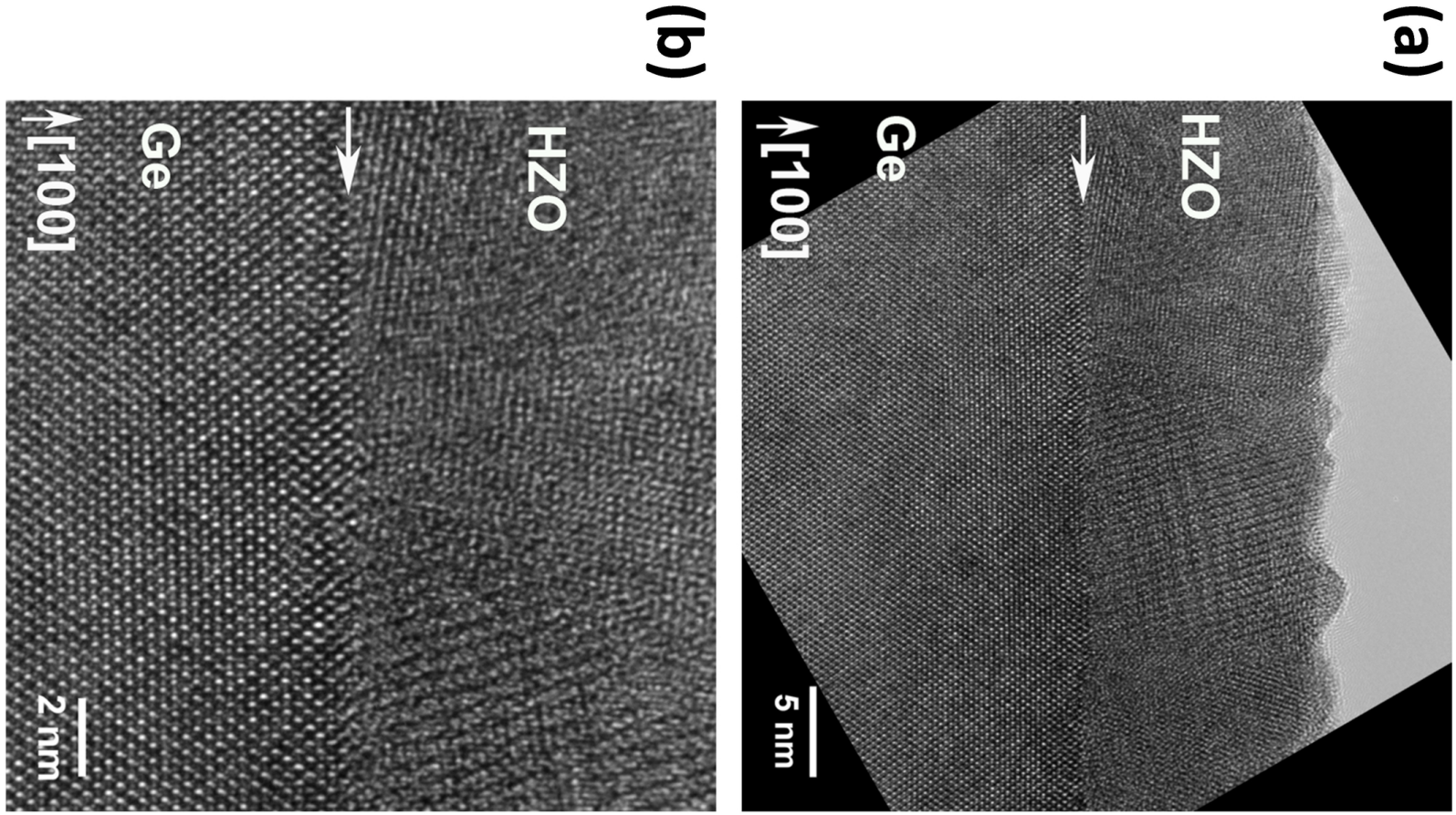

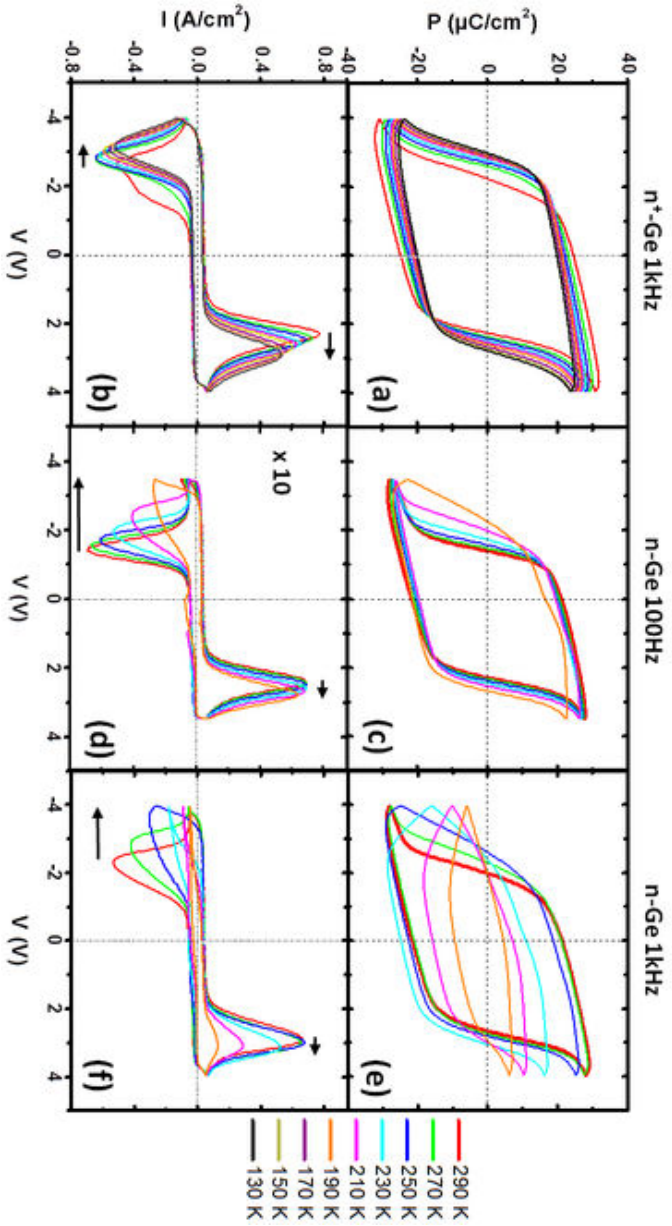

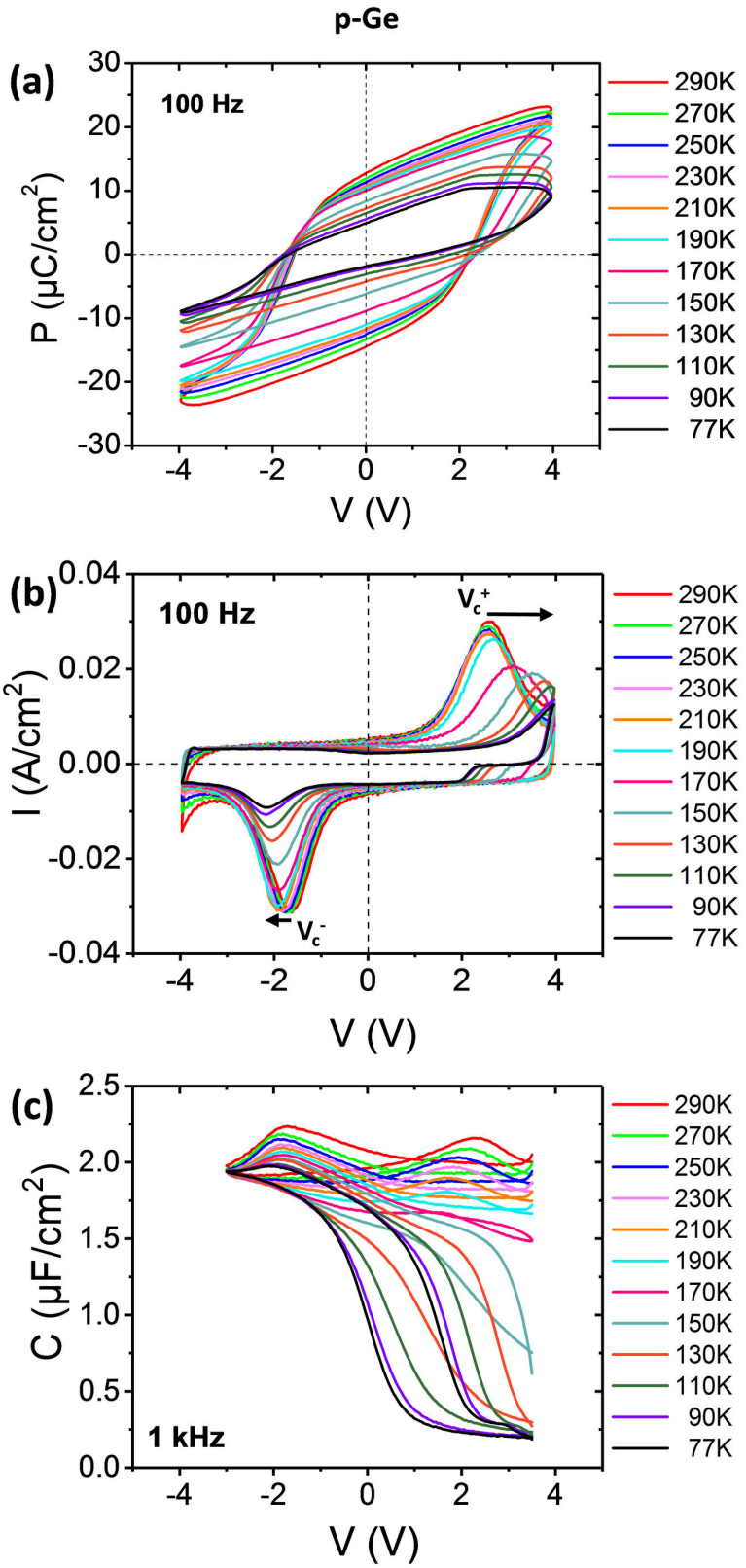

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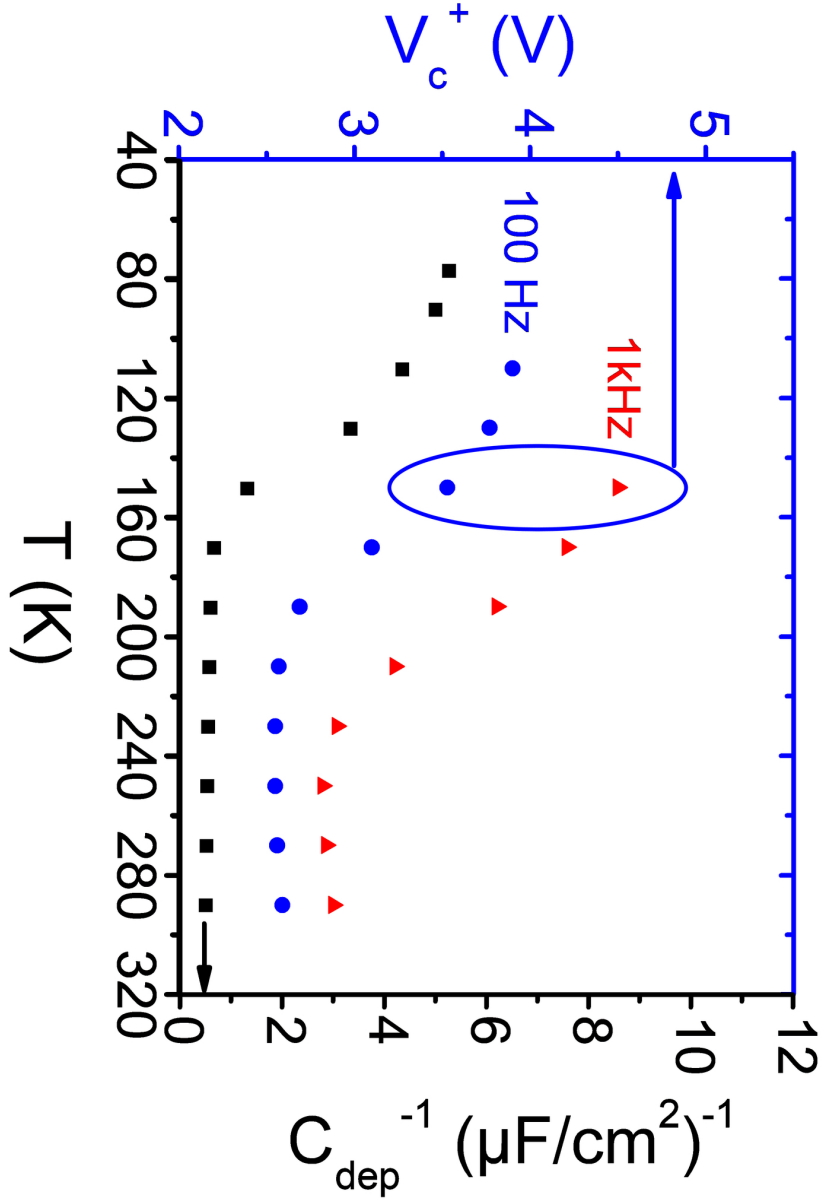
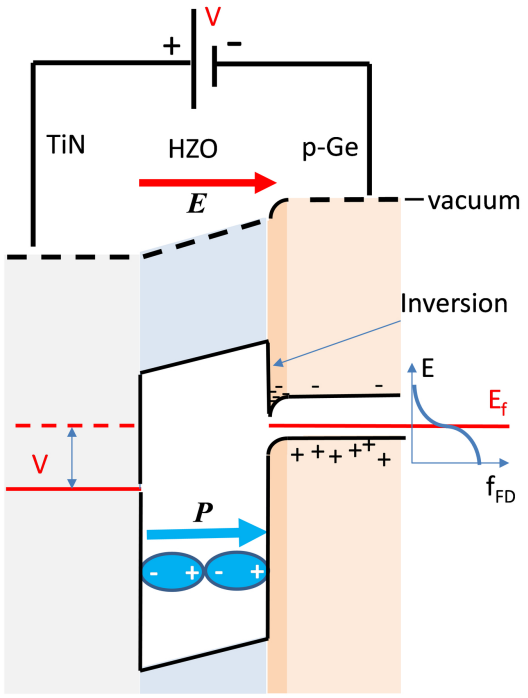
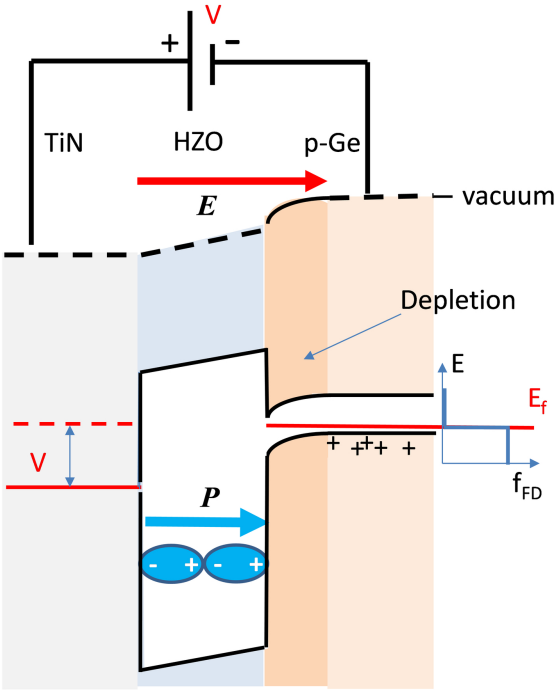


(a) High temperature



(b) Low temperature



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