Design and Verification of 4 X 4 Wallace Tree Multiplier

Mohd Esa and Konasagar Achyut

Abstract. The aim of this paper is to study 4x4 Wallace tree multiplier. In high performance processing units & computing systems, multiplication of two binary numbers is primitive and most frequently used arithmetic operation. Wallace tree multiplier is area efficient & high speed multiplier. This paper presents design and verification of Wallace tree multiplier. Design is carried out in Xilinx ISE Design Suite 14.7 using Verilog HDL and verification is carried out in Questa Sim 10.4e using System Verilog HVL environment.

Keywords: Wallace Multiplier, HVL, HDL, RTL.

1 Introduction

Technology is growing rapidly and being developed since years, today human is totally dependent on technology over the entire range of things. All these things which are manufactured and brought to market has its own disadvantages & advantages with its scaled reliability, product designers keep the three metaphoric terms constantly in the vision and improve them year by year: Area, Speed and Power. This paper is the entirety of the multiplication done in digital electronics by means of binary system.

Binary arithmetic consists of subtraction, multiplication, addition & division. This paper is all about designing and verifying the functionality of Wallace tree multiplier. A binary number system has only 1 and 0 as digits. Multipliers play a necessary role in today's digital signal processing and various other applications. Wallace tree multiplier is structured hardware implementation of digital circuit which multiplies two integers as formulated by Chris Wallace, an Australian computer scientist in 1964. The prominent components used in this multiplier are:

(a) Full Adder:

Combinational logic is a concept in which two or more input states describe one or more output states. Design of a full adder [1], First, we must create a truth table showing the various input and output values for all the possible cases. Fig.1 shows the logical diagram having three inputs A, B, C_{in} and two outputs, Sum and C_{out}. There are eight possible cases for three inputs, and for each case the desired output values are listed. For example the case A = T, B = F and C_{in} = T. The full adder must add these three bits to produce a sum of F and a carry (C_{out}) of T [2]. Two half adders and

OR gate can be combined to make a full adder as shown in fig.1. Table 1 shows that there are four cases where sum is to be a T and four cases where sum is F [3].

Table 1. Full adder truth table

Input			Output	
A	***B***	C_{in}	***Sum***	C_{out}
F	F	F	F	F
F	T	F	T	F
T	F	F	T	F
T	T	F	F	T
F	F	T	T	F
F	T	T	F	T
T	F	T	F	T
T	T	T	T	T

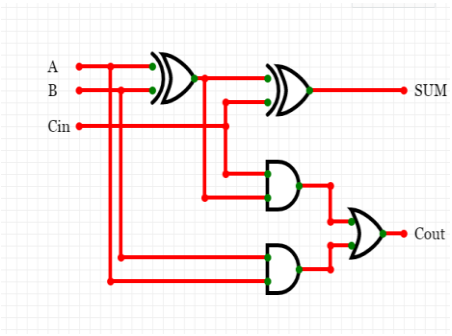


Fig. 1. Logic diagram of full adder

(b) Half Adder:

Full adder operates on three inputs to produce a sum and a carry output. In some cases, a circuit is needed that will perform addition of only two input bits, to produce a sum and a carry output.

Table 2. Half adder truth table

Input		Output	
A	***B***	***Sum***	C_{out}
F	F	F	F
T	T	F	T
T	F	T	F
F	T	T	F

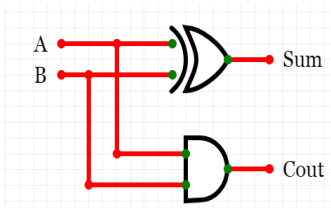


Fig. 2. Logic diagram of half adder

An example would be the addition of LSB position of two binary numbers where there is no carry input to be added. A special logic circuit can be designed to take two input bits, A & B, and to produce sum and carry (C_{out}) outputs. This circuit is called half adder whose task is similar to that of a full adder except that it functions on only two bits. The simplest half adder design includes an XOR gate for sum and an AND gate for C_{out}. The input variables of half adder are called augend and addend bits.

With the emergence of Large Scale Integration, engineers are able to put thousands of gates on a single chip. At this instance design process started getting very difficult and engineers sensed the need to automate the process. Electronic Design Automation (EDA) techniques began to emerge. Because of the complexity of the circuits it wasn't possible to verify these circuits on breadboard and analyse it

accurately. Thus HDLs came into existence [4]. The Verilog Hardware description Language (HDL) became the most extensively used language for hardware description. Verification is intended to be fundamentally different activity than design. This splitting has led to development of narrow focused language for verification.

2 Wallace Tree Multiplier

The initial step is the formation of partial products by multiplying each bit from the multiplier to same bit position of multiplicand. Secondly, groups of three adjacent rows are collected. Each group of three rows is reduced by using half adders and full adders.

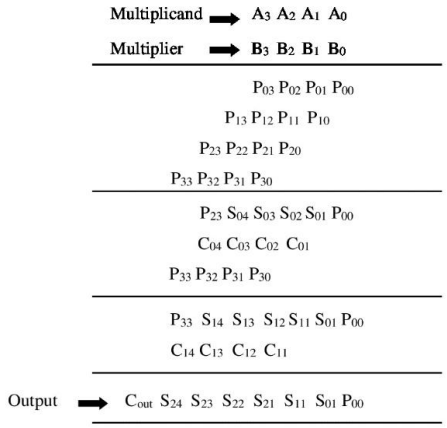


Fig. 3. Operation of 4x4 Wallace Tree Multiplier

Half adders are used in each column where there are two bits whereas full adders are used in each column where there are three bits, any single bit in column is passed to next stage in the same column without any operation. This reduction procedure is repeated in each successive stage until only two rows remain. In the final stage, the remaining two rows are added. After completing all the three stages we get 8 bit of output as shown in fig.5.

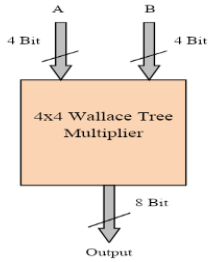


Fig.4. Block diagram of Wallace Tree Multiplier

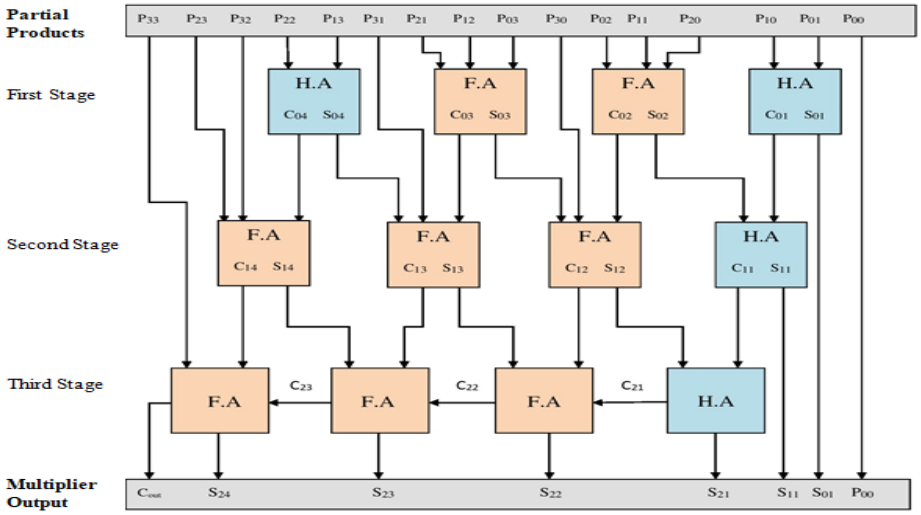


Fig. 5. Wallace Tree Multiplier using full and half adders

3 Design and Verification Results

Simulation provides an efficient way to analyze the design which can be easily rectified by means of EDA tools. Fig.6 shows simulation waveforms of inputs as well as output using Verilog HDL & Fig.7 shows RTL schematic of Wallace Multiplier.

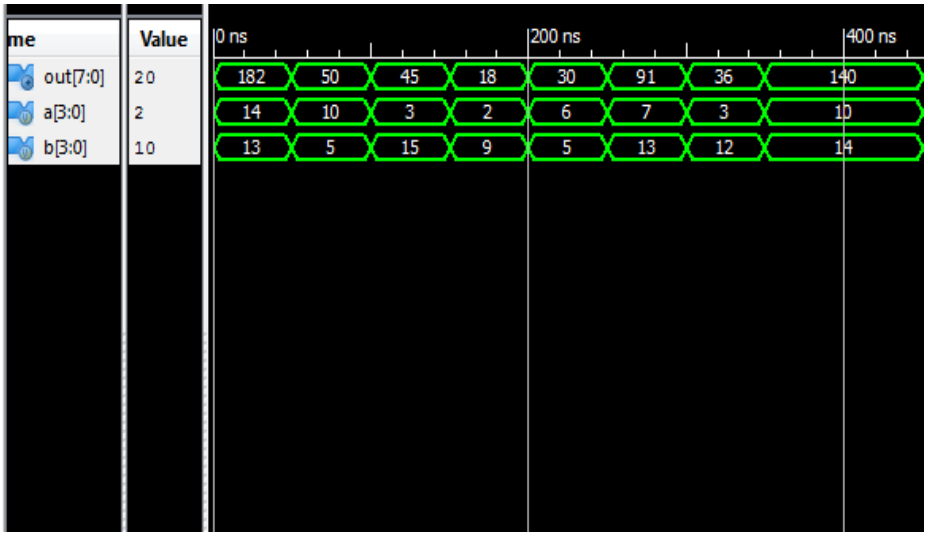


Fig. 6. Simulation output of 4x4 Wallace Tree Multiplier (Using Verilog)

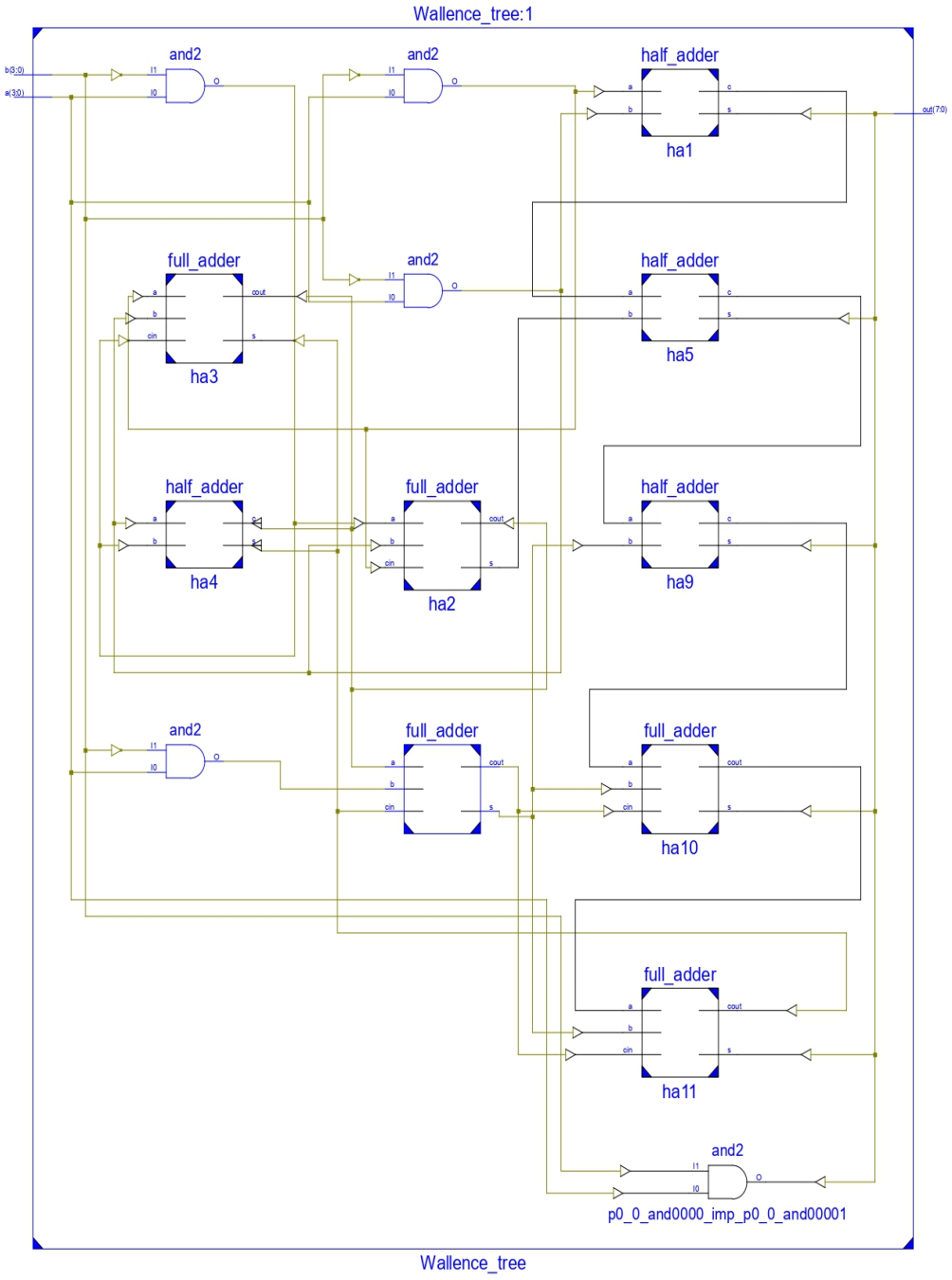


Fig.7. RTL schematic of Wallace Tree Multiplier.

Verification is carried out using object oriented programming concept in system verilog hardware verification language and design is justified error free using functional coverage. Fig. 9 shows the 100% functional coverage report for different random inputs.

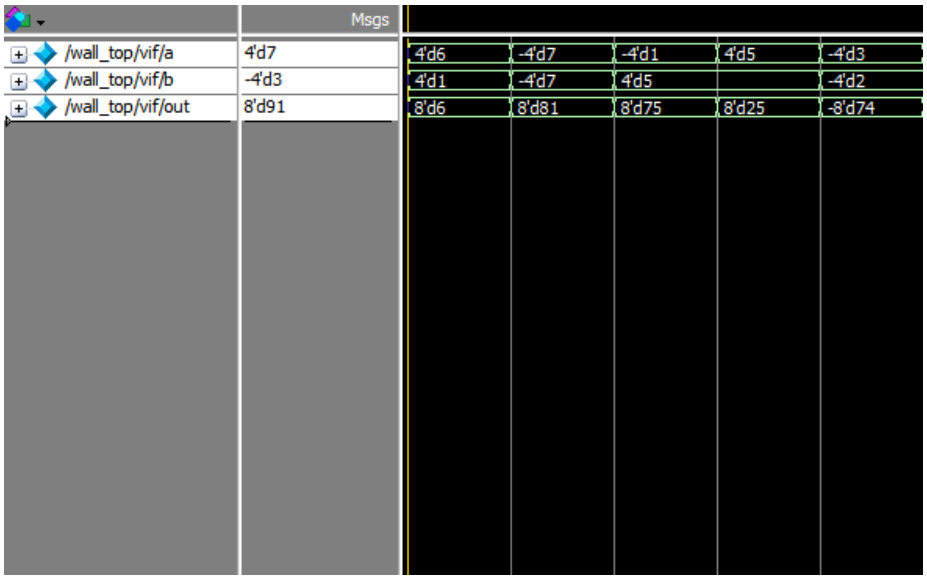
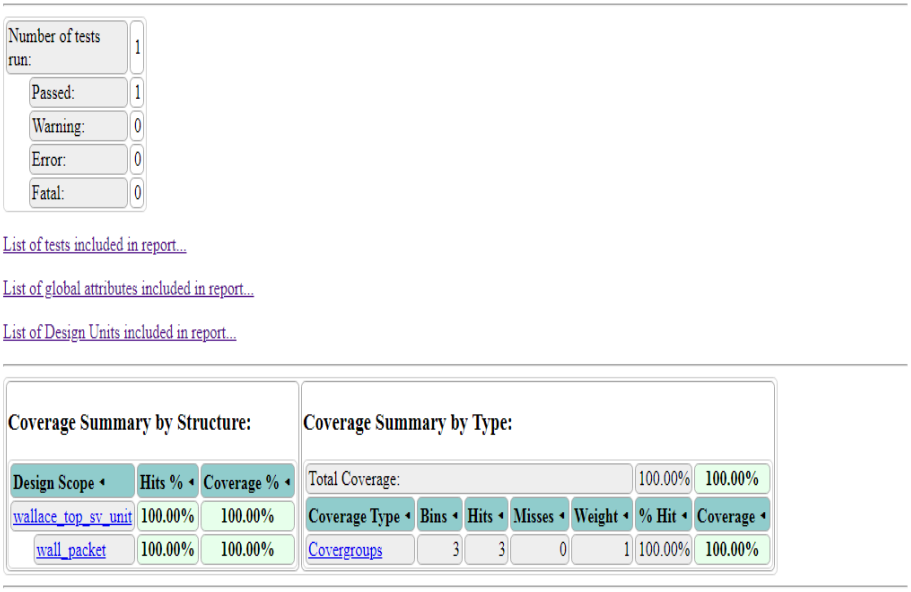


Fig.8. Verification of Wallace Tree Multiplier by generating random inputs



Number of tests run:	1
Passed:	1
Warning:	0
Error:	0
Fatal:	0

List of tests included in report...

List of global attributes included in report...

List of Design Units included in report...

Coverage Summary by Structure:

Design Scope	Hits %	Coverage %
wallace_top_sv_unit	100.00%	100.00%
wall_packet	100.00%	100.00%

Coverage Summary by Type:

Total Coverage:					100.00%	100.00%
Coverage Type	**Bins**	**Hits**	**Misses**	**Weight**	**% Hit**	**Coverage**
Covergroups	3	3	0	1	100.00%	100.00%

Fig.9. Coverage report of Wallace Tree Multiplier using SV environment

4 Conclusion

In this paper we have studied about multiplication of two 4-bit binary numbers using Wallace Tree Multiplier. Wallace Tree Multiplier is designed by means of HDL. After successful simulation of the required design it has been verified for its functionality using HVL with functional coverage. From Fig.6 and Fig.8 it concludes that design is meeting the expected result covering all the verification scenarios explicitly.

References

1. Ronald J. Tocci, Neal S. Widmer, Gregory L. Moss, "Digital Systems, Principles & Applications," Pearson Education, Inc., 2007, pp. 239-240.
2. Ms. Asha K A, Mr. Kunjan D. Shinde, "Analysis, Design and Implementation of Full adder for Systolic Array Based Architectures – A VLSI Based Approach," IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 6, Issue 3, Ver.1(May.-Jun. 2016), pp. 74.
3. Shital Baghel, Pranay Kumar Rahi, Nishant Yadav, "CMOS Half Adder Design & Simulation Using Different Foundry," IJISET – International Journal of Innovative Science, Engineering & Technology, Vol. 2 Issue 3, March 2015, pp. 195.
4. Samir Palnitkar, "Verilog HDL, A Guide to Digital Design and Synthesis, IEEE 1364-2001 Compliant," Pearson India Education Services Pvt. Ltd., pp. 45-46.

Biographies

Mohd Esa completed M.E. (Power Electronics systems) from Muffakham Jah College of Engineering and Technology, Banjarahills, Hyderabad in 2018. He received his B.E degree from Matrusri Engineering College, Hyderabad in 2015. He was awarded gold medal twice for standing first in B.E. III/IV and B.E. IV/IV from Matrusri Engineering College, Sayeedabad, Hyderabad. He has published 10 research papers in various journals and conferences.His research of interests includes Multi level inverters and electric drives. He is trained VLSI Design Engineer.

Konasagar Achyut is trained in VLSI Front End RTL Design and Verification, and he received his Bachelor of Technology degree in 2018, Electronics & Computer Engineering from J.B. Institute of Engineering & Technology, Hyderabad. Being devoted towards science and technology, he is an active member in Institute of Electrical and Electronics Engineering (IEEE), United States and also in International Association of Engineers (IAENG), Hong Kong. His area of interest lies in IP verification, chip planning and FPGA designing.