# Comparison of Two Methods for Realization of Multiplierless Elliptic IIR Filters

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# ABSTRACT

Two methods for multiplierless elliptic IIR filter implementation are discussed: cascade realization and parallel connection of two allpass networks. Elliptic IIR filters are selected because they fulfill the requirements with lower order, and, usually, they require fewer coefficient multipliers. The comparison is made on the basis of adder costs, amplitude characteristics in pass and stop bands, coefficient wordlength and normalized product round-off noise variance at the output of the filter. This paper concentrates on the fixed-point arithmetic. The comparison between these different design algorithms for digital multiplierless IIR filters has not yet been reported. In this paper that comparison has been made for the first time. It is very important to point out that different designs have been compared under the same conditions.

## **1 INTRODUCTION**

By implementing the transfer function of the digital filter in hardware or software form, the finite wordlength effects have the significant influence in fulfilling the given filter specification. The realized frequency response is different from the desired frequency response because the poles and zeros are displaced from their original locations due to quantization. The total deviation of the frequency response caused by this effect and other effects should have a value which enables predetermined demands to be met.

The IIR filters considered in this paper are characterized by low complexity due to the implementation of constants using only binary shifts, adders and subtractors. Since an adder and a subtractor require very similar VLSI areas, for convenience, both will be referred to as 'adders'. The number of adders, expressed by the adder cost, is used to measure the complexity. Delays are costed at 0.2 adders. Every adder has two inputs, and can have any number of outputs. An emphasis on complexity reduction can be achieved by decreasing in number of shift and add operations what is particularly difficult because of the high sensitivity of IIR filter frequency responses to multiplier coefficients. There are a few algorithms for fulfilling these demands.

For IIR filters, the cascade realization due to its simplicity and good properties is very much used by filter designers. RAG-n (the n-Dimensional Reduced Adder Graph) algorithm proposes the application of a multiplier block for the implementation of a group of multipliers sharing the common input, which exploits the redundancy across the coefficients. For achieving this goal, outputs of one adder are used for realization of as many coefficients as possible [1], [2], [3], [4]. This approach is most efficiently deployed by using cascade structure.

It is well known that the structures based on parallel-of-twoallpass networks require only n multipliers for an odd nthorder filter. In [1] and [2], it has been shown that the multiplier block concept is inapplicable for the wave digital filters and other realizations based on allpass sections. Consequently, the conclusion has been drawn that these structures are not suitable for implementation without multipliers.

In [5] and [6], it has been shown that the filter structures consisting of two allpass networks in parallel may have a small number of adders if the transfer function is derived by the bilinear transformation from an elliptic minimal Q-factors (EMQF) analog prototype. This way, (n+1)/2 multiplication constants can be implemented without quantization. The quantization of the remaining (n-1)/2 less sensitive constants is performed using the phase-tolerance scheme and phase-sensitivity functions [6]. This class of filters has all multiplication constants implemented with a small number of shifters and adders.

The goal of this paper is to compare two approaches for multiplierless IIR filter design: (1) the cascade realization and multiplier blocks [1], [2] [3], [4], and (2) EMQF filter realized as a parallel connection of two allpass branches [5], [6]. The comparisons are made on the basis of adder costs, amplitude characteristics in pass and stop bands, coefficient wordlength and normalized product round-off noise variance at the filter output. The dynamic range scaling is performed using the L<sub>2</sub>-norm rule to prevent overflows at the internal nodes [7], [8], [9]. To compute the product round-off noise variance at the output of the scaled filter structure the tool in MATLAB has been developed.

# 2 EXAMPLES SPECIFICATIONS AND REALIZATION STRUCTURES

The required digital filter specifications are usually given with boundary frequencies for the passband Fp and Fa for the stopband, passband ripple Ap, and minimal stopband attenuation Aa expressed in decibels. A filter order n is an important parameter, as well. In spite of EMQF algorithm which requires n to be an odd number, RAG-n algorithm has no limits in this sense.

The filter specifications used for the comparison are:

- *Example 1 Fp*=0.135, *Fa*=0.2, *Ap*=0.2 dB, *Aa*=30 dB
  - 1.a classical cascade realization with multiplier blocks
  - 1.b EMQF, cascade realization with multiplier blocks

1.c EMQF, parallel connection of two allpass networks

Example 2 Halfband filter: Aa=28 dB, Fa=0.28

2.a EMQF, cascade realization with multiplier blocks 2.b EMQF, parallel connection of two allpass networks

*Example 3* Halfband filter: Aa=46 dB, Fa=0.28

3.a EMQF, cascade realization with multiplier blocks

3.b EMQF, parallel connection of two allpass networks,

coefficient word length 8 bits

3.c EMQF, parallel connection of two allpass networks, coefficient wordlength 12 bits

The specifications of example 1 are met with the 4th order elliptic filter and the 5th order EMQF filter. Figure 1.a illustrates the

replacing the five multiplier coefficients of each second-order transposed direct form I filter with multiplier block for the 4th order filter from example 1.a. Producing of multiplier coefficient sets in multiplier blocks 1 and 2 is shown in Figures 1.b and 1.c.

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The flow diagram for filter from example 1.c is presented in Figure 2.The specification of example 2 require the 5th order EMQF filter , while for example 3 the 9th order EMQF filter is needed.



### **3 RESULTS**

The results for example 1 are presented in Figure 3, Figure 4 and in first two rows of Table 1. The classical cascade connection of first and second order sections enables the given specification to be met with a 4th-order filter, whereas for the EMQF algorithm a 5th-order filter is required. It is shown in Figure 4 that the attenuation characteristic obtained by EMQF design method has smaller ripples in passband than by using a classical design method for a cascade connection of first and second order sections, but it increases an adder cost from 17.6 to 26. Passband ripples may be additionally decreased using parallel connection of two allpass networks for EMQF filters. This leads to the following goals: almost three times smaller normalized product round-off noise variance at the filter output and also smaller EMQF adder cost, 21 adders. In all three cases multiplier coefficient wordlength is 8 bits.



*Figure 3 Example 1- Amplitude characteristics* 



Figure 4 Example 1- Amplitude characteristics in the passband

The halfband elliptic filter is a special case of an IIR filter and may be derived from the analog EMQF prototype [5]. Having that in mind through examples 2 and 3 we compare two different approaches to realization of a halfband filter.

Figure 5 displays two magnitude characteristics of the 5thorder halfband filters, with coefficient wordlength of 8 bits, example 2. Obviously, the obtained characteristics are almost identical for both discussed realizations.



Figure 5 Example 2 - Amplitude characteristics

It is demonstrated through example 3 that the sensitivity to multiplication coefficient of 9th order halfband filter in the stopband is higher for the parallel connection of two allpass networks in comparison with the cascade connection of first and second order sections if the coefficient wordlength is 8 bits. Difference between behaviors in the stopband may be reduced increasing the wordlength from 8 to 12 bits for the critical design method what causes the adder cost increasing from 22 to 25 adders. The attenuation curves for this example are shown in Figure 6.



Figure 6 Example 3 - Amplitude characteristics

It is evident from Table 1 that adder cost and normalized product round-off noise variance at the output of the halfband filter are far better if the parallel connection of two allpass networks is applied even if the wordlength has been increased.

## **4 CONCLUSION**

In this paper we carried out a comparison of two design methods for multiplierless elliptic IIR filters. From Figures 3, 4, 5, 6 and Table 1 the following conclusions can be drawn:

-For lower filter order predetermined requirements could be met with smaller adder cost using cascade realization, but the passband ripples of amplitude characteristics are increased.

-EMQF algorithm decreases efficiently passband ripples for cascade realization.

-Better amplitude characteristics in the stopband are achieved using cascade realization. For the same amplitude characteristics in the stopband using parallel connection of two allpass networks an increase in the coefficient wordlength is required.

-For halfband filters parallel connection of two allpass networks realization method enables a substantial reduction in the adder cost.

-Regarding to the product round-off noise variance at the output of the filter parallel connection of two allpass networks is superior.

We paid the most attention to adder costs, amplitude characteristics in pass and stop bands, coefficient word-length and normalized product round-off noise variance at the output of the filter. There are, however, many other parameters that may be taken into account in choosing a filter structure.

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Example	Filter order n	adder cost	coefficient word length	normalized product round-off noise variance
1.a.	4	17.6	8 bits	23.87
1.b.	5	26	8 bits	21.35
1.c.	5	21	8 bits	6.91
2.a.	5	17.8	8 bits	14.08
2.b.	5	11.6	8 bits	1.54
3.a.	9	34.4	8 bits	22.11
3.b.	9	22	8 bits	4.61
3.c.	9	25	12 bits	4.61

Table 1