DSP ARCHITECTURE FOR REAL TIME DIGITAL VIDEO CONVERTER

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ABSTRACT

In this paper we propose the architecture of a digital video standard converter based on the use of DSP processors (AD 21060 SHARC) completely programmable and able to perform real time elaboration. The purpose is to verify experimentally the possibility to implement very complex moto compensation algorithm (for example in real time digital television standard converter), on a multiprocessing DSP system. In this way is possible to make very versatile digital elaborators (because programmable) and at low cost. This system find out applications in:
- Digital Video Broadcasting (DVB) [1-2, 4-6]
- Artificial intelligence
- Robotics and military applications in motion detection system.

1. DIGITAL VIDEO PROCESSOR

The digital video processor executes the conversion on the odd fields sequence and even fields sequence separately. We regards only to the odd fields but the processing is the same for the even one. The algorithms needed for television standard conversion are: temporal interpolation and vertical interpolation [1,2]. The first is used to change the field frequency (50 Hz-60 Hz) by estimation of displacement vectors (or motion vectors) of blocks of pixels in the images (motion compensation), the second is used to change the number of lines in the fields (theorem of Nyquist). The moto compensation is carried out by three groups of DSPs [3]:
1) Estimator of displacement vectors
2) mapper
3) background field generator.
The first group is composed by three DSP that calculate the displacement vectors by two fields, one from the original sequence and the other one from the interpolation in the previous step. The second group is just one DSP that take in input the displacement vectors while the estimator is carrying out them; and contemporary executes the mapping operation of the block. The third group is represented by one DSP that generates a background field averaging the intensity pixel to pixel of the two fields to be motion compensated. This elaboration, simultaneously executed with the previous one, is needed to fill the empty areas caused by the overlapping blocks. The vertical interpolation is performed by another group of three DSPs which use FIR filters to interpolate the lines to determine the new ones. The motion compensation algorithm and the vertical interpolation are carried out in pipeline, in this way we are able to execute them in the same temporal

window represented by the time distance between two fields. As a consequence the real time processing is kept.
The 4 dual-ported memories have been used because two of them are needed to implement a interframe algorithm such as motion compensation, one is needed to store the interpolated field, and the last one must contain the copy of the interpolated field in order to be used by the vertical interpolator without causing bus conflict. In figure 1 it is shown the digital video processor.

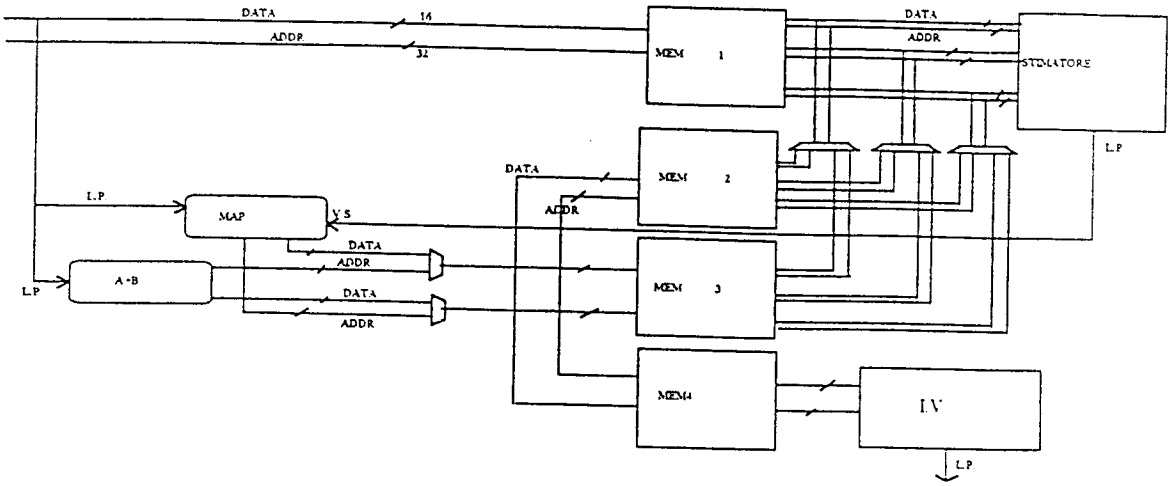


Fig 1 Digital video processor

2. ESTIMATOR OF DISPLACEMENT VECTORS

The estimator is composed of 3 DSP's one of which is always the master (M), while the remaining two carry out block-matching calculations. Fig 2 represents the multiprocessing configuration that has been adopted. In order to explain the architecture selection one must take into account the operations to be carried out in accordance with Bierling algorithm [3] slightly modified.

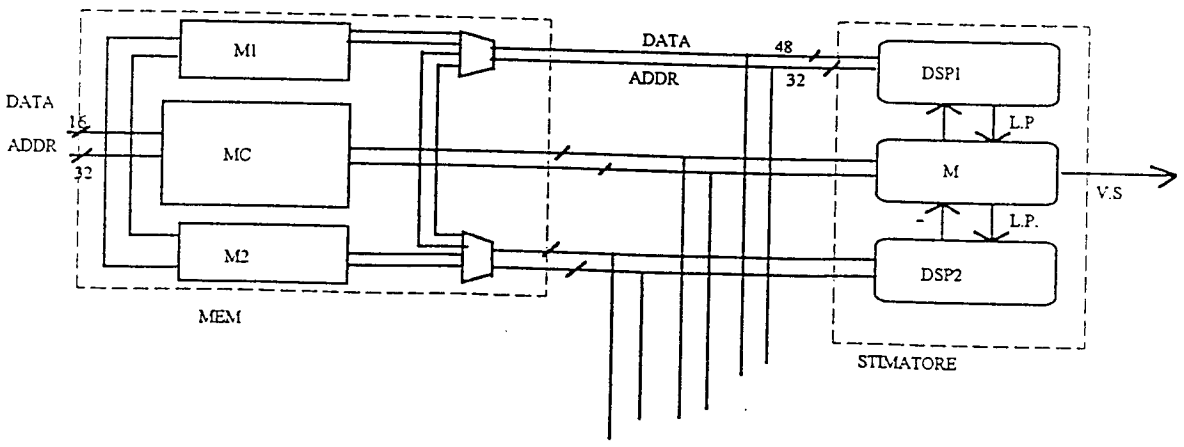


Fig. 2 - Estimator of displacement vectors

This applies a motion-compensation based on hierarchical block matching (HBMA), where the size of blocks and search area varies at different hierarchy levels. Blocks of large size are used at the first level to estimate wide displacements, while blocks of smaller size are used at the second level to refine the previous estimate. Basic parameters that have been adopted are listed below

Level of parameters	1	2
Max displacement (d1)	7	3
Measurement window (Wl)	32	8
Block size (S1)	16	8
Pixel distance (Ul)	8	2

MAD has been used as the block matching criterion, to determine the correspondence between the reference block and the block in the search area. At the first level a comparison is made among 25 positions, at the second level among 16 positions.
On the basis of experimental data obtained by measuring the clock cycles needed to execute MAD and to compare them to determine the displacement vector it is found that the estimator need 2 processors to reach the necessary calculation power. A processing time of 32 ms has been estimated experimentally.
Also in the NTSC case a processing time of 27 ms has been estimated in the worst conditions. Therefore our location is in the NTSC 33.4 ms time window. Data arrangement in memory is another important aspect.
It is noted, in fact7 that the measurement windows used are larger than the blocks in which the image is partitioned therefore they are partly overlapped, as well as search areas are. As a consequence, there are data in common between two continuous blocks which are processed by the two DSP's. Therefore we have partitioned the pixels in three groups, i e the ones used by the first processor, by the second processor and by both. See fig. 2. In this way the two DSP's can load simultaneously their private data, while common data are loaded simultaneously into the two DSP's through a "broadcast" transfer by the master. Therefore the DMA's in each processor can transfer data to the computational core in a transparent way.

3. VERTICAL INTERPOLATOR

The last group of 3 DSP's carries out the vertical interpolation to change the number of lines in the fields. As already noted, this operation is in pipeline with the motion compensation and does not generate any bus conflict thanks to M4 private memory. Six FIR filters are used by the algorithm for the passage NTSC - PAL and 5 FIR filters for the reverse. The worst case from the computational point of view is the determination of the PAL frame which required 0.144 s. Fig. 3 shows the vertical interpolator.

4. CONCLUSIONS

The experiments carried out on the EZ-LAB deve]opment board to determine the routine execution times have confirmed that the operations described are carried out within the established time window. Fig 4 shows the graph of the simulations.

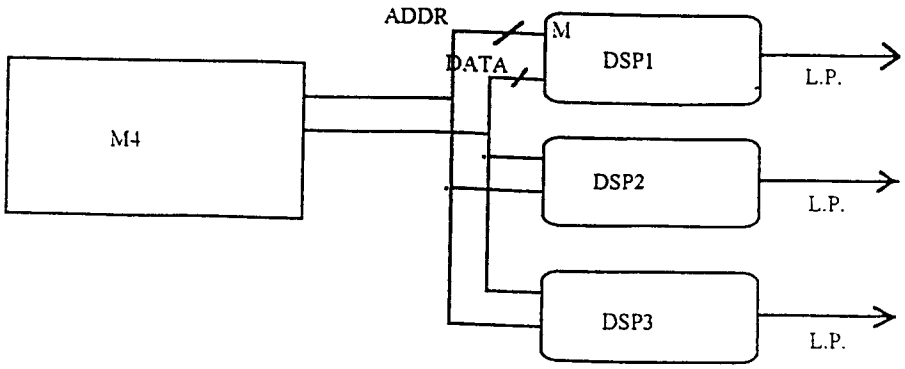


Fig. 3 vertical interpolator

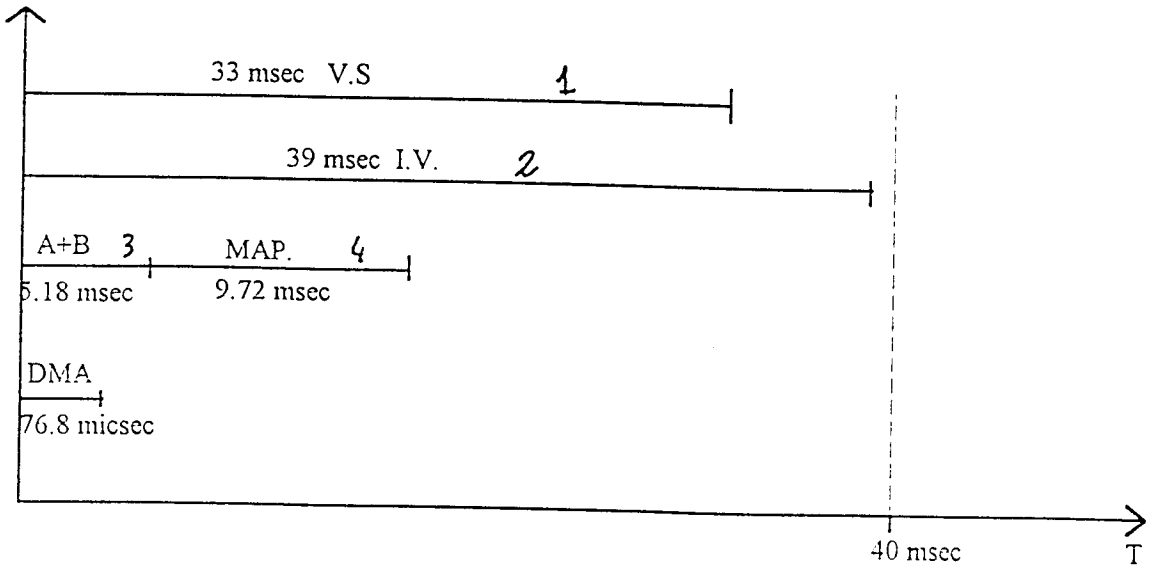


Fig 4 graph of the simulations

1) time needed to estimate displacement vectors
2) time needed to execute the vertical interpolation
3) time needed to create the background field
4) time needed to execute the mapping

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