Through Silicon Vias in MEMS packaging, a review

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***Abstract*—Trough Silicon Via (TSV) is a key enabling technology to achieve the integration of various dies by exploiting the third dimension. This allow the integration of heterogeneous chips in a single package (2.5D integration) or to achieve higher integration densities of transistors (3D integration). These vertical interconnections are widely used for both IC and MEMS devices. This paper reviews TSV technology focusing on their implementation in MEMS sensors with a broad overview on the various fabrication approaches and their constraints in terms of process compatibility. A case study of an inertial MEMS sensor will then be presented.**

***Keywords*—Trough Silicon Via, TSV, MEMS, Sensors, Integration, Zero-level packaging**

I. Introduction

3D integration is a key technology for the future of microfabrication that already resulted in great improvements in performance and miniaturization in the field of memory, imaging, computing and sensing. This technology has been listed in the road maps of both More Moore and More than Moore approaches for which a series of design tools are currently under development.
It is well-known that the Moore's law [1] had accurately predicted the increment of the transistor density in integrated circuits (IC) for more than half a century. However, the transistor scaling started to slow down due to the extremely high difficulties in further reducing the channel length [2]. There are several challenges that need to be addressed. Firstly is the large of both R&D and manufacturing costs. As a result there are only three main player in the race to scale down the channel length. Alternatively, 3D integration increases the density of the transistor per die by adding several layers, interconnected by Thought Silicon Vias (TSVs). This approach is less costly and has resulted in interest among foundries that cannot afford the extremely high costs needed for the reduction of the channel length.
An orthogonal direction than the More Moore approach is described by the More than Moore trend. This term is used to indicate application driven devices where heterogeneous chips need to be integrated. The dies that could be integrated in a single system could include logic circuits, RF transceiver, MEMS sensors and batteries. The various chips could be integrated by a chip-to-chip, chip-to-wafer or wafer-to-wafer stacking process. In this case TSV technology is a key enabling technology widely exploited to realize electrical interconnections among dies.
In all these technologies, TSV is the key enabling technology that allows to electrically connect chips stacked in a 3D fashion [3]. Depending on the specific application, the requirements of the TSVs technology could drastically change.
Certain MEMS devices, such as gyrometers and accelerometers, need to be encapsulated at low pressure or vacuum level for optimum performance. Wafer-to-wafer zero-level packaging enabled by various bonding methods and can drastically improve the yield compared to vacuum packaging individual components. However, TSVs are then required for electrical connection of the active layer in the MEMS.
While the C-MOS fabrication process is standardized the MEMS fabrication process is typically tailored on the specific application and design and could differ depending on the specific laboratory equipment.
In this paper, the various approaches to realize TSVs in MEMS fabrication process will be presented and reviewed. The pros and cons of the different approaches will be discussed with a specific case study of an inertial sensor which is currently fabricated at SINTEF MinaLab. This paper is organized as follows, the second chapter presents an overview of the main fabrication processes and some exotic implementation aiming to go behind the state of art. In chapter III both the mechanical and electrical performances of TSVs are presented highlighting the main parasitic and failure contributions. Chapter IV instead presents the TSV solution that is currently developed within MUPIA project. The paper is than concluded by a brief summary in the Conclusion.

II. TVS in a nutshell

TSVs are structures that electrically connect the two sides of a wafer. The fabrication process of a TSV could be divided in three steps: silicon etching, oxidation and filling of the via. Depending on the specific implementation, a diffusion barrier, typically a titanium thin layer, could be deposited before the conductive filling of the TSVs.
The IC fabrication process is standardized and is commonly divided in two specific phases: definition of the transistor devices, i.e. First-End-Of-Line (FEOL) and definition of the electrical connections by metal lines, i.e. Back-End-Of-Line (BEOL). The via process is commonly identified depending on when it is realized with respect to the two main process phase.
The via-first sapproach identifies structures that are realized on a bare wafer which will be then processed in a conventional C-MOS line. The main concern of this approach is the compatibility of the structures with the high temperature process commonly used in the fabrication of transistors, up to $1000°C$. The via-middle approach refers to TSVs that are realized between the FEOL and the BEOL processes, while the via-last approach is to realize the TSVs as the last step (i.e. via-last) [4]. All these approaches need to be compatible

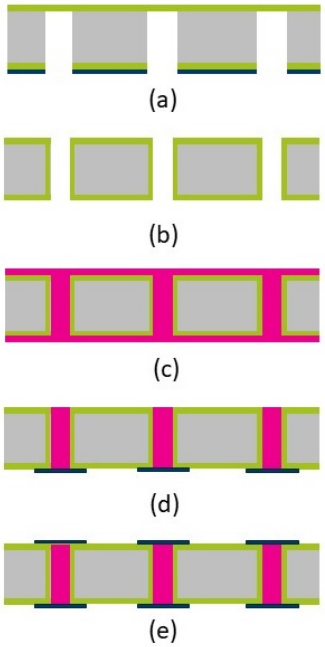

Fig. 1. Possible fabrication of a TSV, DRIE etch with a metal hard mask through the whole wafer (a), passivation (b) and filling (c) of the vias. The excess of conductive material is typically removed by CMP or wet processes ant then metal layers are deposited on both sides of the wafer, i.e. (d) and (e).

with the presence of the transistor avoiding high temperature processes. The via-last approach has a major advantage since it could be realized even on 3^{rd} parties devices but requires challenging etching techniques.

Similar considerations cannot be made for MEMS devices where the fabrication process is typically developed ad-hoc for the specific device. To integrate a TSV process in the fabrication process of a MEMS device it is fundamental to understand the key fabrication steps of the TSVs [3].

Fig. 1 presents a possible implementation of a TSV process. The initial step is the via etching, which is typically realized with an anisotropic dry process, i.e. Deep Reactive Ion Etching (DRIE). It is well known that the aspect ratio of the structure etched with a DRIE process is strongly related to both the single TSV design (i.e. circular or trench section) [5], [6], [7] and the layout design (i.e. fill factor) [5]. The aspect ratio constraints directly the minimum via size for a given silicon thickness. While for IC the main parameter is the minimum feature size, which should be comparable with the connections size, in MEMS design the main concern is the mechanical stability of the packaged device. With advanced fabrication processing exploiting the DRIE Bosch process, it has been demonstrated $500\ \mu m$-deep trenches with aspect ratio of 80 and circular vias with aspect ratio > 20 [7]. With such a technique is possible to realize through-trenches with a minimal feature size of $6\ \mu m$ and through-circular vias with diameters of $25\ \mu m$ in a $500\ \mu m$-thick wafer. Applications that require smaller via size need to use thinner wafers or process blind vias, which will be then opened by a wafer thinning process as presented in Fig. 3. The blind via and the through via approaches greatly affect the subsequent process performances.

The vias need to be electrically insulated to avoid electrical shorting to the bulk of the wafer. A dielectric layer needs to be deposited on the vertical walls of the vias and so a conformal process needs to be implemented. The growth of silicon oxide, by e.g. dry or wet oxidation, is a common solution for wafers that could sustain the high temperature process, i.e. via-first approach. In many applications the temperature of such a process could be an issue and low temperature solutions commonly used are chemical and physical vapor deposition (e.g. CVD and PVD) techniques. Those deposition tools need to be optimized to avoid any undesired accumulation of dielectric material that could create problems in the subsequent via filling. A possible solution is to use the Atomic Layer Deposition (ALD) which guarantees an uniform and conformal layer with a wide range of possible materials. However, the drawback is an extremely low deposition rate [8].

Similar fabrication steps are then used to fill the TSV with conductive materials. The main challenge of the filling step is to achieve a void free fill. Non uniform deposition could create uncompleted filling that could drastically increase the resistance of the connection, thus increasing the power consumption and the temperature of the device. The most commonly used techniques are polysilicon filling based on CVD techniques and metal electroplating[9]. The polysilicon layer deposited to fill the via needs to be doped to reduce the resistivity and the doping type needs to be tailored on the device in order to obtain suitable ohmic contacts and to avoid undesired p-n junctions.

Better performances in terms of resistance is obtained by metal filled TSV. The most common metal used is copper due to its compatibility with electroplating technology [10], [11]. This approach consists in first deposit a conductive and uniform seed layer which is subsequently used in the electroplating process as electrode. There are three approaches to fill the vias, conformal growth, bottom up growth [12] and a combination of the two. The deposition rate is defined by the current density during the deposition, the specific topography of the wafer and non-ideal conditions could induce a non-uniform growth of the metal layer. Additives that help to improve the electron mobility in the solution have been developed to improve and accelerate the filling of the metal layer especially for blind vias[11]. However, the Cu electroplating process is long and requires parameters adjustment that could impact the cost of the process. A different implementation uses CVD tungsten instead of electroplated copper. Tungsten has a lower conductivity with respect to copper, however has a thermal expansion similar to silicon improving the reliability of TSV [13], [14].

Great effort was invested in developing alternative techniques that further improve the filling process. An interesting approach investigates the possibility to fill the TSV directly with solder. This approach greatly reduces the costs of the final system since it merges two fabrication steps, i.e. TSV filling and deposition of solder bumps for system assembly. The filling of the vias is achieved with liquid solder that is forced into the vias by capillary effect [16], high pressure at wafer level [17] or at die level [18], and, for compete trough silicon vias only, by applying a depression on the back side of the wafer [19]. All those techniques show optimal void free filling within few seconds. During the final assembly however,

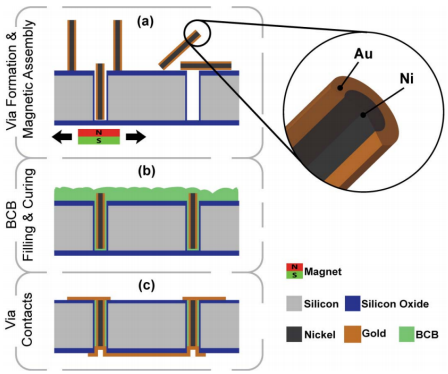

Fig. 2. Main fabrication steps of the Au coated Ni microwires asseembly process proposed by Bleiker et. al.. **Source** : ref [15] (©[2013] IEEE)

the liquid solder could leak out of the vias interrupting the electrical contacts [17].

Another promising approach consists in the filling of the TSV with highly conductive microwires [20]. The microwires are made with ferromagnetic material, e.g. nickel, which are driven into the TSVs by means of a magnetic field. The resistance of each wire could be decreased by a suitable coating, e.g. gold layer [15]. Once the wires have entered each via the wafer is coated by a polymer, which fills the vias and avoids the detaching of the wires. The wires are then electrically connected to the devices by means of suitable metal patterning.

As already mentioned, the TSV could be through the whole wafer but it could also be realized with a non-complete etch. There are two reasons to implement a blind TSV, first because the requirements in terms of aspect ratio and density of the application are too high or because the vias need to electrically connect to a specific layer already fabricated, i.e. via-last. In such a case there is another issue, the dielectric layer should be removed at the bottom of the vias. Such selective etching could be extremely challenging in case of a high aspect ratio vias [4]. A complex fabrication process to avoid it have already been proposed [21], however it greatly increase he complexity of the process and so the overall cost. A possible fabrication process used to realize high density and high aspect ratio TSV is presented in Fig. 3. The defining process for wafer thinning widely used to expose the TSV enabling electrical contact with suitable metal deposition is Chemical-Mechanical Polishing (CMP) [22]. This process is even compatible with the highly demanding fusion bonding process [23].

The design and fabrication process of the TSV needs also to be considered in the assembly of the system. In most applications the assembly is performed with solder bonding which is a standard process used in the packaging industry. Solder bonding has various advantages in the 3D stack of chips as it provides both the mechanical bonding and the electrical connections between wafers. Furthermore the liquid phase solder could improve the alignment of the dies due to the surface tension of the solder [24]. A similar approach commonly implemented in wafer MEMS fabrication process is thermo-compression bonding. This solution realizes a metal-to-metal bond without exploiting the liquid phase. For this reason it could be used also for low pressure packaging.

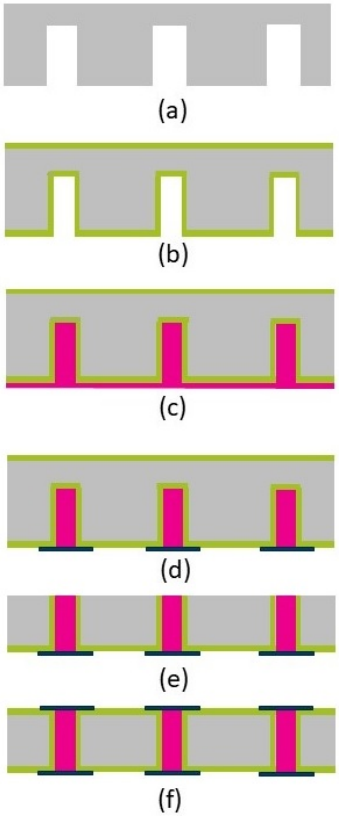

Fig. 3. Possible fabrication of a blind TSV, high aspect ratio silicon etching (a), the via are then passivated (b) and filled (c). The vias are then electrically connected with a metal layer (d). The wafer is then thinned to reveal the Vias by a CMP process (e). The vias are then completed with a second metal layer on the back side of the wafer (f).

III. TVSs PERFORMANCES

Each TSV introduces non-idealities in both the electrical and mechanical domain that could affect the device's performances. As already mentioned, the requirements of the TSVs could differ quite a lot depending on the specific application. Memory and logic circuits require, in general, high number of TSV with fine pitch and high bandwidth. While for a MEMS sensor, the requirements depends on the specific transduction mechanism implemented, but are in general less strict in terms of electrical performance. Ndip et. al. made an accurate high frequency electrical model for the TSV [25]. The model takes into account various parasitic contribution that affect the high frequency performance of the TSV, e.g. skin effect. Such a model is even too detailed for the majority of MEMS sensor and could be greatly simplified by considering specific implementations of the sensor.

For most sensor designs there are two contributions that have major impact on performance: the in-line resistance is split in two (i.e. R_{TSV}) and the parasitic capacitance toward ground (i.e. C_{par}) as shown in Fig. 4. The resistance is defined by the via design, i.e. area and length of the via, and the resistivity of the conductive material. The parasitic capacitance depends on the area around the TSV, the thickness of the insulating layer and dielectric constant related to the specific material, typically

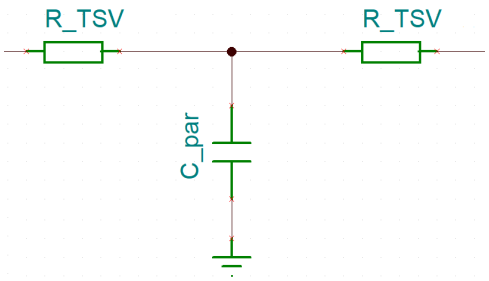

Fig. 4. Simplified equivalent circuit of a single TSV.

SiO_2. The resulting equivalent circuit represents a low pass filter which cut-off frequency depends on both values.

In literature various approaches to improve the performances of TSVs have been investigated. The in-line resistance could be improved by implementing a material with higher conductivity. The current implementation of high performances TSV exploits electroplated Cu, which has extremely good conductance. For this reason, most of the effort has been focused on the reduction of the parasitic capacitance, which is directly related to the geometry and material properties of the insulation layer. The oxide layer commonly implemented has a certain residual stress that limits the maximum thickness of the layer and hence most of the approaches tend to replace the insulation layer. A common solution, exploited also in the magnetic microwires approach, uses a polymer material, e.g. BCB, used also to bond the wires in position [20], [15]. A similar approach has also been implemented in electroplated TSV where the vias are patterned into the BCB polymer (which is also a photosensitive material). To further improve the capacitance value the TSV was then realized in a polymer well. This approach drastically increases the distance between the vias and the electrical ground reducing the parasitic capacitance. But having the TSVs in a common polymer well, however, could increase the cross-talk between different lines, which should be carefully evaluated. The BCB polymer used in those implementations has also been substituted by low-k polymer to further reduce the parasitic capacitance [21].

Polymer based TSV not only could improves the electrical performance of the TSV but it could also reduce the stress induced by temperature variation. TSV could introduce reliability issues related to the mechanics of such heterogeneous structure [26]. The difference in thermal expansion coefficient of the various layers could induce deformations that could jeopardize the mechanical and electrical performance of the device [27], [28], [29]. This result is even more critical in copper TSV, which has a thermal expansion 6-7 times higher than silicon. At high temperatures, the metallic vias expand more then the surrounding silicon, generating an high compressive stress that could plastically deform the metal generating metal extrusion up to 200 nm. This issue is commonly referred as copper pumping. The induced thermal stress could damage also the dielectric layer insulation the vias from the Si, e.g. layer delaminations [30] and cracks. The scalloping obtained by the bosh DRIE process could create stress accumulation points that induce those failures. Once the device is cool down to room temperature the metal TSV generates tensile stress that could also affect the performance of the neighboring device, e.g. by lowering the carrier mobility. All these failure mechanics

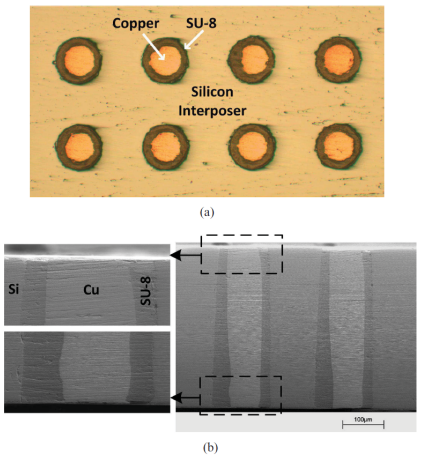

Fig. 5. TSV with electroplated Cu and polymer filling. **Source** : ref [15] (©[2015] IEEE)

induced by the stress could be reduced by optimizing the fabrication process [31] or by implementing low stiffness material, e.g. polymer, as dielectric layer as shown in Fig. 5. The induced thermal stress is extremely important in the reliability of devices packaged in a low pressure cavity since the thermally induced deformation could affect the ambient stability of the device.

IV. MUPIAs TSVs

MUPIA project addresses the topic of a manufacturing process for a high performance inertial MEMS [32]. There are various challenges that need to be addressed from the fabrication point of view. Among the various processes that are currently being developed and optimized in our laboratory the TSV is one of the most interesting. The device consists of a capacitive inertial sensor realized in the device layer of an SOI wafer, which must be packaged at high vacuum. Furthermore, the design requires high thermal stability that can only be achieved by a careful design.

As presented in the previous chapter, the design of the TSV is strongly dependent to the specific fabrication process implemented. The main step that needs to be define is the packaging. Among the different approaches to realize a low pressure cavity the wafer-to-wafer fusion bonding is the most convenient because it guarantees a good bonding quality without any interlayer which could induce undesired thermal stresses. The requirement of fusion bonding is however quite challenging, as it requires an extremely flat surface and, due to the high temperature involved, avoidance of any incompatible materials (e.g. metal layers). The fabrication process that has been defined within this project is depicted in Fig. 6. The fabrication process of the capping wafer starts with the etching of cavities needed for housing the mechanical part of the device. Then the TSVs are etched trough the capping wafer (Fig. 6(b)) with a DRIE process. The used DRIE tool implements a 3-stage process, which guarantee a superior aspect ratio of the etched structures as shown in the SEM image in Fig. 7. Furthermore, the design of a single TSV is not circular, as in many implementations, but rectangular with the longer side approximately 10 times longer than the shortest side. This design facilitates improving the etching performance without

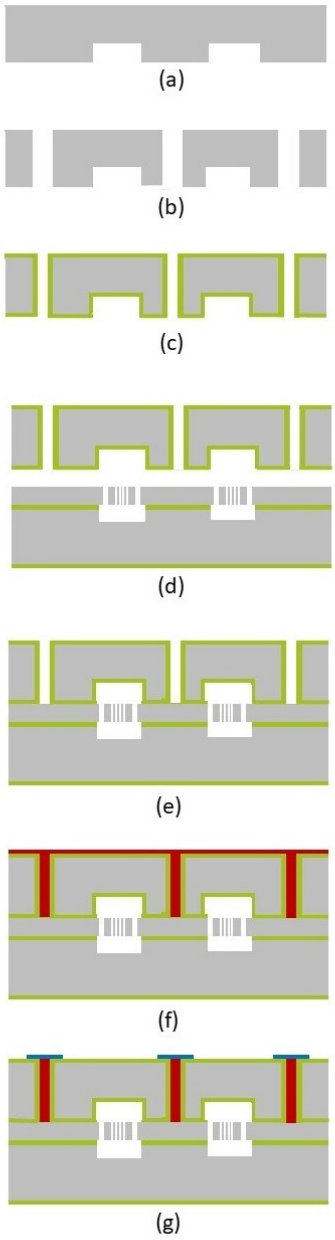

Fig. 6. Main process steps of the TSVs fabrication process within MUPIA project. Etch of the cavity housing the inertial sensor (a), Etch of the TSVs (b), oxidation of the wafer (c), fusion bonding of the capping wafer onto the device layer (d) and (e), Vias filling by polysilicon deposition (f) and then deposition and pattern of metal pads (g).

affecting the filling step with CVD tools [6].

The etching step is followed by the growth of the oxide layer. Since there are no other material than silicon and silicon oxide on the capping wafer, the wafer can sustain a high temperature process which guarantees a better and more conformal oxide. Growth of the oxide before the wafer bonding step has another advantage as it does not require to open the passivation at the bottom of such a deep TSV, which could be quite challenging process wise [4].

The capping wafer is then bonded onto the SOI wafer, which has had the native oxide removed. The blind vias are then filled by a high temperature, conformal polysilicon deposition process. The deposition of the polysilicon layer is split in two steps allowing to adjust the doping content to the desired value. The excess of polysilicon is then removed by a dry process leaving the TSVs electrically insulated. The process is then concluded by the deposition and patterning of the top metal layer, used for signal routing and contact pads.

To guarantee a minimal thermal impact most of the device is realized in Si, while the SiOx, used for passivation, was designed as symmetric as possible. Each TSV is designed to have approximately $50\ \Omega$ and $0.7\ pF$ when realized in $400\ \mu m$-thick wafer.

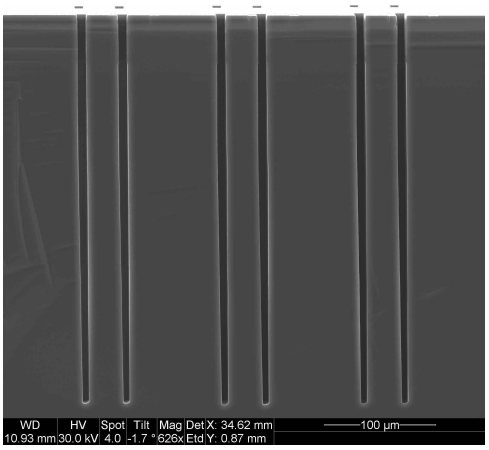

Fig. 7. SEM cross section of high aspect ratio $350\ \mu m$ deep TSVs in a test wafer

V. Conclusion

3D integration is a promising approach to achieve the higher and heterogeneous integration by exploiting the third dimension. However, wire bonding technology does not provide sufficient performances and needs to be substitute with a more suitable technology. Through silicon vias is a key enabling technology for advance packaging and 3D integration compatible with typical fabrication processes used in microfabbrication of both IC and MEMS devices. This paper reviews TSV technology focusing on their implementation in MEMS sensors with a broad overview on the various fabrication approaches and their constraints in terms of process compatibility. The electrical and mechanical performances of TSVs are presented highlighting possible countermeasure. The paper then presents a case study of TSV designed for an inertial MEMS sensor within SINTEF MiNaLab laboratories.

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References

[1] G. E. Moore, "Cramming more components onto integrated circuits," *Proceedings of the IEEE*, vol. 86, no. 1, pp. 82–85, Jan 1998.

[2] W. M. Arden, M. Brillouët, P. Cogez, M. Graef, B. Huizing, and R. Mahnkopf, "" more-than-moore " white paper," 2010.

[3] M. Motoyoshi, "Through-silicon via (tsv)," *Proceedings of the IEEE*, vol. 97, no. 1, pp. 43–48, Jan 2009.

[4] S. Van Huylenbroeck, M. Stucchi, Y. Li, J. Slabbekoorn, N. Tutunjyan, S. Sardo, N. Jourdan, L. Bogaerts, F. Beirnaert, G. Beyer, and E. Beyne, "Small pitch, high aspect ratio via-last tsv module," in *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*, May 2016, pp. 43–49.

[5] B. Wu, A. Kumar, and S. Pamarthy, "High aspect ratio silicon etch: A review," *Journal of Applied Physics*, vol. 108, pp. 051 101–051 101, 09 2010.

[6] Y. Tang, A. Sandoughsaz, and K. Najafi, "Ultra high aspect-ratio and thick deep silicon etching (udrie)," in *2017 IEEE 30th International Conference on Micro Electro Mechanical Systems (MEMS)*, Jan 2017, pp. 700–703.

[7] Y. Tang, A. Sandoughsaz, K. J. Owen, and K. Najafi, "Ultra deep reactive ion etching of high aspect-ratio and thick silicon using a ramped-parameter process," *Journal of Microelectromechanical Systems*, vol. 27, no. 4, pp. 686–697, Aug 2018.

[8] J. Vitiello and F. Piallat, "Alternative deposition solution for cost reduction of tsv integration," in *2018 IEEE 68th Electronic Components and Technology Conference (ECTC)*, May 2018, pp. 2163–2167.

[9] G. Parès, N. Bresson, S. Moreau, V. Lapras, D. Henry, and N. Sillon, "Effects of stress in polysilicon via - first tsv technology," in *2010 12th Electronics Packaging Technology Conference*, Dec 2010, pp. 333–337.

[10] K. Y. K. Tsui, S. K. Yau, V. C. K. Leung, P. Sun, and D. X. Q. Shi, "Parametric study of electroplating-based via-filling process for tsv applications," in *2009 International Conference on Electronic Packaging Technology High Density Packaging*, Aug 2009, pp. 23–27.

[11] H. L. H. Wu and S. W. R. Lee, "Study on copper plating solutions for fast filling of through silicon via (tsv) in 3d electronic packaging," in *2011 6th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT)*, Oct 2011, pp. 343–346.

[12] L. Ma, H. Ling, M. Li, J. Sun, X. Yu, and Y. Li, "Pure bottom-up filling process for efficient tsv metallization," in *2013 14th International Conference on Electronic Packaging Technology*, Aug 2013, pp. 356–359.

[13] G. Parès, N. Bresson, S. Minoret, V. Lapras, P. Brianceau, J. F. Lugand, R. Anciant, and N. Sillon, "Through silicon via technology using tungsten metallization," in *2011 IEEE International Conference on IC Design Technology*, May 2011, pp. 1–4.

[14] B. Mattis, L. Soirez, C. Bullock, D. Martini, S. Jensen, J. Levy, and A. Jones, "Front-side mid-level tungsten tsv integration for high-density 3d applications," in *2016 IEEE International 3D Systems Integration Conference (3DIC)*, Nov 2016, pp. 1–4.

[15] S. J. Bleiker, A. C. Fischer, U. Shah, N. Somjit, T. Haraldsson, N. Roxhed, J. Oberhammer, G. Stemme, and F. Niklaus, "High-aspect-ratio through silicon vias for high-frequency application fabricated by magnetic assembly of gold-coated nickel wires," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 5, no. 1, pp. 21–27, Jan 2015.

[16] J. Gu, X. Jiang, H. Yang, and X. Li, "Capillary effect based tsv filling method," in *2014 IEEE 27th International Conference on Micro Electro Mechanical Systems (MEMS)*, Jan 2014, pp. 1115–1118.

[17] Y. Ohara, Y. Inagaki, M. Matsui, and K. Asami, "A cost effective via last tsv technology using molten solder filling for automobile application," in *2017 IEEE 67th Electronic Components and Technology Conference (ECTC)*, May 2017, pp. 47–52.

[18] A. Horibe, K. Sueoka, T. Aoki, K. Toriyama, K. Okamoto, S. Kohara, H. Mori, and Y. Orii, "Through silicon via process for effective multi-wafer integration," in *2015 IEEE 65th Electronic Components and Technology Conference (ECTC)*, May 2015, pp. 1808–1812.

[19] Y. Ko, M. Kang, H. Kokawa, Y. S. Sato, S. Yoo, and C. Lee, "Advanced tsv filling method with sn alloy and its reliability," in *2011 IEEE International 3D Systems Integration Conference (3DIC), 2011 IEEE International*, Jan 2012, pp. 1–4.

[20] A. C. Fischer, N. Roxhed, T. Haraldsson, N. Heinig, G. Stemme, and F. Niklaus, "Fabrication of high aspect ratio through silicon vias (tsvs) by magnetic assembly of nickel wires," in *2011 IEEE 24th International Conference on Micro Electro Mechanical Systems*, Jan 2011, pp. 37–40.

[21] T. T. Bui, N. Watanabe, M. Aoyagi, and K. Kikuchi, "Twice-etched silicon approach for via-last through-silicon-via with a parylene-ht liner," in *2015 International 3D Systems Integration Conference (3DIC)*, Aug 2015, pp. TS8.6.1–TS8.6.4.

[22] M. Murugesan, T. Fukushima, J. C. Bea, H. Hashimoto, Y. Sato, K. W. Lee, and M. Koyanagi, "$wafer thinning for high - density three dimensional integration_1 2 - inch wafer - level 3d - lsi programat ginti$," in $25th$ *Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC 2014)*, May 2014, pp. 57–61.

[23] S. Skordas, D. C. L. Tulipe, K. Winstel, T. A. Vo, D. Priyadarshini, A. Upham, D. Song, A. Hubbard, R. Johnson, K. Cauffman, S. Kanakasabapathy, W. Lin, S. Knupp, M. Malley, M. G. Farooq, R. Hannon, D. Berger, and S. S. Iyer, "Wafer-scale oxide fusion bonding and wafer thinning development for 3d systems integration: Oxide fusion wafer bonding and wafer thinning development for tsv-last integration," in *2012 3rd IEEE International Workshop on Low Temperature Bonding for 3D Integration*, May 2012, pp. 203–208.

[24] Y. Martin, J. Nah, S. Kamlapurkar, S. Engelmann, and T. Barwicz, "Toward high-yield 3d self-alignment of flip-chip assemblies via solder surface tension," in *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*, May 2016, pp. 588–594.

[25] I. Ndip, B. Curran, K. Lobbicke, S. Guttowski, H. Reichl, K. Lang, and H. Henke, "High-frequency modeling of tsvs for 3-d chip integration and silicon interposers considering skin-effect, dielectric quasi-tem and slow-wave modes," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 1, no. 10, pp. 1627–1641, Oct 2011.

[26] I. De Wolf, K. Croes, and E. Beyne, "Expected failures in 3-d technology and related failure analysis challenges," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 8, no. 5, pp. 711–718, May 2018.

[27] Y. Chen, W. Su, P. Zhang, and X. l. Lin, "Failure analysis examination of the effect of thermal cycling on copper-filled tsv interposer reliability," in *2018 19th International Conference on Electronic Packaging Technology (ICEPT)*, Aug 2018, pp. 148–151.

[28] K. Croes, V. O. Cherman, Y. Li, L. Zhao, Y. Barbarin, J. De Messemaeker, Y. Civale, D. Velenis, M. Stucchi, T. Kauerauf, A. Redolfi, B. Dimcic, A. Ivankovic, G. Van der Plas, I. De Wolf, G. Beyer, B. Swinnen, Z. Tőkei, and E. Beyne, "Reliability concerns in copper tsv's: Methods and results," in *2012 19th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits*, July 2012, pp. 1–5.

[29] M. Song, L. Chen, and J. A. Szpunar, "Thermomechanical characteristics of copper through-silicon via structures," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 5, no. 2, pp. 225–231, Feb 2015.

[30] K. H. Lu, S. Ryu, Q. Zhao, X. Zhang, J. Im, R. Huang, and P. S. Ho, "Thermal stress induced delamination of through silicon vias in 3-d interconnects," in *2010 Proceedings 60th Electronic Components and Technology Conference (ECTC)*, June 2010, pp. 40–45.

[31] J. De Messemaeker, O. V. Pedreira, B. Vandevelde, H. Philipsen, I. De Wolf, E. Beyne, and K. Croes, "Impact of post-plating anneal and through-silicon via dimensions on cu pumping," in *2013 IEEE 63rd Electronic Components and Technology Conference*, May 2013, pp. 586–591.

[32] D. N. Wright. (2018) Mupia project websites. [Online]. Available: https://www.sintef.no/projectweb/mupia/