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An Efficient Implementation of MIL_STD_1553B Bus Controller Module Using Verilog HDL

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Abstract

The MIL_STD_1553 was developed in the 1970s as a serial communication bus for military applications by DoD (Department of Defense) USA and standardized in 1973. Later, the two various versions namely MIL_STD_1553A and MIL_STD_1553B were evolved, the later version MIL_STD_1553B is widely used in military applications because of its high reliability and flexibility. Modern avionic systems require high speed operation; however 1553B cannot reach the speed of the applications at high speed. To meet the real-world requirements, it is needed to improve the performance of the data bus, so this proposed work is focused on the implementation of military standard 1553B Bus Controller module using Verilog HDL and simulation is carried out by Xilinx ISE. Improvement in speed of operation due to reduction in delay is shown.

Keywords: *communication, Controller module, MIL_STD_1553B*

INTRODUCTION

In early decades, avionics systems integration was done using data bus standard with point to point wiring, but as the number of devices in the avionic systems increased as a part of modernization to perform the specific applications, complexity also increased and it became difficult to track the data. The MIL-STD-1553 got evolved to overcome these drawbacks. This protocol was developed at Wright Patterson Air Force Base since the 1970s by DoD USA specifically for military applications. It underwent number of revisions, became open for commercial applications and also became International standard and essential component for the International space programs, missiles, satellites and advanced commercial avionics applications. In 1975 version A of 1553 (1553A) was developed & later in 1978, version B (1553B) got evolved with Broadcast option. The primary goal of the 1553B was to provide flexibility without creating new designs for each new user. This was accomplished by specifying the electrical interfaces explicitly so that compatibility between designs by different manufacturers could be electrically interchangeable. Version B is highly reliable and flexible, therefore widely used in defense systems especially in military applications. The working and implantation of Bus Controller of MIL-STD-1553B is discussed here.

MIL_STD_1553B BUS

MIL-STD-1553B is a time division multiplexed, dual redundant, bidirectional, serial data bus with 1 megabits per sec (1Mbps) data rate. Manchester Bi-phase encoding technique is used here because of its high bit error reliability.

MIL-STD-1553B defines three types of terminal devices that are allowed on the bus:

- Bus Controller (BC)
- Remote Terminal (RT)
- Bus Monitor (BM)

The block diagram of the military standard 1553B BUS is shown in Fig. 1.

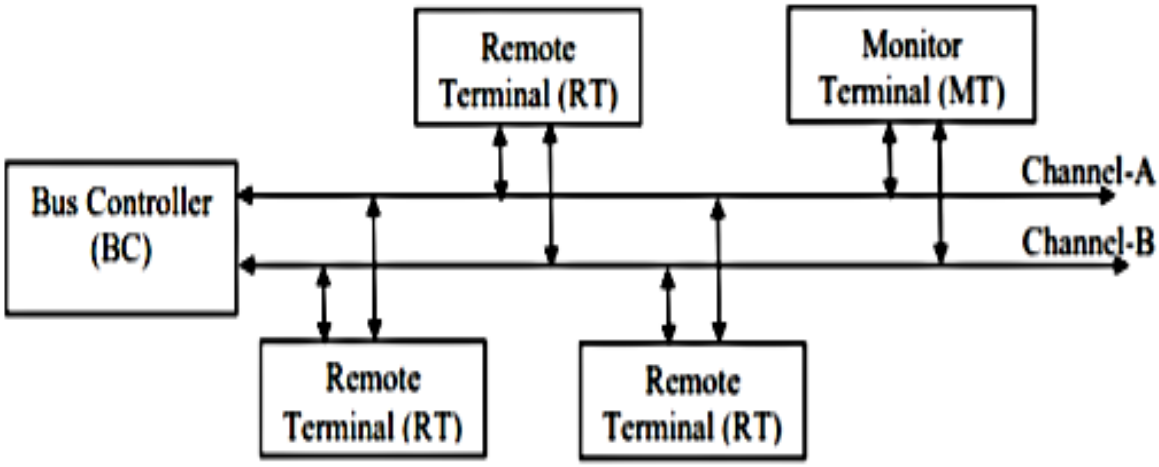


Figure 1: *Block diagram of MIL_STD_1553B.*

Bus Controller

The Bus Controller (BC) in the military standard 1553B is a sole source of communication and used to communicate between various remote terminals and subsystems over the data bus. It uses a command/response process for the data transfer. A single 1553B data bus will be interfaced with several terminals, among those terminals only one can act as a BC and active at a time. It initiates the command, which is responsible for:

- The data transfer between various remote terminals and subsystems.
- The control and management of the bus.

Remote Terminal

Any terminal not operating as either the bus controller or bus monitor mode is operating in the remote terminal (RT) mode. Remote terminals are the largest group of bus components. The RTs are connected between bus and various subsystems so it can also be known as an interfacing device and it includes all the necessary electronics for the data transmission. The subsystem connected to the RT is a sender or receiver of the data being transferred. We can interface a maximum of 31 RTs to a single data bus. After receiving the valid command issued by the BC, the RT will respond accordingly by sending the status word.

Bus Monitor

The bus monitor (BM) listens to all messages on the bus and records selected activities. The BM is a passive device that collects data for real-time or post capture analysis. The BM can store all or portions of traffic on the bus, including electrical and protocol errors. BMs are primarily used for instrumentation and data bus testing. The BM won't take part in data transmission.

Transmission Media

The twisted shielded pair transmission line is used as a transmission media and it connects the main bus and stubs. Each remote terminal has its stub to get connected with the bus (stub is to provide the local loads).

BUS CONTROLLER OVERVIEW

BC is the initiator of the data transmission or sole source of communication (if BC won't issue the command no data transmission takes place between RTs and subsystems). The bus controller can provide communication for 31 remote terminals and can control the data transmission over the data bus.

The two main pre-defined data transmission formats by the military standard 1553B are word formats and message formats.

Word Formats

The communication happens in the form of messages. Each message is made up of three unique word formats and each word format is total of 20 bits consisting of synchronization field of initial 3 bits, information field of next 16 bits and the last one is parity bit, which is always odd as defined by the standard (transmission occurs when it is odd).The message is a complete data transmission process from command word to a status word. The Command word, Data word and Status word are the three different word formats pre-defined by the standard and the word formats of all three words are shown in Fig. 2.

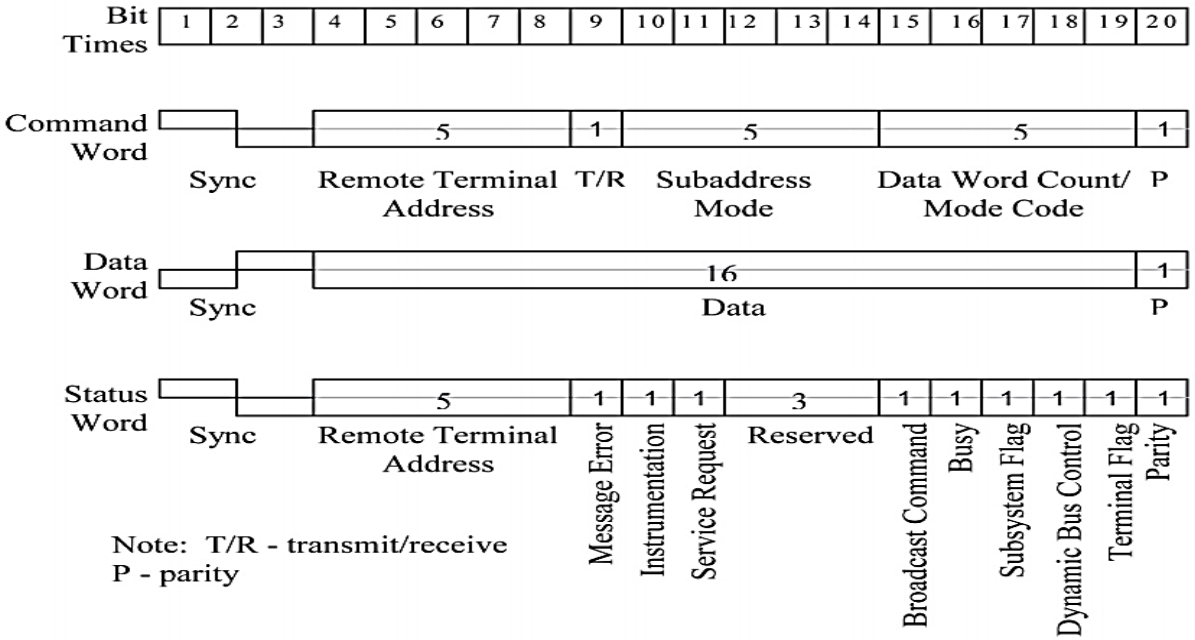


Figure 2: *Word formats of military standard 1553B.*

Command Word

Each word has its own format but a common structure. If the command word is considered, it has a field for synchronization, RT address, T/R bit (T/R = 0 – Receive and T/R = 1 – Send), sub-address mode, word count/mode code and the parity bit. The command word will always be issued by the BC to any RT to initiate them to send the data, receive the data or perform any other operations. According to the command word, the respective remote terminal will respond.

Data Word

Except for the synchronization field (to identify the word type) and parity bit, the data word has 16 bits for the information field and it consists of actual data to be sent. Both bus controller and RT can be able to send data word and the information field of 16 bits in the data word is user-defined based on the requirements. Each message can transmit up to 32 data words in military standard 1553B.

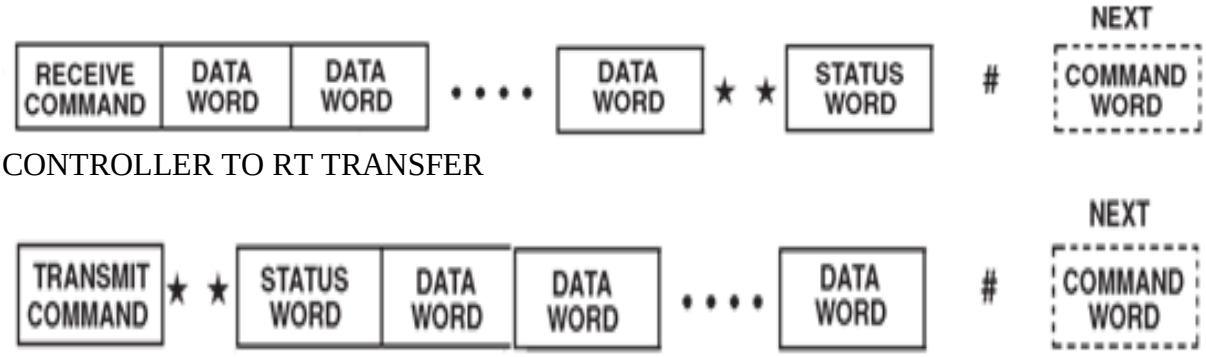
Status Word

The status word can only send by the RT, after receiving the valid command from the BC. The status word from the RT, when it receives the valid message from BC indicates the state of the RT that the message received was error-free and

accurate. If RT is busy it will send a busy signal and also the RT can send the service request to the BC through the status word. If the RT receives the invalid message from BC it will generate the error message. It also consists of a special bit called Dynamic Bit Control, when it is 1 the respective RT becomes BC and "the BC becomes RT or become inactive".

Message Format

The communication between BC and RT happens in the form of a message; this message is having different message formats (type of messaging). Among those message formats, two message formats are implemented, they are BC-RT and RT-BC. It uses the command/response method based information transfer. The message formats implemented here are pre-defined by the standard and those formats are shown in Fig. 3.



Note: # Intermessage Gap ** Response Time

Figure 3: *Message formats of MIL_STD_1553B.*

DESIGN AND IMPLEMENTATION OF BC

The BC consists of protocol controller, encoder and decoder. In this work, BC module is designed and implemented using Verilog HDL and simulated by Xilinx ISE 14.7 and three RT modules are designed to show how efficiently the transmission of data is done by the implemented BC. The proposed BC is shown in Fig. 4.

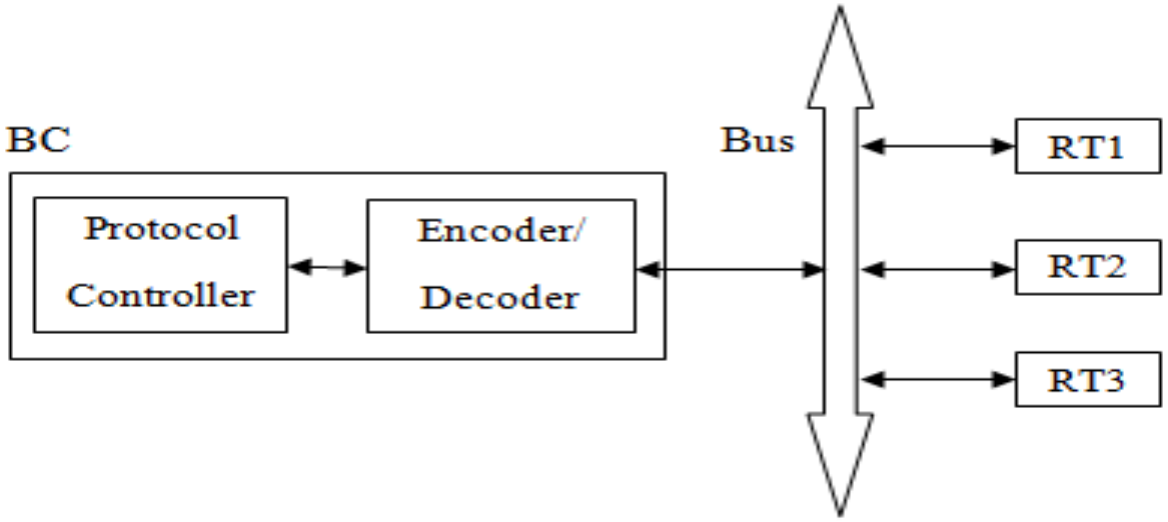
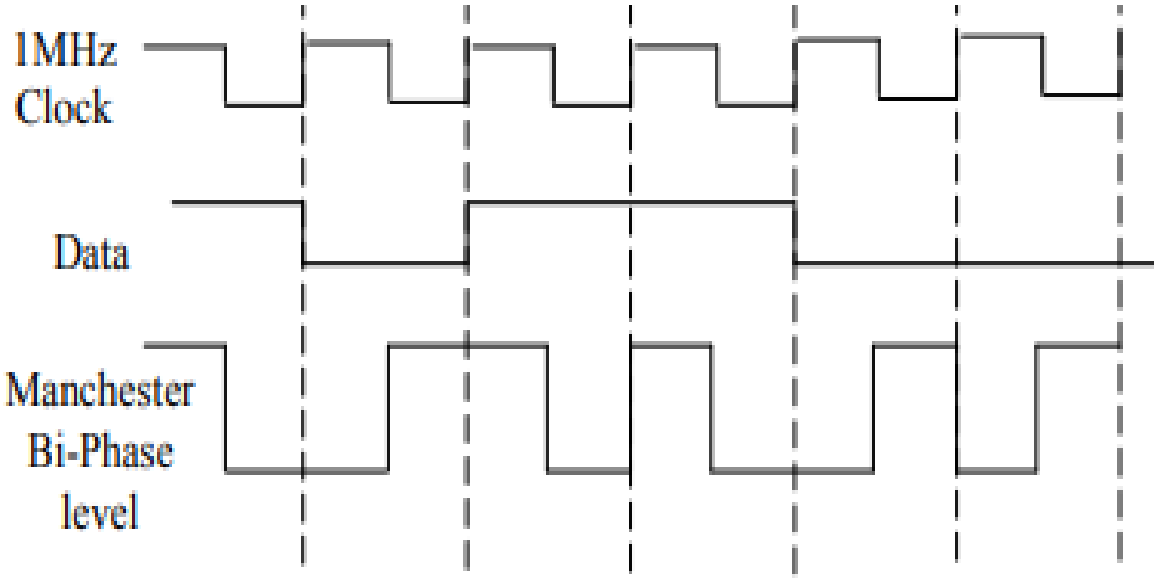


Figure 4: *Block diagram of proposed BC.*

The encoding and decoding technique used here is Manchester Bi-phase encoding and decoding technique because of its high bit error reliability also it uses fewer amounts of core cells compared to IRIG-B decoder. The separate encoder and decoder blocks are used but in this work, the common block of encoder and decoder is designed and included in the bus controller. The method of encoding is shown in Fig. 5 and decoding is the reverse process of it.



Data -- 0 => 0 to 1 1 => 1 to 0 For an equal amount of time

Figure 5: *Manchester bi-phase encoding.*

The protocol controller of BC will generate command word along with data word according to the request made by the user to BC. The generated command word is of 16 bits will be sent to the encoder, the encoder will encode the command word given to it and generate the encoded data of 20 bits by adding the parity bit and synchronization field of 3 bits to identify the word type. Based on the command word generated, type of the operation or message format (here, BC to RT or RT to BC) will be decided.

If it is BC to RT, the BC will send the command word of type receive along with the data word by setting T/R = 0 and Specifying data word count (1 to 32 data words per message) to be received by the remote terminal also the address of remote terminal to which it wants to communicate. Then the command word sent by the BC will be validated by RT. Thus particular RT will receive data words sent by the BC. After receiving, the RT will send the status word as an acknowledgement.

In case of RT to BC, the BC will send command word of type transmit by setting T/R = 1 and specifying word count to be sent and also the RT address to which it wants to communicate. The RT will decode the command word sent by the BC & then it sends the status word along with the number of data words specified by the BC through command word.

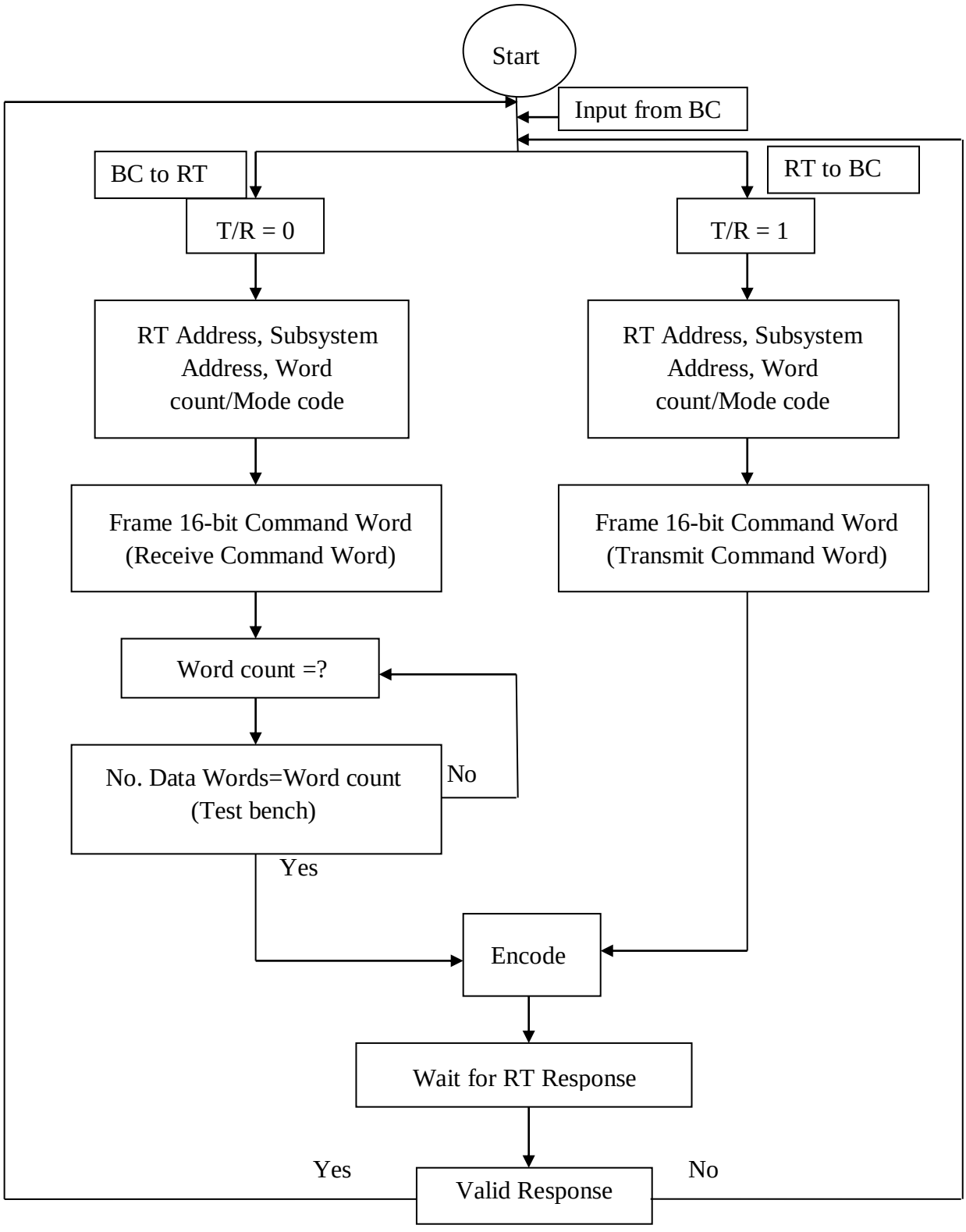


Figure 6: *Flow diagram of the proposed BC.*

Fig. 6 shows that the BC will give input to the protocol controller as per the user request then the protocol controller generates receive command (when T/R=0)

or transmit command (when T/R=1) from the input given by the BC. If it is a receive command, the protocol controller will send the command word along with the number of data words to be received. If the framed command word is of transmit type, protocol controller will send only command word. The output from the protocol controller will be encoded and sent over the bus and BC will wait for the RT response. If it receives a valid response the entire process will be repeated for the next message, if not the BC will discard this and will send the same message again it repeats for another 3 times.

RESULTS AND ANALYSIS

The design and implementation of BC is carried out by Verilog HDL and the simulation is carried out by Xilinx ISE 14.7 (targeted device – Spartan 6) and the results are obtained. Fig. 7 shows the schematic representation of proposed BC, Fig. 8 gives the information about delay which is obtained from the Xilinx ISE, Table 1 shows the comparison of timing results obtained and Fig. 9 and 10 shows the simulation results of the data transferred between BC to RT and RT to BC respectively and the Fig. 11 gives the device utilization summary.

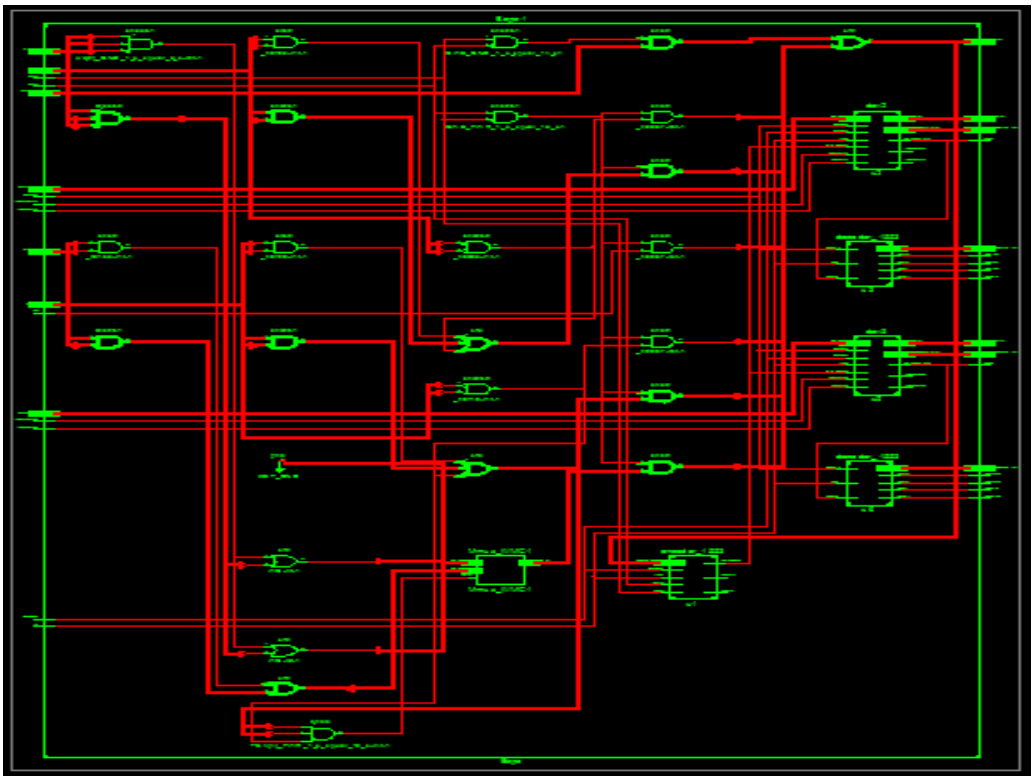


Figure 7: *Schematic representation of the proposed BC.*

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Timing Summary:
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Speed Grade: -3

   Minimum period: 3.847ns (Maximum Frequency: 259.919MHz)
   Minimum input arrival time before clock: 6.048ns
   Maximum output required time after clock: 8.046ns
   Maximum combinational path delay: 6.697ns
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Figure 8: *Timing summary.*

Table 1: *Comparison table of results obtained.*

Title	year	Min. period in ns	Min. i/p arrival time before clock in ns	Max. o/p required time after clock in ns	Max. combinational path delay in ns	Frequency of operation In MHz	Number of data words transmitted
Design and implementation of high performance MIL-STD-1553B Bus Controller	2017	10.599	12.484	4.394	_	94.350	4
An Efficient Implementation of MIL_STD_1553B Bus Controller Module using Verilog HDL (Proposed Work)	2019	3.847	6.048	8.046	6.729	259.919	4

From the obtained results, it is observed that the delay is 3.847 ns, which is promising and however the frequency of operation is increased to 259.919 MHz with respect to obtained delay.

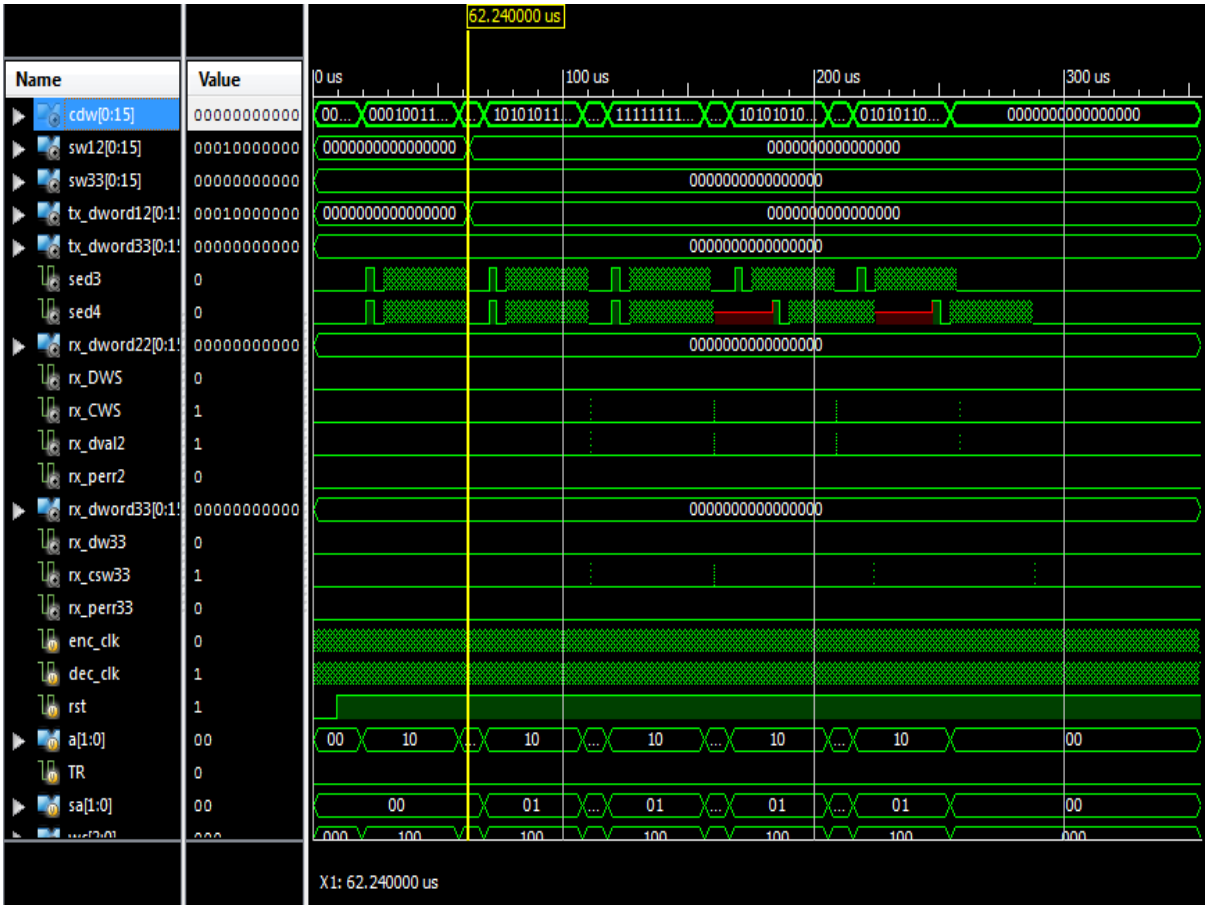

Figure 9: *Simulation result of BC to RT transmission.*

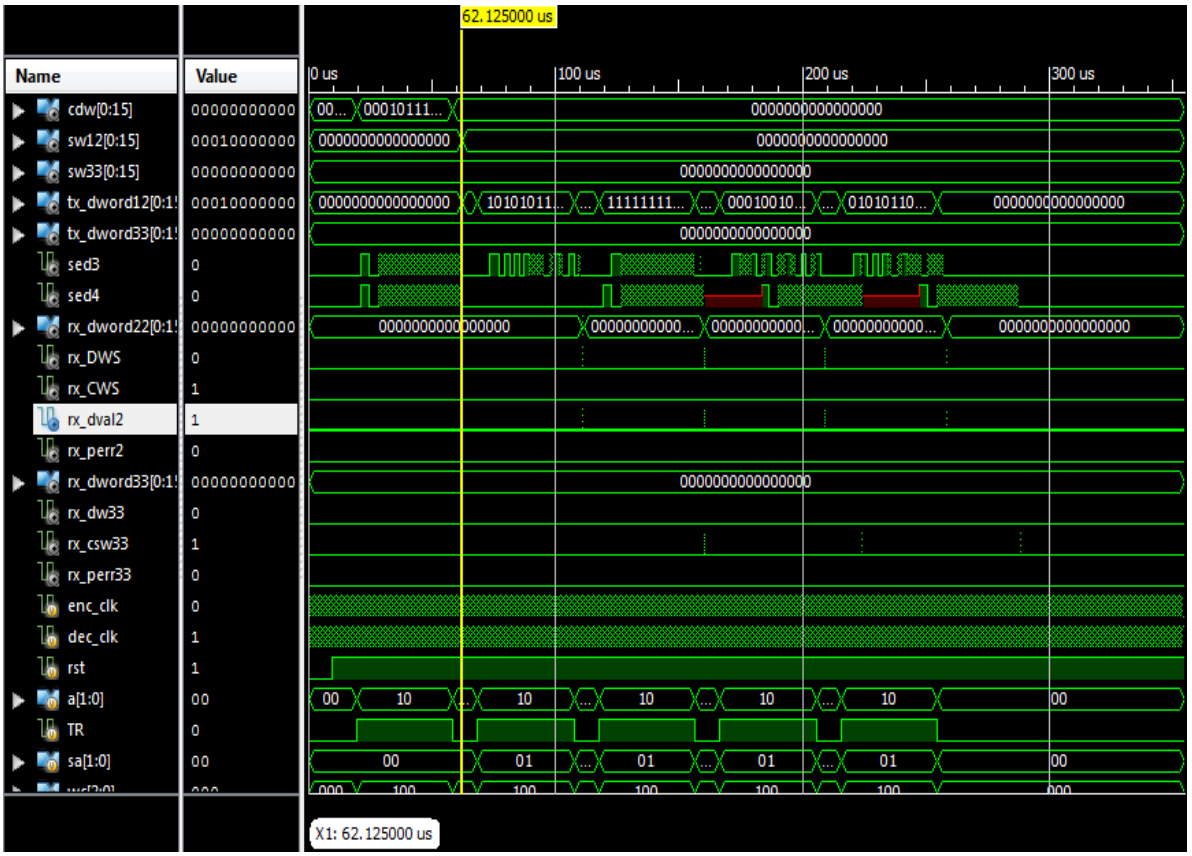

Figure 10: *Simulation result of RT to BC transmission.*

BC to RT: In Fig. 10, the BC has sent the receive command word along with the data words (cdw [0:15]), the number of data words transmitted here are 4 and the number of RTs implemented are 3 dev1, dev2, dev3 respectively, here dev2 (dev12) is giving response to the BC by sending the status word as an acknowledgment with respect to the RT address mentioned in the command word.

RT to BC: In Fig. 11, the BC has sent the transmit command word (cdw[0:15]), the dev2 (dev12) is giving the response to the BC by sending the status word along with the data words as an acknowledgment concerning the RT address mentioned in the command word.

Logic Utilization	Used	Available	Utilization
Number of Slice Registers	362	54576	0%
Number of Slice LUTs	434	27288	1%
Number of fully used LUT-FF pairs	294	502	58%
Number of bonded IOBs	205	190	107%
Number of BUFG/BUFGCTRLs	2	16	12%

Figure 11: *Device utilization summary.*

As per the targeted device, device utilization summary is shown in Fig. 11.

CONCLUSION

The BC module of the Military standard 1553B is the main initiator for the communication between RTs and subsystems so the BC module is implemented and its typical operations like BC to RT and RT to BC are verified. From the obtained results it is evident that its frequency of operation is increased to 259.919 MHz with respect to the obtained delay 3.847 ns, which is promising for the typical high speed applications.

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