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The Fourth Fundamental Element to Memristor-based Memory

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Abstract

The realization of the missing memristor by Hewlett-Packard in 2008, the memristor, adds a new promising technology that enable the continuous improvement of the performance, speed and cost of integrated circuits. This paper deals different models of memristor having certain advantages and disadvantages. Different applications such as chaotic circuits using memristor, memristor based oscillator, Composite behavior of parallel and series memristor circuit, Memristor to eliminate the improper shutdown of computer with no data loss and the most important memristor based memory which can replace current flash memory has been discussed and its future development is discussed. The memristor based memory has the bright future, because it can store multi-bit like 2-bit or multi-bit storage.

Keywords: Component, formatting, insert, style, styling

INTRODUCTION

In the circuit theory, we know about three basic fundamental elements as capacitor C, resistor R, and inductor L. Leon Chua in 1971 1, introduced 'memristor' which is non-linear passive two terminal electrical component having the relationship between electric charge and magnetic flux linkage as shown in Error! Reference source not found.. He characterized memristor as charge-controlled if the relationship of f (q, ϕ) is expressed as a function of charge and as a flux control if the relationship of f(q, ϕ) is expressed as a function of flux. The voltage across the charge controlled memristor was given by:

$$v(t) = M(q(t))i(t) \quad (1)$$

Where, $M\big(q(t)\big) = d\varphi(q)/d(t)$ incremental -memristance and has unit of resistance.

Similarly, the current of flux controlled memristor is given by

$$i(t) = W\big(\varphi(t)\big)v(t) \quad (2)$$

Where, $W(\varphi) = dq(\varphi)/dt$ incremental menductance and has unit of conductance.

He also realized that certain type of memristor can be used for switching and delaying signals. Although no physical memristor was developed without internal power but there was a hope of inventing physical memristor device with monotonically increasing ϕ-q curve as shown in Figure 2. In 1976, Chua and Kang 2, generalized memristor system model, generic properties of memristor system and canonic dynamical system model was presented. Memristive system are hysteric in sense that their Lissajous figure as shown in Figure 3 which passes through the origin vary with the excitation frequency and combinations of non-linear resistive, capacitive and inductive component cannot duplicate the circuit properties of non-linear memristor. Some examples of physical device which where modeled as memristor one-port are as follows:

Thermistor, discharge tube as a first-order and Ionic system as second-order time-invariant current controlled memristive one-port. Also, Ionic system as a first-order time-invariant voltage controlled memristive one-port for potassium channel.

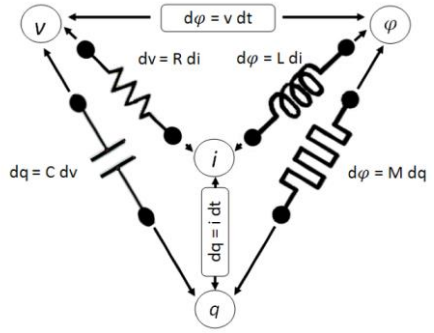


Figure 1: *Four basic elements and their physical relationship.*

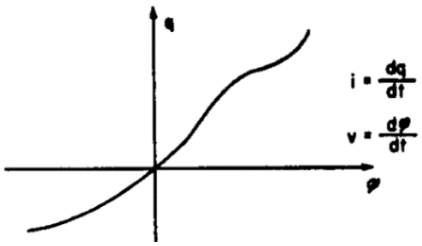


Figure 2: *Monotonically increasing flux and charge curve.*

To identify memristive devices, passivity criterion, no energy discharge property, DC characteristics, Double-valued Lissajous figure property, symmetric Lissajous figure property, limiting linear characteristic, small signal AC characteristics, local passivity criterion, these properties are used.

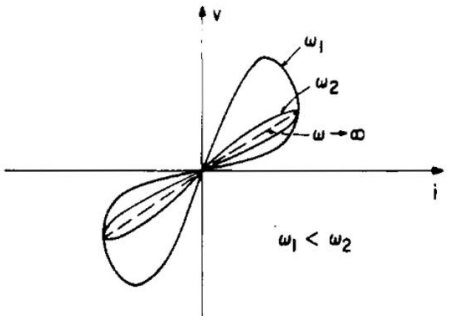


Figure 3: *Frequency response of Lissajous figure.*

At the same time, there was no direct connection between mathematics and the physical properties of any physical system, and hence, it almost took forty years to adopt this concept. In 2008 3, R Stanley Williams et al., fabricated solid state implementation of electrical device that behave as perfect Memristance with certain restricted range of state variable w. This w specifies the distribution of dopants in the device. The state variable w concept was not anticipated by Chua. The basic equation of current-controlled memristor for circuit analysis in differential form:

$$v = R(w)i \quad (3)$$

$$\frac{dw}{dt} = i \quad (4)$$

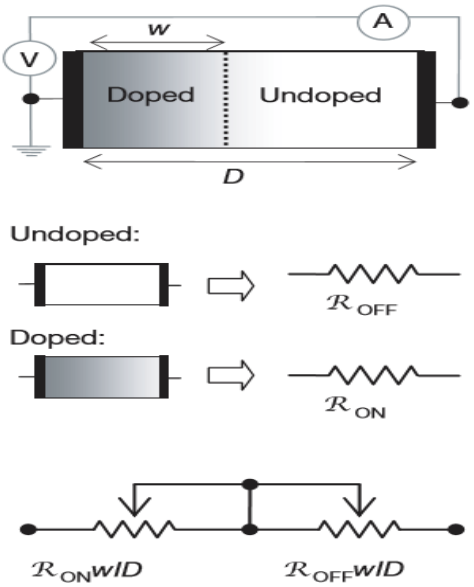


Figure 4: *Two terminal electrical (TiO_2) devices and its total resistance.*

R is resistance that depends upon internal state of the device; w is the state variable which specifies distribution of dopants in the device. Here, they consider thin semiconductor (TiO2) layers thickness D, in which one layer is doped with oxygen (Ron indicating low resistance because of more oxygen) and other layer is undoped (Roff indicating high resistance) are sandwiched between two metal contacts (Pt.), as shown in Figure 4. The total resistance of the device is determined by two variable resistor connected in series Roff and Ron. The external bias v(t) across device will move boundary between two layers by causing the charged dopants to drift with average ion mobility μ.

$$v(t) = \left(Ron\frac{w(t)}{D} + Roff\left(1 - \frac{w(t)}{D}\right)\right)i(t) \quad (5)$$

$$\frac{dw(t)}{dt} = \frac{\mu Ron}{D}i(t) \quad (6)$$

Memristance of the system for which Roff <<Ron give as,

$$M(q) = Roff(1 - \mu\, Ron/D^2 \times q(t))$$

It has been clearly stated that magnetic field does not plays any role in the mechanism of memristance, this is one possible reason why this phenomenon has been hidden for so long. Physical memristor device is inaccessible so, it is very useful to have computer model of memristor as a tool for speeding up the analysis of the behavior and developing application of memristor via simulation experiment. In 2009 study done and suggested a concrete window function that will correspond to the memristor was proposed in the following form [4]:

$$f(x) = 1 - (2x - 1)^{2p} \quad (7)$$

Where, p is the positive integer.

As shown in Error! Reference source not found., difference between models with linearity and non-linearity drift disappear when p increases. The window function describe that the non-linearity in ionic transport appear particularly at the thin film edge where the speed of the boundary between the doped and undoped regions gradually decreases to zero.

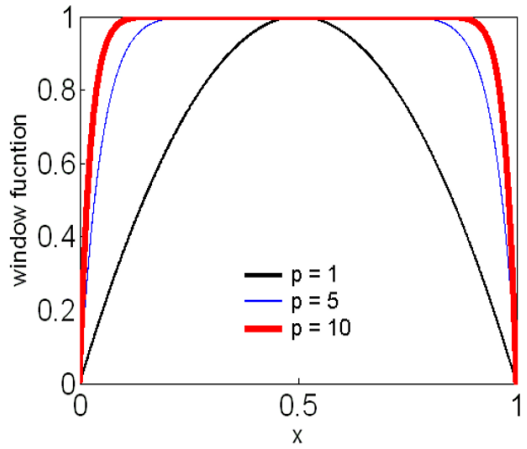


Figure 5: *The window function (6) described by Joglekar et al. for p= 1, 5 and 10.*

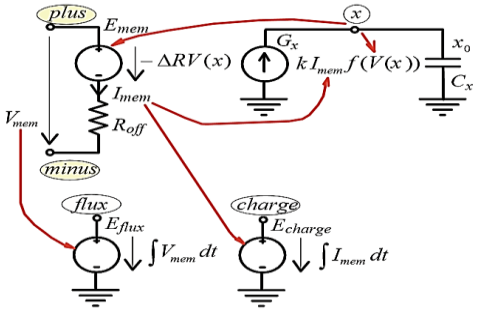


Figure 6: *Structure of SPICE model.*

In 2009, Z. Biolek et al. 5, described the SPICE model of the memristor fabricated by HP laboratories. The SPICE structure of the memristor made up on the basis of state equations. These equations modelling the boundary affect which offers results better than Joglekar et al., model as shown in Error! Reference source not found.. They also discussed about two problems, associated with boundary effect, related to the way of defining window function. First, the memristor remembers the x-coordinate of the boundary between two layers not the amount of electric charge that pass through it. Second, modeling the memristor as component which exactly remembers the entire electric charge which pass through it.

As a result, window function was considered as a measure of the amount of electric charge that stores memristor but the memory effect is lost at boundaries. This difference between the behavior of the model and the requirements for operation of real memristive circuit element was resolved by a new window function as:

$$f(x) = 1 - [x - u(-i)]^{2p} \quad (8)$$

Where,

$$u(i) = \begin{cases} 1, if\ i \geq 0 \\ 0, if\ i < 0 \end{cases} \quad (9)$$

'P' is positive integer and 'i' is memristor current. One advantage of Biolek's window function as shown in Error! Reference source not found. is that it remove the coverage issues at the boundaries of memristor model.

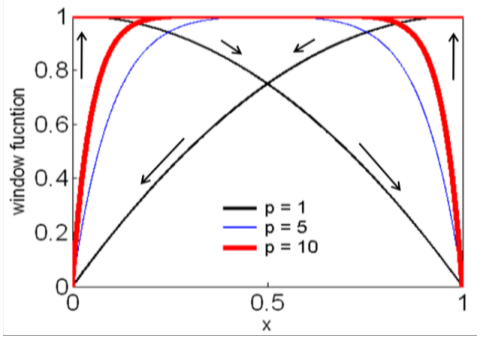


Figure 7: *Linear window function (8) proposed by Z. Biolek et al.*

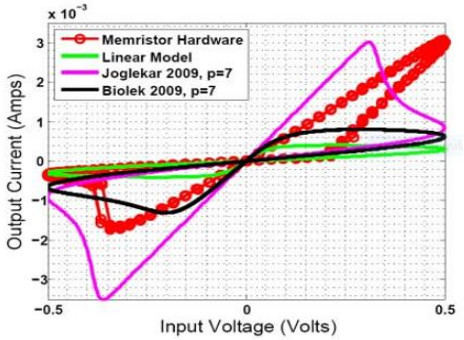


Figure 8: *Comparison between linear, Joglekar and Biolek memristor model.*

In 2010, Nathan R McDonald et al. 6, analyzed the above function and explained it by giving an example as, if x starts at 0, f(x)=1. Then, x increases approaching D, the f(x) approaches 0. Once current reverse the direction f(x) immediately switches 1. Then, as x decreases back to 0, f(x) also decreases to 0. When current reverses, the cycle begins once again. Comparison between memristor hardware, linear model, Joglekar model and Biolek model is shown in Figure 8. The disadvantage of non-linear model is that it doesn't consider the non-linearity of the large electric field within a memristor .This disadvantage is overcome by Exponential Model. Yang et al. 7 used equation 10 to fit the experimental measure I-V characteristic of memristor:

$I = x^n \beta \sinh(\alpha V) + \chi(\exp(\gamma V) - 1)$(10)

Where, α, β, γ, χ are fitting constant and n is free parameter. At OFF-state, the I-V curve behaves similar to a P N junction (the exponential part); while at ON-state the I-V curve follows a tunneling process (sinh part). However, the state equation will be modeled by the following nonlinear equation:

$\dot{x} = \text{asinh}(bv) f(x, i)$ (11)

Where, f(x, i) can be any window function. Mathematical modeling of a memristive device using different window functions are described and compared in Table 1 by Hazem Elgabra et al. 8. They also discussed disadvantages with these models and discovered a modified model that gives more realistic description of a memristor device.

Table 1: *Comparison between linear, non-linear, exponential model.*

Models	Linear	Nonlinear	Exponential
Boundary Conditions	✗	✓	✓
Window Function	✗	✓	✓
Nonlinear in Electric Field	✗	✗	✓
Voltage sensitivity	Linear	Linear	Highly nonlinear
Switching time	Symmetric	Symmetric	Symmetric (polarity-dependence resistance)

Thus, the exponential model presents a more sensible description of a functional memristive device because this model is more sensitive to voltage level which gives it the flexibility to stable reading with fast writing. A low voltage level can be used

during the read process and higher voltage level can be used for writing the memristor in much smaller times. Exponential model has many features that make it predominant to all other models in terms of its ability to describe memristor-base memory functionality. They also introduced a reading access approach that enhances the stability of the memristor and reduces its power consumption.

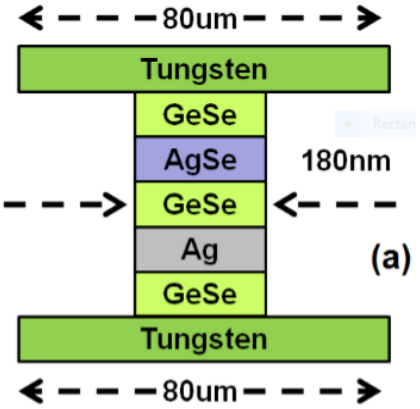


Figure 9: *Chalcogenide-based memristor model.*

Various memristor devices have been developed since HP have announced its TiO2 memristor, like polymeric memristor, layered memristor, polymeric memristor, ferroelectric memristor, carbon nanotube memristor, spin memristive systems. These memristive devices have some advantages and drawbacks over others. In 2010, Robinson E. Pino et al. 9, developed ion conductor Chalcogenide-based memristor model, that utilize single valued equation and describe all regions of operation of memristor devices. Additionally, improvements have been made to this memristor model to include non-linear boundary conditions. The non-linear boundary conditions proposed are of form:

$$f(w) = 1 - [\frac{w}{D} - u(-i)]^{2p} \quad (12)$$

$$f(w) = 1 - [\frac{2w}{D} - 1]^{2p} \quad (13)$$

The non-linear window function in (12) and (13) assure zero velocity of the doped/undoped barrier interface as w reaches either boundary, w=0 and w=D. Moreover, when p increases the difference between the models with linear and non-linear drift disappear.

APPLICTIONS

Memristor based Chaotic Circuit

Since 2008, when Itoh and Chua proposed first chaotic circuit in 10, many chaotic circuits have been developed. Bharathwaj Muthuswamy in 2010 11, implemented memristor based chaotic circuit. This memristor circuit is not an emulator but a physical device. The circuit is also suitable for prototyping on the breadboard and has frequency content in the 0.5 kHz range.

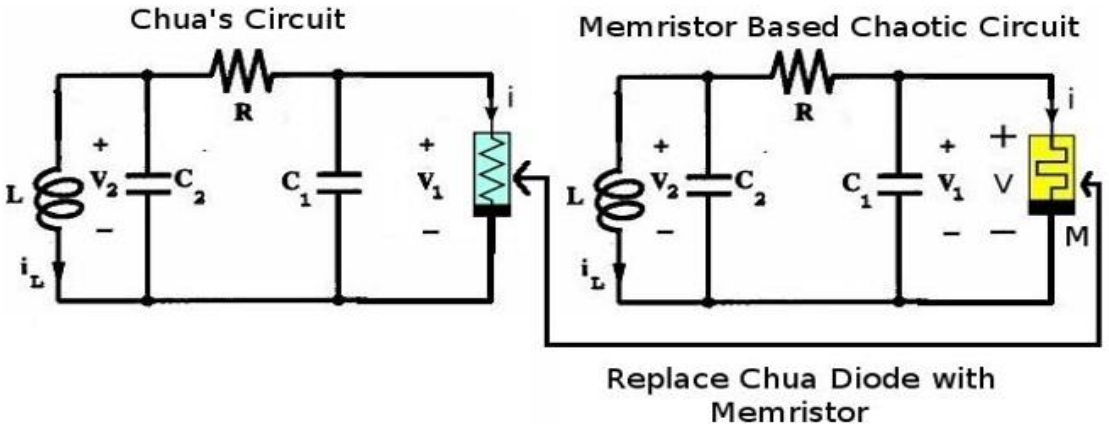


Figure 10: *The memristor chaotic circuit is made by replacing chua's diode with the flux controlled memristor.*

In 2013, Zhang Xuliang et al. 12, proposed a new memristor emulator using several simple discrete components. The emulator can meet most of the behavior characteristics of a generic memristor. The equivalent circuit of the emulator is shown in Figure 11, which is simply composed of a common varactor in series with an inductor and a common diode. The emulator can be seen as a charge-controlled nonlinear resistor with memory, and the hysteretic loop does have the tendency to be a straight line when in the limit of infinite frequency as shown in Figure 12, and for the existence of the varactor, the emulator can only act as a memristive system with the circuit under running; it cannot store the information after power off, like an ideal memristor. The simplest chaotic circuit has been discovered as the three elements circuit as shown in Figure 13. The memristor to be the only locally active element and non-linear device, which provide the circuit with the necessary non linearity and the third state variable.

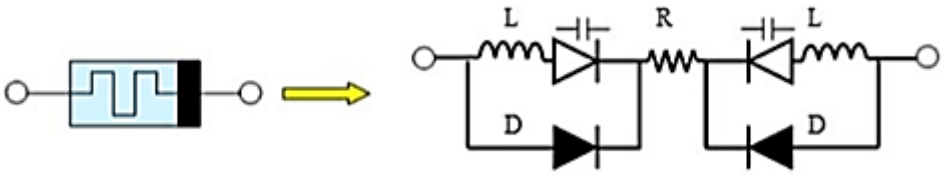


Figure 11: *Memristor emulator circuit.*

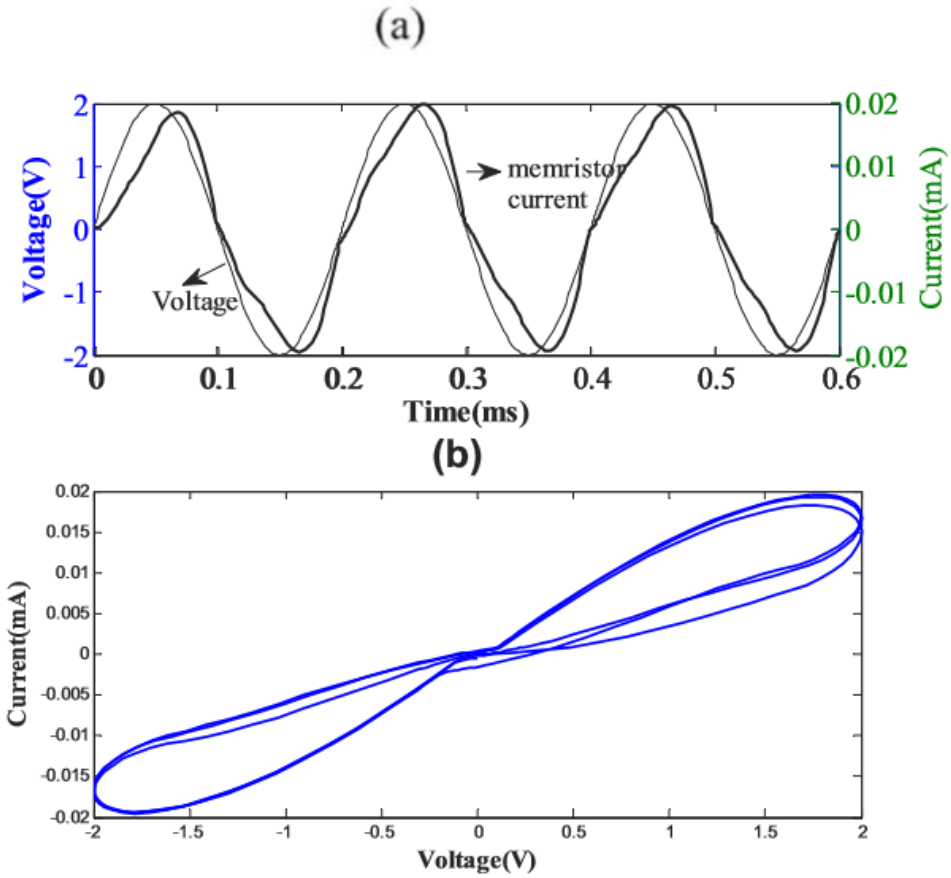


Figure 12: *(a) The applied sinusoidal voltage and the current flows through the emulator; (b) i−v curve of the emulator when sinusoidal stimulus applied.*

Memristor based Oscillator

In 2011, M. Zidan et al. 13, proposed memristor-based reactance-less oscillator as shown in Figure 14. Later A. G. Mosad et al.14, presented an improved memristor based relaxation oscillator which offer higher frequency range and wider tuning range and can operate on the positive supplies or alternatively a positive and negative supply and as shown in Figure 15. Memristance resistance is in range: $R_{on} < R_m < R_{off}$ so, memristor resistance is forced to oscillate between Ron and R_{off}. The memristor resistance R_m is given by,

$$R_m(t) = R_a \frac{(V_{01}(t) - V_{in}(t))}{(V_{in}(t) - V_{out}(t))} \quad (14)$$

Consequently, the proposed oscillator provides a suitable solution for low frequency applications such as the biomedical and embedded systems applications.

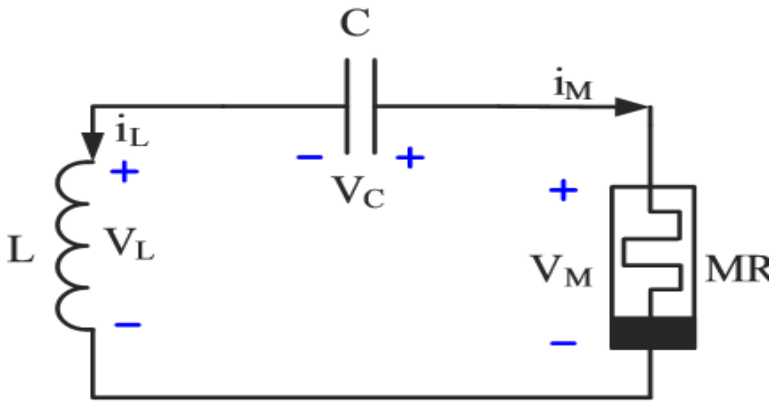


Figure 13: *Simplest chaotic circuit.*

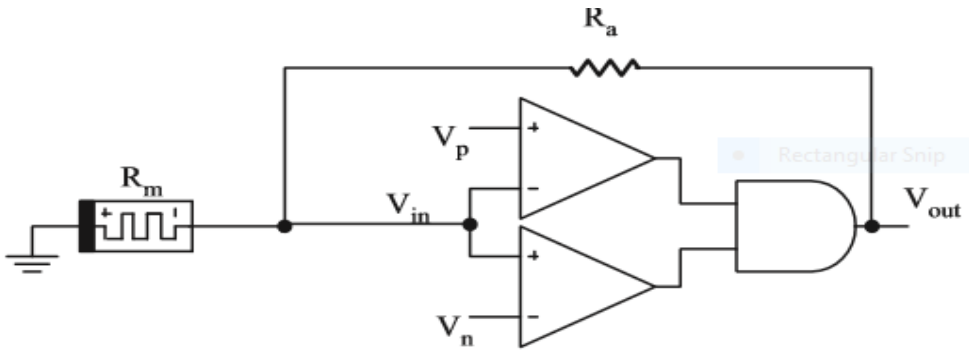


Figure 14: *Memristor based reactance-less oscillator.*

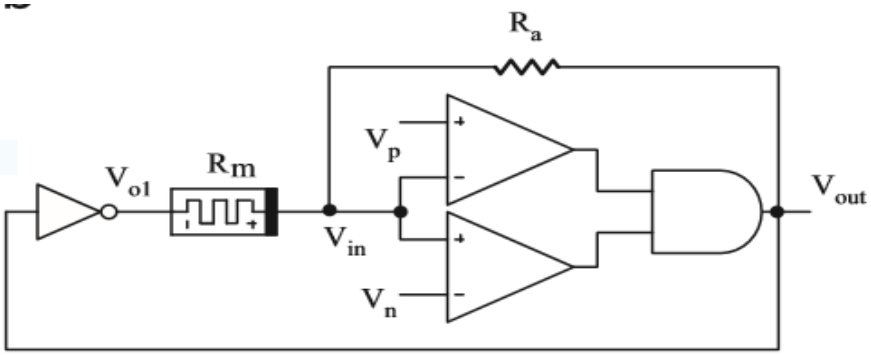


Figure 15: *The proposed memristor-based relaxation oscillator circuit.*

Composite Behavior of Parallel and Series Memristor Circuit

In 2013, Ram Kaji Budhathoki et al. Error! Reference source not found., analyzed composite behavior of parallel and series memristor circuit by assuming all memristor circuit operate at a stable composite memristance state.

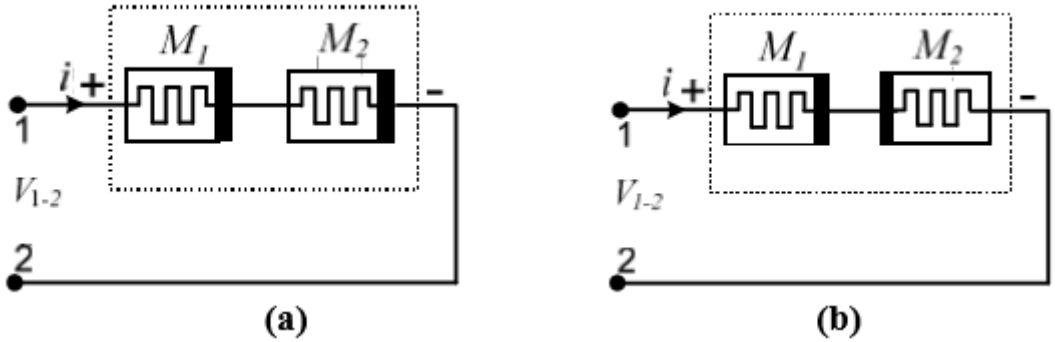
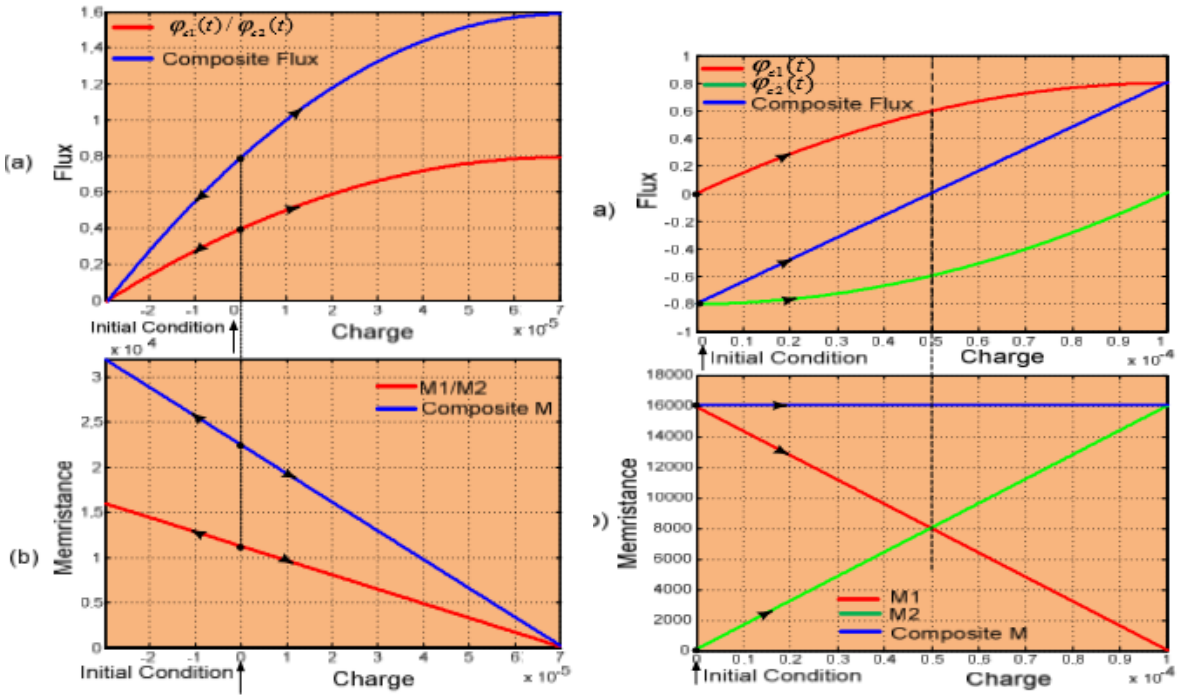


Figure 16: *A serial memristor circuits (a) with the identical (b) the opposite polarities.*

It has one important advantage that it can be fully integrated on-chip proving an area efficient solution. In serially connected memristors as shown in Figure 16, the sign of composite flux is changed depend upon the corresponding memristor polarity.



(a) (b)

Figure 17: *(a) same polarity device (b) Opposite polarity device.*

The flux v/s charge curve as shown in Figure 17 of the composite device with the same polarities becomes more nonlinear, and the composite memristance increases, for the same amount of input charge. Whereas device with opposite polarities becomes linear, due to the complimentary action of the back-to-back series connected memristors. The composite memristance is constant, when none of the memristors in

the composite device is operating at the boundary. In the case of the parallel memristor circuit with the same polarities, the composite charge is increased as the number of parallel memristors is increased, while the flux remains constant as shown in Figure 18. The range of variation of the composite memristance becomes smaller.

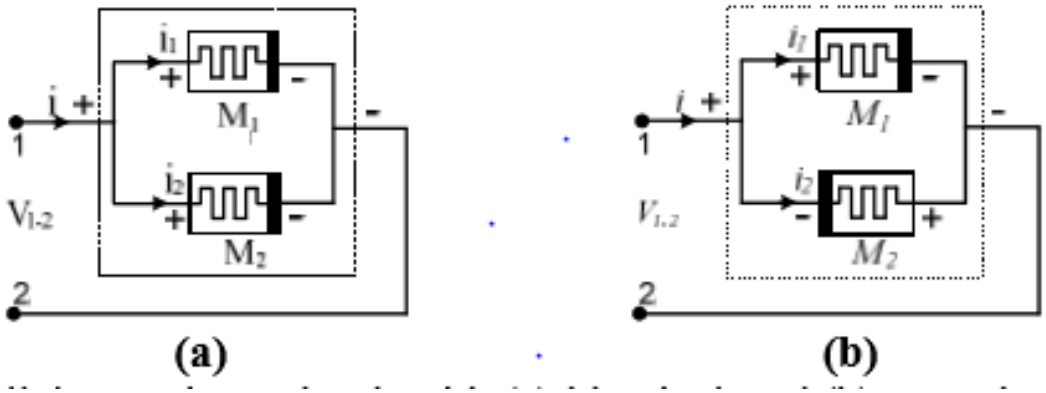
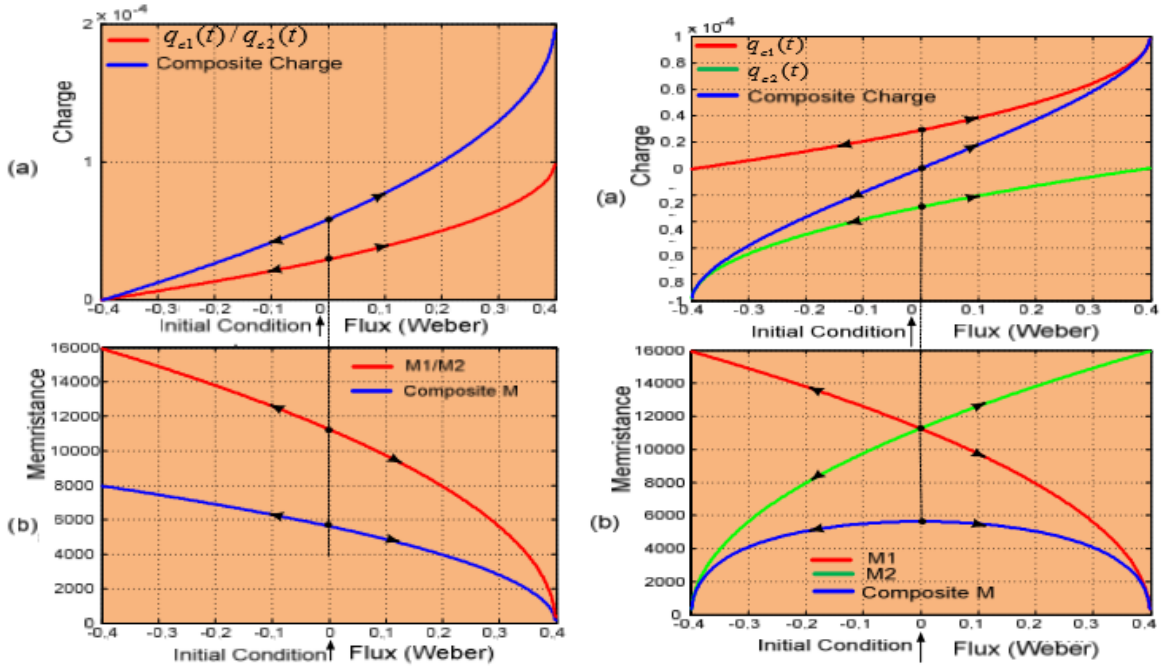


Figure 18: *Parallel memristor circuit (a) identical (b) opposite polarities.*

However, the charge vs. flux curve of parallel memristors with opposite polarities becomes more linear than that of single memristor, and the composite memristance changes gently as shown in Figure 19.



(a) (b)

Figure 19: *(a) Same polarity device (b) Opposite polarity device.*

Memristor to Eliminate the Improper Shutdown of Computer with No Data Loss

In 2014, Awadhesh Kumar Maurya et al. 16, described memristor applications as 1 bit non-volatile memory as a flip-flop, 2-bit adder, 2-bit multiplier and the most application of memristor is to eliminate the improper shutdown of computer with no data loss.

Memristor Based Memory

Memristor offers a promising alternative to conventional memory devices. Recently used memory devices such as DRAM, SRAM, and NAND Flash will soon be facing difficulties due to continuous scaling down. Memristor are considered to be very good component for future memory device when compared to other emerging technology such as Magneto Resistive RAM (MRAM) and phase change RAM (PCM/PCRAM).These memories have property of remembering data after bias removal, but memristor have advantage of high density over others. Detailed comparison between memristor based memory, traditional memories and other emerging memories is shown in

Table 2. From table we can see that the memristor based memories are good candidate for replacing both permanent and running storage devices. Memristor based memory is fabricated as a high-density cross bar architecture. Memristive devices are located at each intersection between two cross bars as show in Figure 21. In memristor based memory write operation is straight forward but read operation is more challenging.

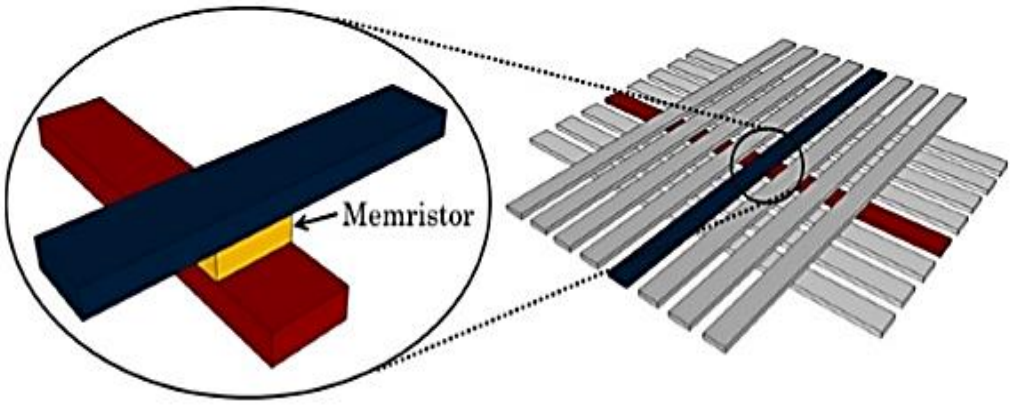


Figure 20: *Memristor based memory architecture.*

Table 2: *Comparison between different memories.*

	Memristor	PCM	STT-RAM	DRAM	Flash	HD
Chip area per bit (F^2)	4	8–16	14–64	6–8	4–8	n/a
Energy per bit $(pJ)^2$	0.1–3	2–100	0.1–1	2–4	10^1–10^4	10^6–10^7
Read time (ns)	<10	20–70	10–30	10–50	25,000	5–8x10^6
Write time (ns)	20–30	50–500	13–95	10–50	200,000	5–8x10^6
Retention	>10 years	<10 years	Weeks	<Second	~10 years	~10 years
Endurance (cycles)	~10^{12}	10^7–10^8	10^{15}	>10^{17}	10^3–10^6	10^{15} ?
3D capability	Yes	No	No	No	Yes	n/a

In 2012, Mohammed Affan Zidan et al. 17, investigated read operation of memristor based memory and also analyzed the sneak path problem. They also introduce a new technique for solving the sneak path problem by gating the memory cell using a three terminal memristor device as shown in Figure 22.

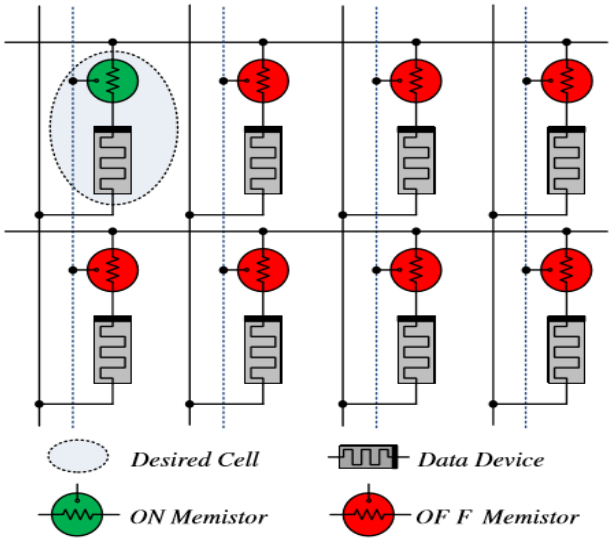


Figure 21: *Structure of proposed memristor gate array where an example of selected of selected cell is shown.*

In 2015, hybrid crossbar architecture for a memristor based cache was proposed by Chris Yakopcic et al. 18, is used in high density cache design and also to remove the long write latencies of memristor device. This scheme allows multiple read and writes to concurrently access different sub array within a cache. This paper deals with breaking a large memristor grid into smaller size of 4×4 or 8×8 memristor surrounded by isolating transistor. This will improves the noise margin of the system, while still enabling much higher densities.

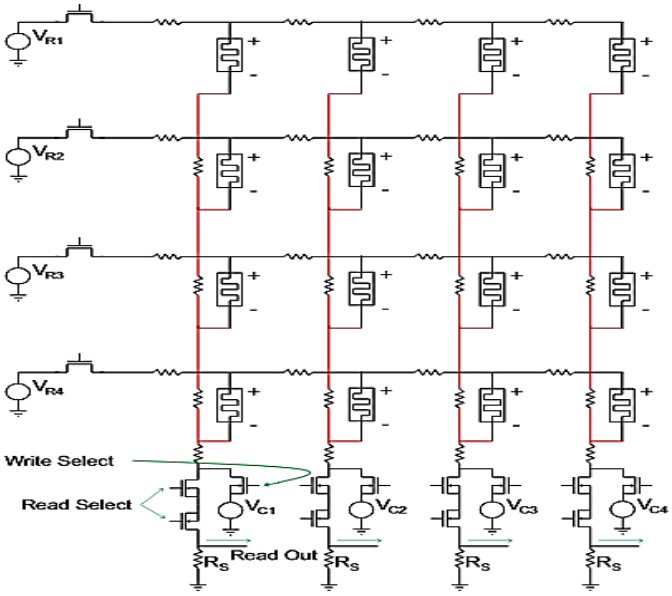


Figure 22: *Crossbar circuit used to carry out noise margin and energy experiment.*

In a proposed hybrid crossbar memory, a large memory array composed of many smaller memristor crossbar arrays along with transistors is shown in Figure 23. These memory based caches can improve the performance of processor and reduce overall power consumption more than STT-MRAM and SRAM cache implementation. However, this device has a resistance that is still too low for use in a cache.

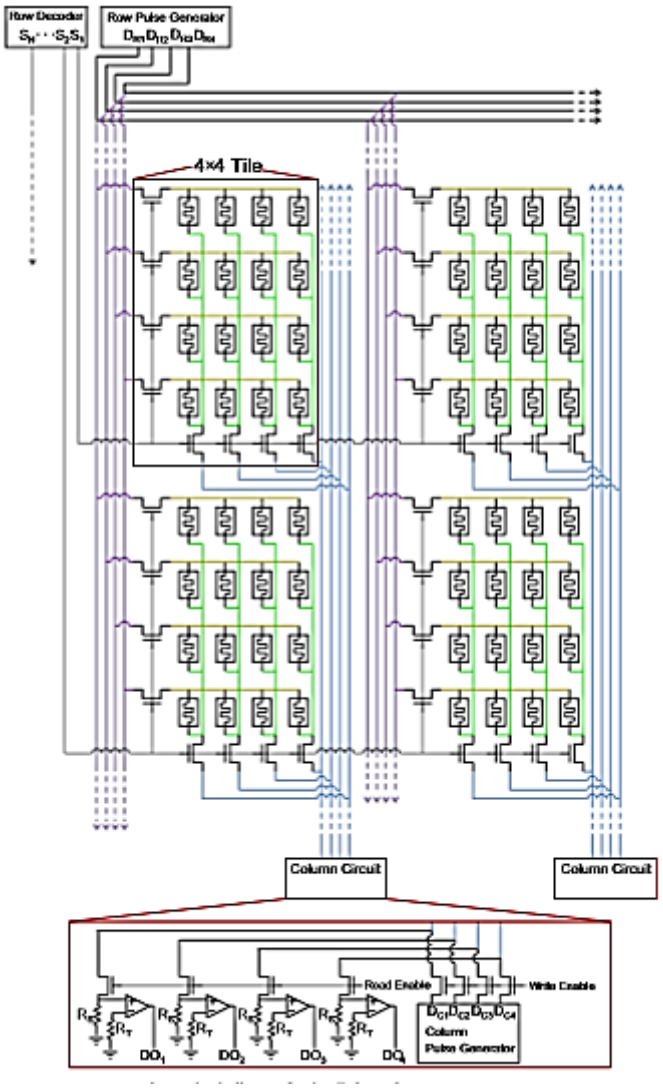


Figure 23: *Circuit diagram for the crossbar memory structure.*

The memristor device can be used to store multi-values state such as “00”, “01”, “10” and “11” as shown in Figure 24. In 2-bit memory case, there will be 3 different thresholds values are used. For n-bit storage, the memristive device can use m different threshold values where n and m is a non-zero integer.

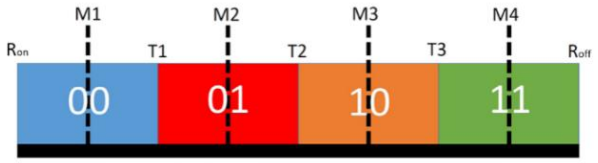


Figure 24: *Threshold values bounds for the 2-bit memristor-based memory cell.*

The process variation occur in the fabrication of nano-scaled memristive device makes it difficult to control its dimension. Process variation is originated from following two main sources:

- The sub-wavelength lithography process.
- The random uncertainties of the dopants atoms which increases as the technology is scales.

The memristor parameters such as width, length, thickness and device resistivity fluctuate due to process variation. This process variation effects on the memristor based memory and result in write and read failure. In 2016, hassan mostafa 19, described about the statistical yield improvement under process variations of multi-valued memristor based memory.

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