A Low Power Time Domain ECG Interface Based on Flexible a-IGZO TFTs

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***Abstract*—This work presents a low power ECG interface for wearable applications, based on unipolar a-IGZO TFTs manufactured on a flexible substrate. The interface consists of a cascaded diode-connected load preamplifier followed by a reset integrator, which is used to convert the voltage signal to a pulse-width modulated (PWM) representation. The output is thus provided as a binary PWM waveform, which can be conveniently sent to a reader device using wireless communication and can be further converted to a digital representation using a simple counter. The flicker noise and the offset are eliminated using an approach similar to correlated double sampling. An input chopper is exploited to alternate the connection between the inputs of the preamplifier for each sample. The output signal is then extracted by subtracting two consecutive samples after conversion to the digital domain. In this way offset and low-frequency noise, which are correlated between the two samples, are effectively cancelled.**

Keywords—IGZO; ECG; bio-signal read out; voltage to pulse width conversion.

I. INTRODUCTION

Wearable electronic devices are gaining a growing research interest and popularity. Wearables should be power-efficient to ensure long battery life. Besides, they should be flexible and conformable to the human body, to increase user comfort. Amorphous Indium Gallium Zinc Oxide (a-IGZO) Thin Film Transistors (TFTs) are very suitable for this kind of applications as they can be fabricated on large flexible substrates at low cost, provide sufficient mobility to cope e.g. with low-frequency bio-potential signals (their typical mobility is between 15 and 20 cm^2/Vs), and ensure good parameter uniformity.

Conversion to a robust representation (e.g. digital) is essential before sending signals from a wearable patch to a reader device (e.g. smart phone), to increase noise immunity during transmission. Bio-signal acquisition systems designed and fabricated using flexible TFT technologies have been published in literature for electroencephalogram (EEG) [1], electromyogram (EMG) [2,3] and heart rate (HR) [4] measurements. However, in [1], [2] and [3] the signal is not digitized. Moreover, the power consumption reported in [1] is 11 mW, which is rather high for wearable applications. The power consumption reported in [4] is much lower, but the total input referred noise achieved in that work is relatively high, enabling only HR measurements. The input signal is digitized in [5] but power consumption is still 2 mW, and the circuit

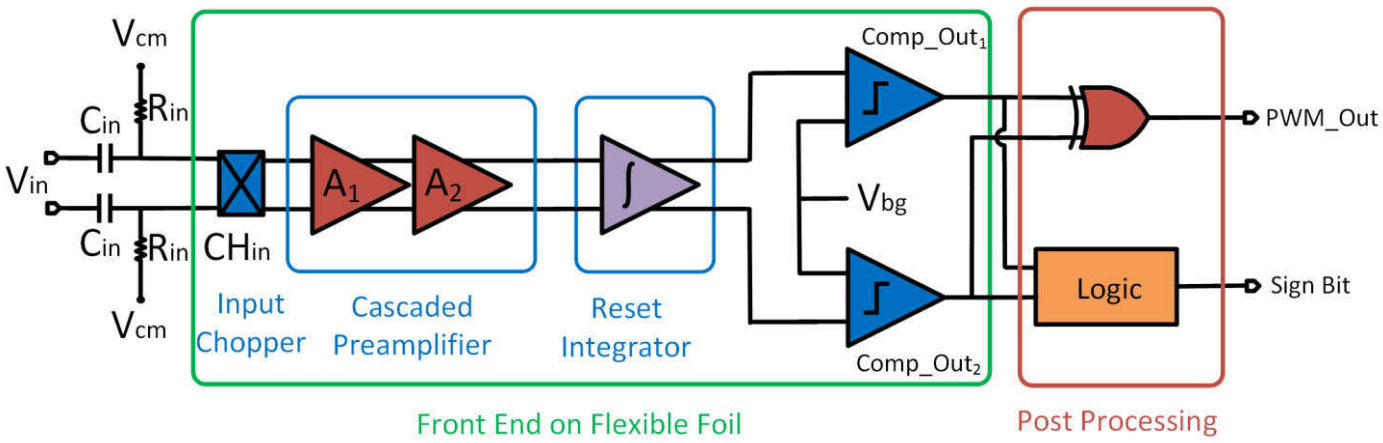

Fig. 1 General system architecture

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does not provide a voltage, but a current input, making it inconvenient to measure bio-potentials. In this paper the analogue output from a voltage-mode front end is converted to PWM waveform with low power consumption. A system level chopping approach is used to reduce input referred noise and achieve a noise performance compatible with electrocardiogram (ECG) measurements.

The rest of the paper is organized as follows: In Section II an introduction of the a-IGZO TFT technology used for this work is given. Section III discusses the system architecture, while the circuit principles are discussed in Section IV. Section V presents the simulation results and Section VI concludes the paper.

II. TECHNOLOGY

The system presented in this work is built using dual gate self-aligned a-IGZO TFTs, which are manufactured on a glass substrate covered with a flexible 15µm thick polyimide layer to enable flexible circuits. The TFTs are unipolar n-type transistors with a channel mobility around 16 cm^2/Vs. The back gate of the TFT can be conveniently used in circuit design e.g. to increase the output resistance or the transconductance. The typical operating voltage range is 5 to 10 V. The minimum channel length is 2 µm. More details on this technology are given in [6].

III. SYSTEM ARCHITECTURE

The system architecture is shown in Fig. 1. The front-end built with a-IGZO TFTs consists of an input chopper, a 2-stage preamplifier consisting of cascaded diode-connected load differential amplifiers (Fig. 2a), a reset integrator (Fig. 2b) and pseudo CMOS comparator with controllable hysteresis (Fig 2c). The input signal is AC-coupled before the input chopper. The preamplifier output is fed to the reset integrator. The differential signal current generated by the input TFT pair in the reset integrator discharges the load capacitors which are periodically reset. The time instants at which the integrator outputs fall below a specified level V_{ref} is monitored by two pseudo CMOS comparators with controllable hysteresis. The time delay in level crossing between both branches of the integrator output, T_{out}, is proportional to the input signal (Fig. 2d). The comparator outputs are then fed to an XOR to obtain a PWM output having a pulse width equal to T_{out} which is proportional to the differential input voltage, with an additional sign bit. More details on the circuit functionality are presented in next section.

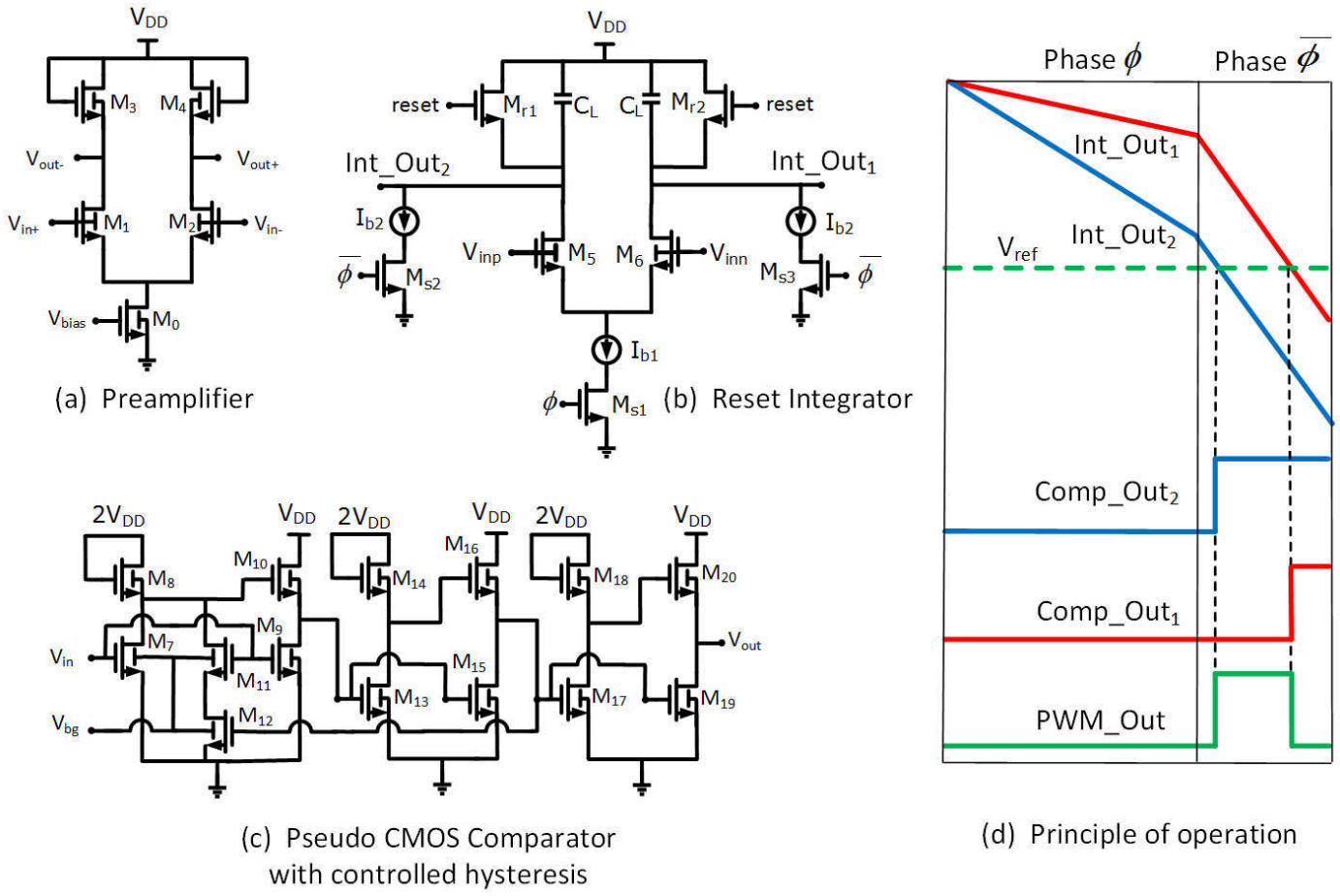

Fig. 2 Schematics of a) the preamplifier, b) the reset integrator, c) pseudo CMOS comparator and d) working principle of the reset integrator

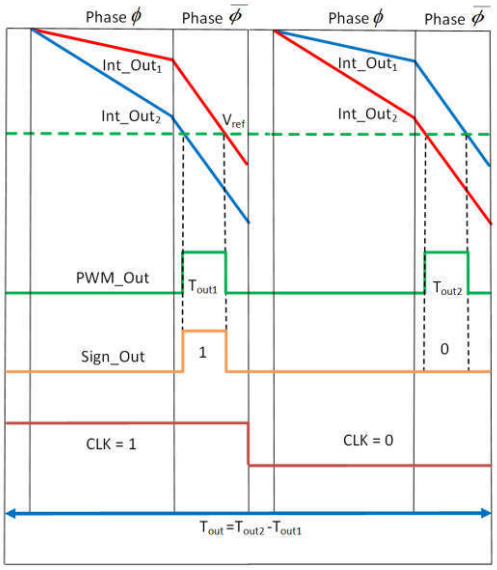

Fig 3 Principle of system level chopping

IV. Circuit Principle

The preamplifier consists of a diode-connected load differential amplifier (Fig. 2a). The input TFTs in the preamplifier have large (15000 μm^2) area to reduce the 1/f noise. The back gates of the current-source TFT M_0 and the load TFTs $M_{3,4}$ are connected to the source to increase the output resistance (Fig. 2a). Moreover, the back gates of the input TFTs $M_{1,2}$ are connected to the front gates to increase transconductance. The reset integrator (Fig. 2b) consists of a differential input pair $M_{5,6}$ and load capacitors C_L. In the first phase ϕ a signal-dependent discharging of the output capacitors occurs via the differential pair, while in the second phase $\overline{\phi}$ a constant current discharging takes place (Fig. 2b,d). The outputs of the integrator are connected to pseudo CMOS comparators which consist of three pseudo CMOS comparators connected in cascade. The output of the second inverter (Fig. 2c) in the cascade is connected to gate of M_{12} to provide positive feedback. This introduces hysteresis in the comparator, while the switching threshold of the comparator can be controlled through the back gate biasing V_{bg} of $M_{17,11,12}$ as will be shown in the next Section. The hysteresis is beneficial to suppress kickback noise from the integrator outputs.

The low-frequency noise is eliminated using an approach similar to correlated double sampling. An input chopper (CH_{in}) is used to alternate the connection between the inputs of the preamplifier periodically with a low frequency. The output signal is extracted by subtracting two consecutive samples, while taking into account the sign bit, as shown in Fig.3. When CLK is high the inputs of the preamplifier are connected in the usual way and a PWM output of pulse width T_{out1} is obtained. In the next phase CLK goes low, the inputs of the preamplifier are reversed and the PWM output of pulse width T_{out2} is obtained. By subtracting T_{out2} from T_{out1} (while keeping the sign bit in consideration), a final pulse T_{out} is

Fig 4 Layout of the presented system

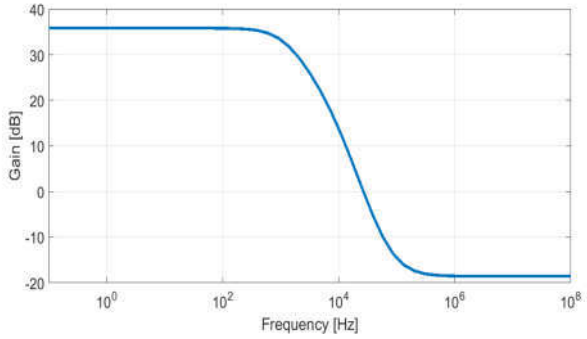

Fig. 5 Simulated frequency response of the preamplifier

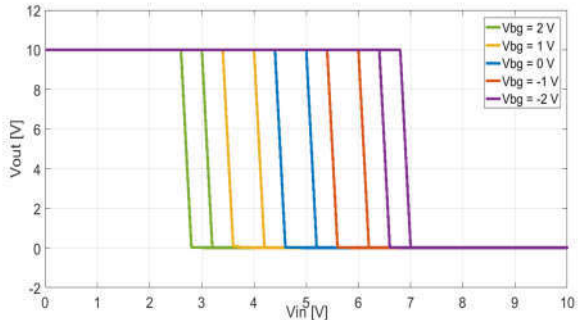

Fig. 6 DC transfer curve of the comparator implemented by cascading three pseudo-CMOS comparators. The threshold can be controlled by the back gate voltage V_{bg}

obtained. This approach cancels the quantities that present high correlation between two consecutive samples, i.e. offset and flicker noise, On the contrary the signal is doubled. This approach can be considered as system level chopping. One of the benefits of this technique over conventional chopping is that the preamplifier does not need to have a large bandwidth, as the signal is not up-modulated to the chopping frequency, but it is just sampled at a frequency which is at least twice the minimum Nyquist frequency.

V. Simulation Results

A. Circuit Characterization

Fig. 4 shows the layout of the frontend consisting of preamplifier, reset integrator and comparator. The total area is 6.5mm x 3mm. The system is simulated using in house models

TABLE I.
COMPARISON TO PRIOR LITERATURE

	JSSC'17 [1]	SSCL'18 [3]	ESSCIRC'18 [4]	ISSCC'17 [5]	This work[c]	
Technology	a-Si	a-IGZO	a-IGZO	a-IGZO	Dual Gate Self Aligned a-IGZO	
Architecture	Chopped Amplifier	Chopped Amplifier with Frequency Division Multiplexing	Chopped Amplifier + Reset Integrator	ADSM	Preamplifier + Reset Integrator + Pseudo CMOS Comparator	
Input domain	Voltage	Voltage	Voltage	Current	Voltage	
Output type	Analogue	Analogue	PWM	PWM	PWM	
Application	EEG	EMG	HR	Temperature Sensor	ECG	
Chopping Frequency	5 kHz	5-8 kHz	500 Hz	-	-	250 Hz
Integrated noise (BW)	2.3 μV_{rms} (100 Hz)	125-31.4 μV_{rms} (500 Hz)	186.3 μV_{rms} (200 Hz)	1.23 nA_{rms} (10 Hz)[a] 4.38 nA_{rms} (300 Hz)[a]	52.5 μV_{rms} (100 Hz)[d]	18.3 μV_{rms} (100 Hz)[d]
Current consumption (µA)	200	50	5.2	100	2.6	
Supply voltage (V)	55	26	10	20	10	
Power dissipation (mW)	11	1.3	0.052	2	0.026	
NEF	126.29	385.53[b]	1166.4	-	330.26	115.12
PEF	$8.77x10^5$	$3.86x10^6$ [b]	$1.36x10^7$	-	$1.09x10^6$	$1.32x10^5$
Area (mm^2)	90	11.2	52.5	27.9	19.5	

[a] Calculated from data in [5]
[b] Considering 31.4 μV_{rms} in 500 Hz bandwidth
[c] Simulated results
[d] Simulated with transient noise analysis

of the a-IGZO TFTs that include noise. Fig. 5 shows the simulated frequency response of the cascaded preamplifier. It achieves a gain of 35.8 dB in 1.1 kHz bandwidth with 2 µA current consumption from 10 V supply.

The current consumption in the integrator during the first phase ϕ is 250 nA while in the phase $\overline{\phi}$ it is 500 nA in each branch. Fig. 6 shows the simulated DC transfer curve of the comparator. Indeed, it can be seen from Fig. 6 that trip point of the comparator can be controlled through the back gate voltage V_{bg} applied to $M_{17,11,12.}$

B. Signal Reconstruction

The signal is reconstructed in the voltage domain from the PWM output signal. The reset frequency and its harmonics can be removed from PWM output by low-pass filtering in a 125 Hz band, which passes only the input signal and thus allows its reconstruction in the analogue domain. The reset frequency is 500 Hz while the CLK signal is half of the frequency of the reset signal. Fig. 7 shows the reconstruction of a 1 mV_{pp} ECG signal obtained in simulation using this method. The simulation includes a realistic noise model, and the ECG signal is still well recognizable.

An overview of the main circuit performance of our ECG interface and some relevant publications is given in Table I. The better performance compared to [4] is due to both TFT technology and circuit improvements. From the technology perspective, the self-aligned IGZO technology used in this work has a Hooge factor which is around five orders of magnitude better than the IGZO technology used in [4] and thus contributes less 1/f noise. From the circuit perspective, in this work a system level chopping has been used, which reduces the total input referred noise of whole system. The conventional chopping used in [4], on the contrary, was only applied to the preamplifier and the input of the integrator. Besides, the higher amplifier gain and larger input transconductance, both obtained thanks to the double gate TFT architecture, benefit the noise efficiency of the interface. The interface presented in this work achieves in simulation 52.5 μV_{rms} integrated input referred noise in the 1-100 Hz band without application of system level chopping. With 250 Hz system level chopping an input referred noise of 18.3 μV_{rms} is simulated in the 1-100 Hz band, resulting in NEF of 115.12. The total power consumption is 26.25 µW with 10 V supply voltage. This makes the simulated PEF of the presented interface 6.64x better than [1].

VI. CONCLUSION

This paper presents a low power flexible interface able to measure ECG and providing a PWM output. The output binary PWM waveform can be conveniently sent to a reader device using wireless communication and can be further converted to a digital representation using a simple counter. System level chopping is used to eliminate offset and flicker noise.

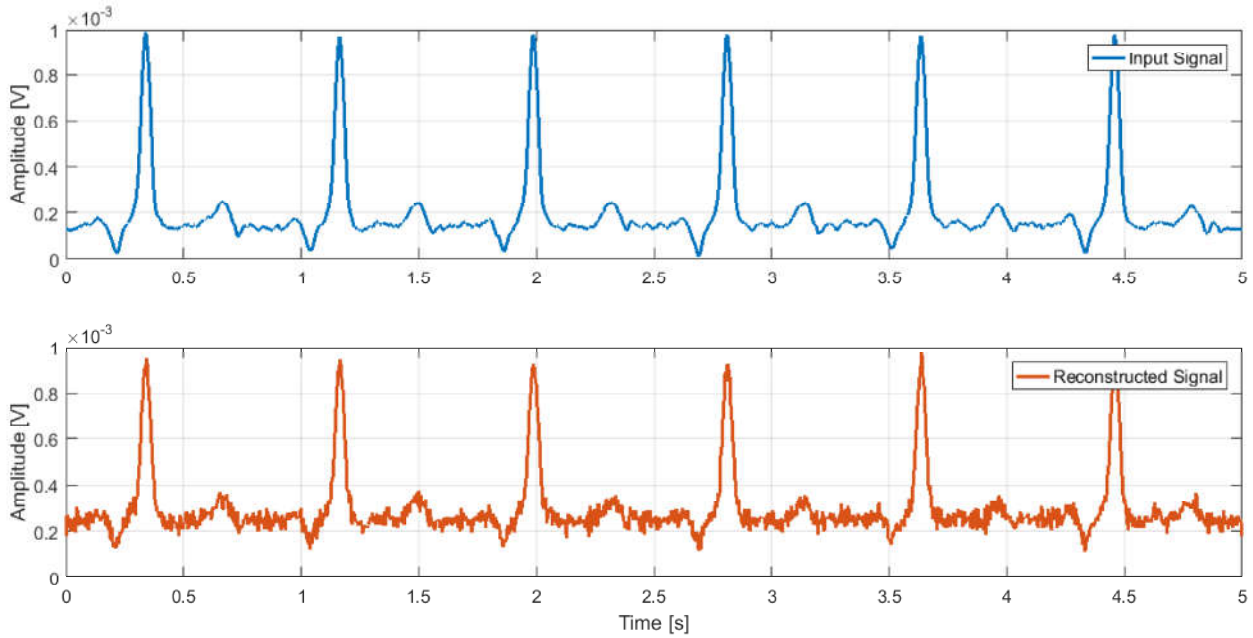

Fig. 7 Simulated response of the full system to an ECG source signal

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