1cm^2 sub-1V Capacitive-Coupled Thin Film ID-Tag using Metal-oxide TFTs on Flexible Substrate

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***Abstract*—In this paper a capacitive coupled radio-frequency identification tag fabricated on flexible thin-film substrate is presented. The antenna of the tag is monolithic integrated "on-chip". The footprint of the tag is defined by the size of the antenna, 1cm^2. The tag operated at 24V applied reader voltage at a frequency of 1MHz. The achieved data transmission speed of the thin-film tag is 5.8kbps. The technology is a unipolar indium gallium zinc oxide (IGZO) self-aligned transistor architecture.**

I. Introduction

Through the last years radio-frequency identification (RFID) [1]- [4] tags using organic or unipolar metal-oxide thin-film transistors (TFTs) have been demonstrated. The number of papers illustrate the great interest to TFT technologies for Internet of Everything (IoE) applications. This paper presents a thin-film tag with capacitively-coupled "on-chip" antenna, whereas most of the literature focuses on about inductive coupled chips and antennas. The 1cm^2 antenna can be realized using standard TFT stack metallization, in other words - monolithically, eliminating post-manufacturing tag assembly steps. Moreover, the short read range and compact size feature enhanced system security for data communication between tag and reader. This is exemplified in the following using a lab reader unit and a capacitive-coupled ID-tag (CAPID) on polyimide substrate. Building up on the early seminal work [1], many advancement of the state-of-art is demonstrated: tag size, on-chip antenna, reader voltage and power dissipation using a unipolar metal-oxide technology.

II. Technology

Self-aligned TFT architecture is chosen due to the non-overlapping source-drain to gate contacts [5], resulting in negligible parasitic capacitance between the contacts compared to etch-stop-layer (ESL) and back channel etch processes (BCE). Parasitic capacitance adds to the total input capacitance of the circuit chip [2] and the full CAPID tag. On a temporary glass carrier with a 25µm thick polyimide film, a humidity barrier is deposited and afterwards a thin layer IGZO is DC sputtered and patterned to define the active semiconductor area. Next, 100nm PECVD SiO_2 is deposited as a gate dielectric at a deposition temperature of 250^{o}C. Afterwards, 100nm Mo is added as gate-metal. The gate/dielectric stack is patterned within the same process step. We deposit 400nm CVD SiN to fulfill a double purpose: act as intermetal dielectric and hydrogen dope the IGZO in the areas not covered by the gate/dielectric stack. The contact holes for the Source-Drain (SD) contacts are opened and 100nm Mo is deposited and patterned to define the SD-contacts. The last step in the TFT process is a final anneal. All process steps in the backplane process stay below a thermal budget of 300^{o}C.

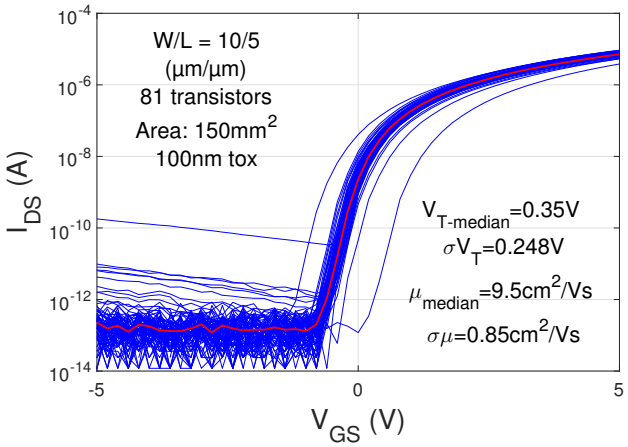

Fig. 1. TFT transfer curves of 81 self-aligned 10/5 (µm/µm) IGZO TFTs on polyimide foil over 150mm^2 wafer. Red line is the median ID-VGS.

In Fig.1 the transfer characteristics of 81 10/5 (µm/µm) TFTs are shown over 150mm^2 wafer. The median charge carrier mobility is μ=9.8cm$^2/Vs$ and the threshold voltage V_T=0.35V. Moreover, the standard deviation over a 150mm^2 wafer for V_T is respectively 248mV and of μ is 0.85cm$^2/Vs$.

III. Tag System and Results

In Fig.2 the building blocks of the CAPID reader and tag are shown. The reader needs a AC power source, a MΩ resistor as a demodulator and the emitting side of the electrodes that serve as antenna. The tag requires: the receiving side of the electrodes to act as antenna, a power management circuit to regulate the incoming voltage, the (12b) code generator (CG) to create the tag's ID, a clock generator to define the

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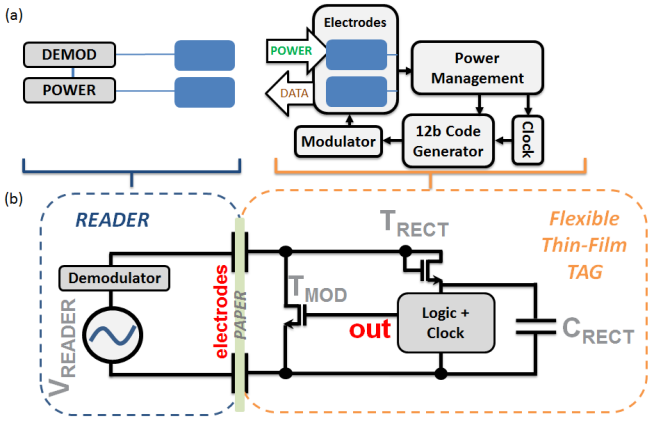

Fig. 2. The implemented reader and CAPID block diagram and detailed schematics of the system.

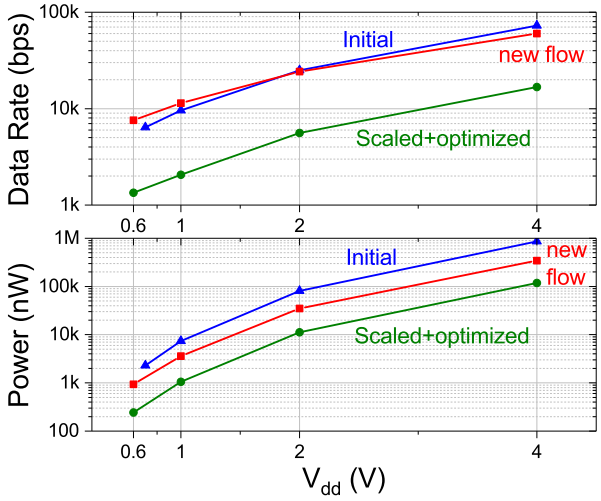

Fig. 3. Measured power dissipation and data rate of the initial, scaled+optimized and new flow CG circuits for various supplies.

speed of transmission, and a modulator to transmit the ID to the reader through the electrodes. The CG consists of 438 TFTs and the choice of logic gates is pseudo-CMOS topology [3], [4].

Due to the very limited power received at the tag's antenna, because of the capacitive coupling, low power techniques have been applied to the main power block, the CG [2]. The power dissipation of the CG is improved up to an order of magnitude compared to the initial CG designs, increasing the channel length (from 5µm to 10µm) of the logic gates and optimizing its width. The power dissipation is reduced to 243nW at 0.6V of power supply compared to 2.29µW, yet the data rate of the new CG is reduced up to 7 times.

Alternative, the power dissipation of the CG is improved by enhancing the digital flow and using more logic gates. In Fig. 3 the CG results are shown for various power supplies from 0.6V to 4V. The new design is now dissipating only half power, compared to the initial CG, but maintains the same speed. Further reduction of the power can be achieved

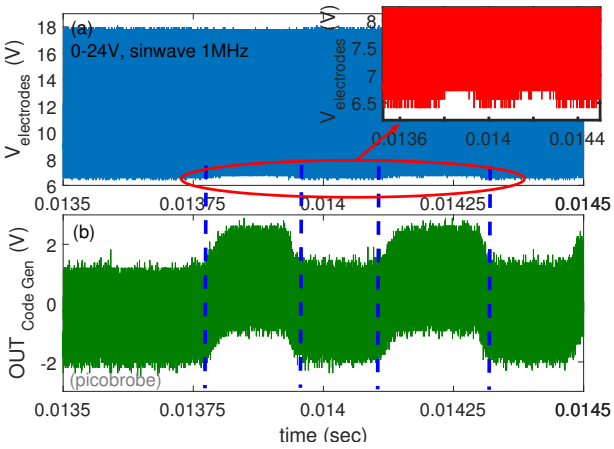

Fig. 4. (a) Measured modulation at the reader electrodes of a flexible CAPID tag (b) measured output of the same CAPID tag's CG.

by optimization the TFT sizes. Note also that the channel length of the new flow is smaller than the initial design.

In Fig.4 (a) the measurements of the flexible CAPID tag with a reader are shown (blue and red in zoom). The modulated signal at the electrodes (Fig.2) for an applied 24V AC signal is shown, verifying successful modulation of the applied signal from the generated code generator circuit. For verification of the code, the output of the CG is measured by a picoprobe matching the modulated signal at the electrodes as shown in Fig.4 (b). The data transmission rate is 5.8kbps.

IV. Conclusion

We have demonstrated a 1cm^2 capacitive-coupled tag-ID on flexible substrate. The main benefit of capacitive-coupled ID-tags is the enhanced security due to the short read distance compared to inductive-coupled tags. In addition, multiple advancements on cost, size, power and voltage is highlighted using unipolar self-aligned TFT technology compared to seminal capacitive-coupled work.

Acknowledgment

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