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Lab-STICC

EPIC

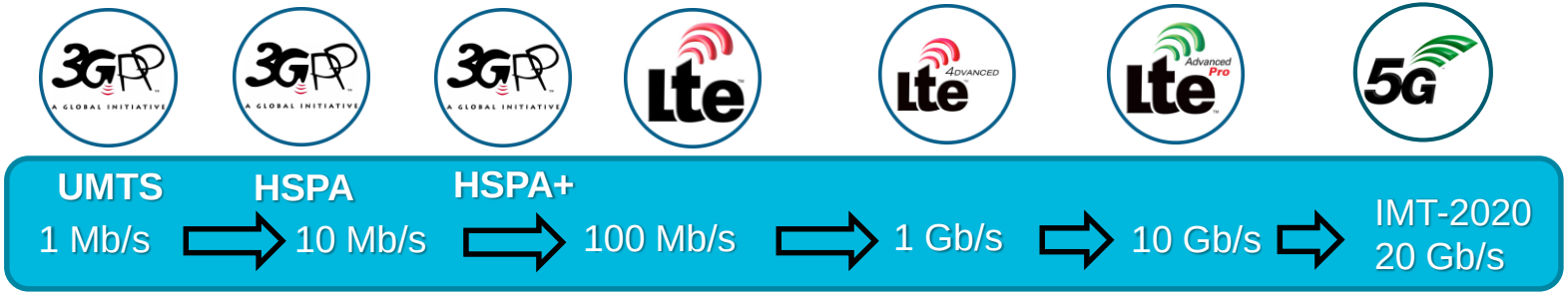
EPIC Grant Agreement No 760150

Channel coding for Tb/s wireless communications: insights into code design and implementation

Catherine Douillard

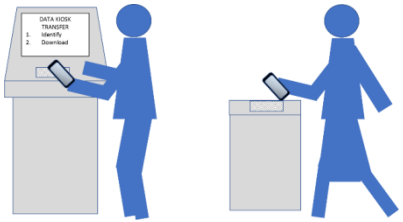
The International Symposium on Ubiquitous Networking - UNet'19
21 Nov. 2019 – Limoges - France

Wireless communication standards and throughput evolution

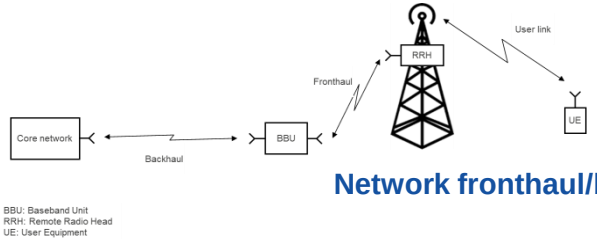


1Tb/s for B5G?

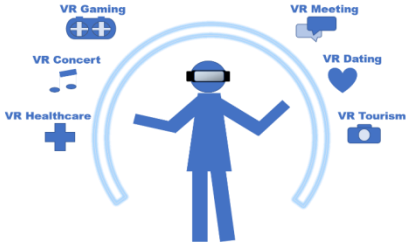
B5G high throughput (Tb/s) scenarios and applications



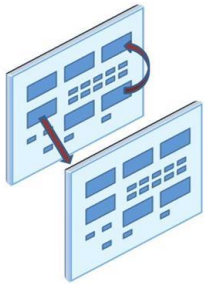
Data kiosk



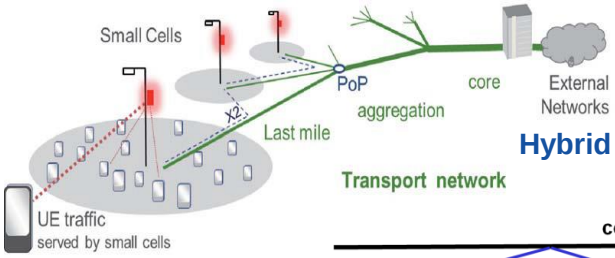
Network fronthaul/backhaul



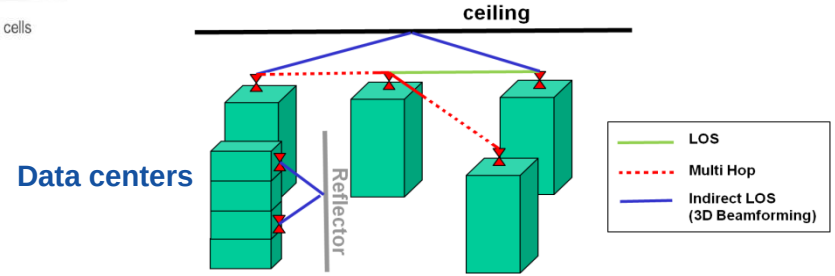
Mobile virtual/augmented reality



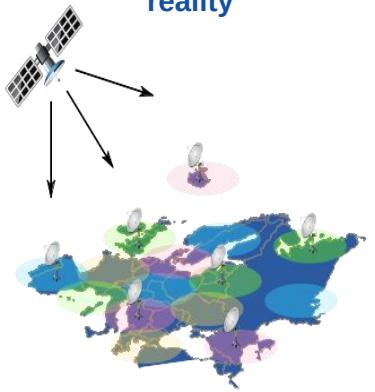
Wireless intra-device communication



Hybrid fiber-wireless links



Data centers



High-throughput satellites

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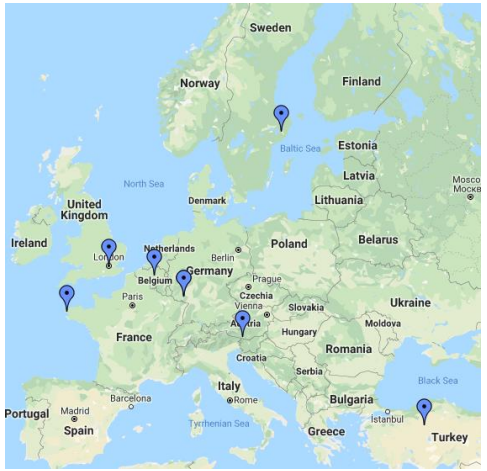
What about channel FEC coding?

Enabling Practical Wireless Tb/s Communications with Next Generation Channel Coding

H2020 EPIC (2017–2020)

The EPIC project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 760150.

General Project Information



- Project reference: **760150**
- Project start: **1st September 2017**
- Duration: **3 years**
- Total costs/EC contribution: **EUR 2.966.268,75**
- **Eight partners** from **seven** different **European countries:**
  - Creonic Gmbh , Ericsson AB, IMEC, IMT Atlantique, InterDigital Europe, Polaran, Technikon, Technische Universität Kaiserslautern
- **Mission:** EPIC aims to develop a new generation of Forward-Error-Correction (FEC) codes in a manner that will serve as a fundamental enabler of practicable beyond 5G wireless Tb/s solutions and also to develop and utilize a disruptive FEC design framework allowing to advance state-of-the-art FEC schemes.
- Website: www.epic-h2020.eu

Project Goals

- Design and implementation of **next generation FEC** for wireless Tb/s technology and **Beyond-5G systems**
- Advancement of **state-of-the-art channel codes** and **channel coding technology** for wireless Tb/s technology
- **Holistic design approach**: code design, decoding algorithms and efficient implementation on advanced silicon technologies in a cross-layer approach
- Validation and demonstration of new FEC technology and corresponding implementations as **virtual silicon tape-out**

Project methodology: phase 1

- Identification of relevant (B5G) Tb/s use-cases
  - Requiring new Forward Error Correction (FEC) coding techniques
  - Display a diverse set of FEC design challenges
- Key Performance Indicator (KPI) analysis
  - **System level requirements** (error rate, throughput, latency, power consumption, cost and volume)

    $\Rightarrow$ **FEC code level requirements** (area, area efficiency, energy efficiency and power density)
- Technology gap analysis
  - Comprehensive **state-of-the-art study**
  - **Scaling to 7 nm CMOS** technology
  - **Comparison** against FEC requirements

Key performance indicator (KPI) requirements

- **System-level KPIs** (error rate, throughput, latency, power, cost, flexibility)
  $\Rightarrow$ **FEC code-level KPIs** (error rate, throughput, latency, energy efficiency, area efficiency, and power density)

Use case	BER	Flexibility	Latency	Throughput (Gb/s)	Power (W)
Virtual reality	$\leq 10^{-6}$	high	0.5 ms	500	0.25
Data kiosk	$\leq 10^{-12}$	low	0.5 ms	1000	1
Intra-device commun.	$\leq 10^{-12}$	medium	100 ns	500	0.5
Backhaul	$\leq 10^{-13}$	medium	1 µs	250	1
Fronthaul	$\leq 10^{-12}$	medium	1 µs	1000	0.5
Data center	$\leq 10^{-13}$	medium	100 ns	1000	0.75
Hybrid fiber-wireless	$\leq 10^{-12}$	medium	200 ns	1000	1
High-speed satellite	$\leq 10^{-10}$	medium	10 ms	100-1000	0.5

FEC KPI requirements

Bounds due to realistic IC implementation contraints

FEC KPI bounds $f_{CK} \leq 1$ GHz	
Area limit	10 mm²
Area efficiency limit	100 Gb/s/ mm²
Energy efficiency limit	~1 pJ/bit
Power density limit	0.1 W/mm²

Code families

Capacity approaching coding schemes in recent/emerging wireless standards

- Turbo codes (4G⁺)
- LDPC codes (5G NR)
- Polar codes (5G NR)

Perform close to Shannon limit

Efficient implementations exist

State of the art (SoA) and gap analysis

- Identify **SoA of high-speed turbo**, **LDPC** and **polar decoders**
- **Scale to 7 nm CMOS** technology node
  - E. g. 28 nm to 7 nm technology ⇒ Area ÷12
    ⇒ Energy per bit ÷4
    ⇒ Clock speed ×3 (with a limitation at 1 GHz)
- **Scale to the desired throughput**
- Analyze the **gap to the target** in terms of FEC KPIs
- Deduce the fundamental **challenges in enabling wireless Tb/s link technology** for each code family

SoA and gap analysis: examples (scaled to 7 nm)

	Use case	SoA Turbo Decoder								
	Backhaul	[65] [66]	[67]	[68]	[68]	[69]	[70]	[76]	[77]	[83]
Code Flexibility		LTE-A	LTE-A	LTE-A	LTE-A	LTE-A	*K*= 4096	LTE	LTE-A	*K*= 6144
Architecture		PMAP	PMAP	PMAP	PMAP	PMAP	PMAP	XMAP	XMAP	FPMAP
Nb decoders		99	32	16	16	29	34	89	151	2
Nb max it.		5.5	6.0	8.0	5.5	6.0	8.0	5.5	6.0	39.0
Throughput (*Gb/s*)	250	244.6	152.9	58.2	84.7	92.8	222.5	247.7	251.7	130.7
Area (*mm²*)	10.0	9.9	9.9	9.7	9.7	9.7	10.0	10.0	6.9	8.8
Power (*W*)	0.9	38.9	n/a	5.3	3.6	10.2	30.8	25.8	30.7	13.3
Area eff. (*Gb/s/mm²*)	25	24.6	15.4	6.0	8.8	9.6	22.3	24.9	36.4	14.9
Power dens. (*W/mm²*)	0.09	3.91	n/a	0.55	0.38	1.05	3.08	2.59	4.44	1.51
Energy eff. (*pJ/bit*)	3.6	158.9	n/a	91.1	43.1	110.0	138.4	104.2	122.2	101.5
Latency (*µs*)	1	2.5	1.3	1.7	1.2	1.9	0.6	2.2	3.7	0.1
Frequency (*MHz*)	1000	1000.0	1000.0	1000.0	1000.0	1000.0	818.0	1000.0	1000.0	413.7

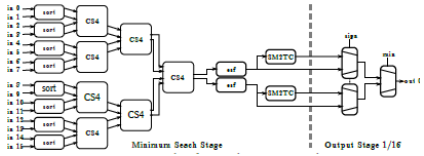
	Use case	SoA LDPC Decoder					
	Virtual Reality	[85]	[87]	[89]	[90]	[96]	[97]
		LDPC-BC	LDPC-BC	LDPC-BC	LDPC-BC	LDPC-CC	LDPC-CC
		partially	fully	unrolled	unrolled	pip. WD	pip. WD
Num. of Decoders	-	24	17	2	1	42	21
Throughput (Gb/s)	500	502.5	519.6	760.0	574.2	502.7	503.5
Area (mm²)	9.1	0.6	1.7	0.4	2.2	1.5	0.6
Power (W)	0.2	0.6	3.2	0.4	2.1	1.0	0.7
Area Eff. (Gb/s/mm²)	54.8	874.5	302.2	1880.4	265.9	325.0	820.5
Pow. Den. (W/mm²)	0.03	1.0	1.9	1.0	1.0	0.6	1.1
Energy Eff. (pJ/bit)	0.48	1.2	6.2	0.5	3.6	2.0	1.3
Latency (µs)	500	0.03	0.06	0.03	0.10	0.34	NA
Freq. (MHz)	1000	1000.0	1000.0	714.0	1000.0	1000.0	1000.0

Conclusions

- Microelectronics progress alone cannot keep pace with the requirements
- Biggest challenge for the 3 code classes: **power consumption** and **related KPI** (energy efficiency, power density)
  - Especially when flexibility (packet size, code rate) is required

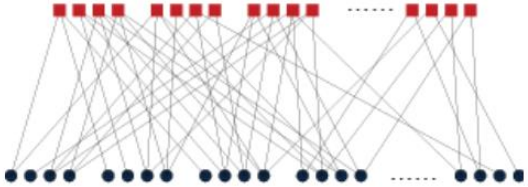
1Tb/s FEC Challenges

Goals: ~1pJ/bit, ~100mW/mm², ~1000 bits in 1ns



Energy efficient high throughput architectures

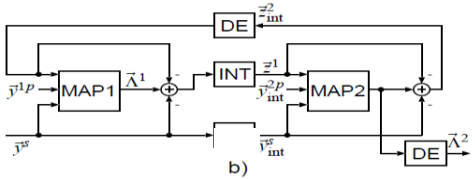
- Large locality and regularity, large parallelism

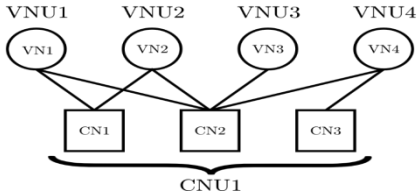


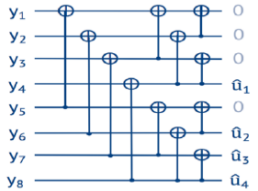
Information theory

- Irregularity, Iterative/sequential decoding algorithms

Code	Decoding algorithms	Parallel vs. serial	Locality	Compute kernels	Transfers vs. compute
Turbo code LDPC code Polar code	MAP Belief propagation Successive cancelation/List	serial/iterative parallel/iterative serial	low (interleaver) low (Tanner graph) high	Add-Compare-select Min-Sum/add Min-Sum/add/sorting	compute dominated transfer dominated balanced





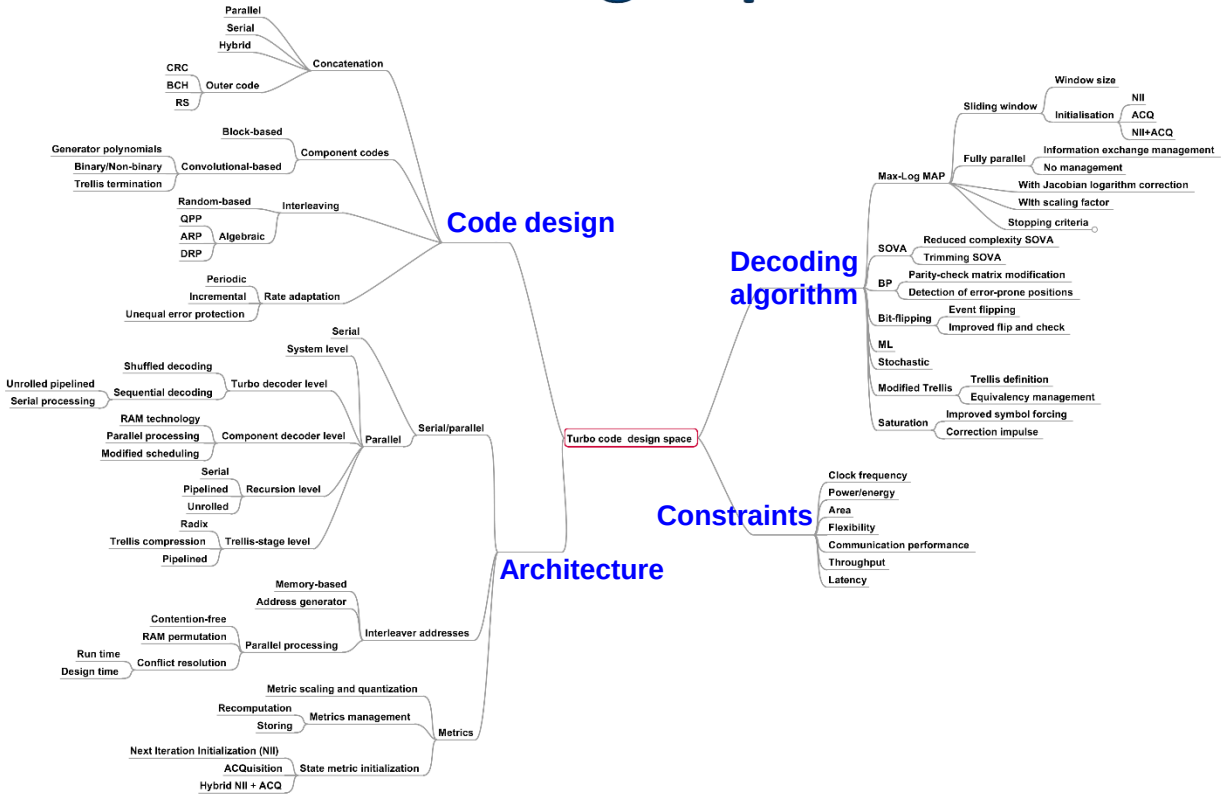


Bridging the gap between SoA and EPIC goals

- Necessity to explore the interrelation between **code structure**, **decoding algorithms**, **error correction performance** and **implementation**
- Deliver new code structures, decoding algorithms and architectures

  $\Rightarrow$ **Design Space Exploration** under EPIC KPIs
  - Set up design space for each code class
  - Prune the design space under EPIC KPI constraints
  - Select most promising candidates to derive new solutions to meet the 1Tb/S challenges
- Example: turbo codes
  - Turbo codes are the most challenging codes

Example: turbo code design space



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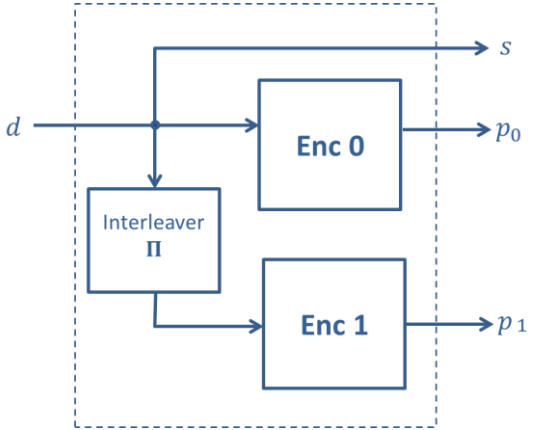
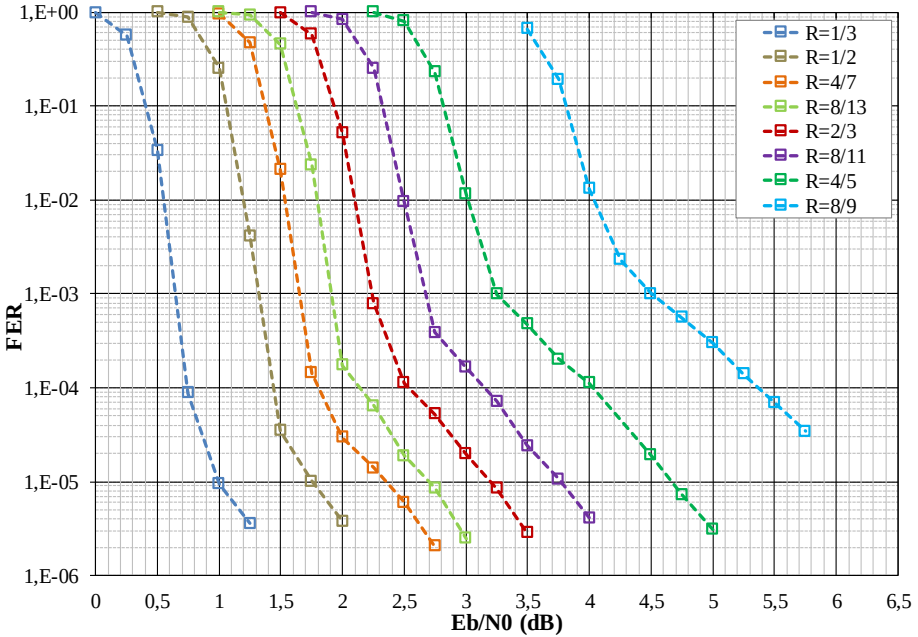
Towards 1Tb/s decoding of turbo codes

EPIC Grant Agreement No. 760150

Why is LTE FEC code not suitable for B5G communication systems?

- **Low error rates**
  - LTE turbo code (TC) cannot guarantee frame error rates (FER) lower than 10^{-5} for high code rates





K = 4032 bits
Scaled Max-Log MAP decoding
8 iterations
AWGN channel
QPSK modulation

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Why is LTE FEC code not suitable for B5G communication systems?

- **High throughput**
  - **QPP interleaver is contention free**
    - Maximum parallelism degree 64
    - Parallel processing on multiple sub-decoder cores
    - Throughput: a few Gb/s with nowadays ASIC technologies, a few tens of Gb/s with next technology nodes (7 nm)
  - **Achieving beyond 100 Gb/s requires**
    - Pipelining the Max-Log-MAP recursions
    - Unrolling the iterations ⇒ hardwired interleavers/de-interleavers
  - **Shortcoming of LTE QPP interleaver for very high throughputs:**
    - No common parameters for different block sizes
    - Issues with place and route of the interleaving network for all sizes

1. Code design

- Focus on interleaver design
- Joint puncturing pattern/interleaver design to support incremental redundancy (flexibility)

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Interleaver design

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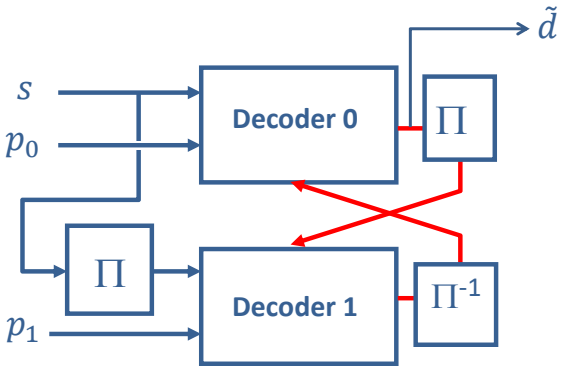
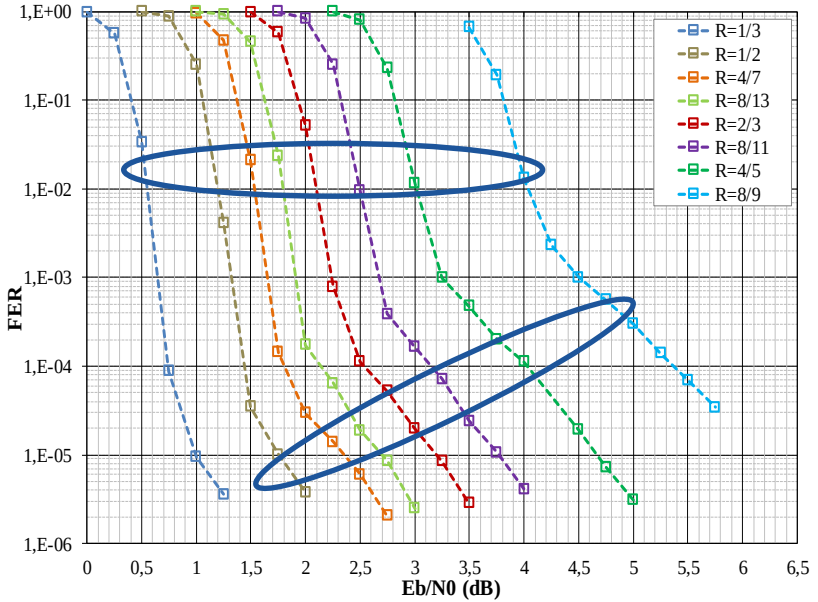
Turbo codes interleaver design

The interleaver is a fundamental component of the turbo code structure

1. Minimum Hamming distance
2. Correlation in the decoding process





Focus on the ARP (Almost Regular Permutation) interleaver model

Regular Interleaver for tail-biting trellises

$$\Pi(i) = (P \cdot i) \bmod K$$

ARP Interleaver

$$\Pi(i) = (P \cdot i + S(l)) \bmod K$$ [1]

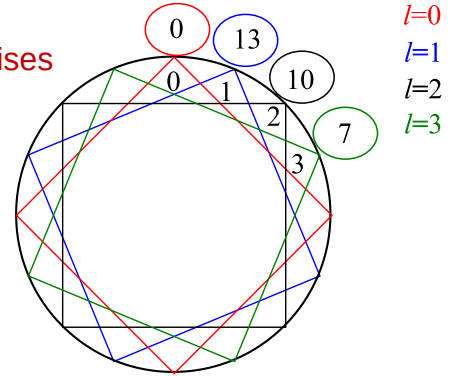
Layer number

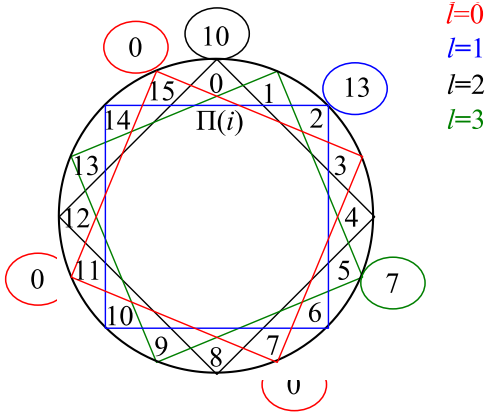
$$l = \mathrm{i} \bmod Q \qquad Ex.\ Q = 4$$

Shift value

$$S(l) = T_l + B_l Q$$

$$\begin{cases} T_l \in (0, \dots, Q-1) \\ B_l \in (0, \dots, (K/Q)-1) \end{cases}$$





NB: QPP interleavers (LTE) can be expressed as ARP interleavers [2]

[1] C. Berrou, Y. Saouter, C. Douillard, S. Kerouedan, Michel Jezequel, "Designing good permutations for turbo codes: towards a single mode", ICC 2004, Jun 2004, Paris, France.

[2] R. Garzón Bohórquez, C. Abdel Nour, and C. Douillard. “On the Equivalence of Interleavers for Turbo Codes,” *IEEE Wireless Communication letters,* vol. 4, no.1, Feb. 2015.

Joint design of interleaver parameters and puncturing patterns

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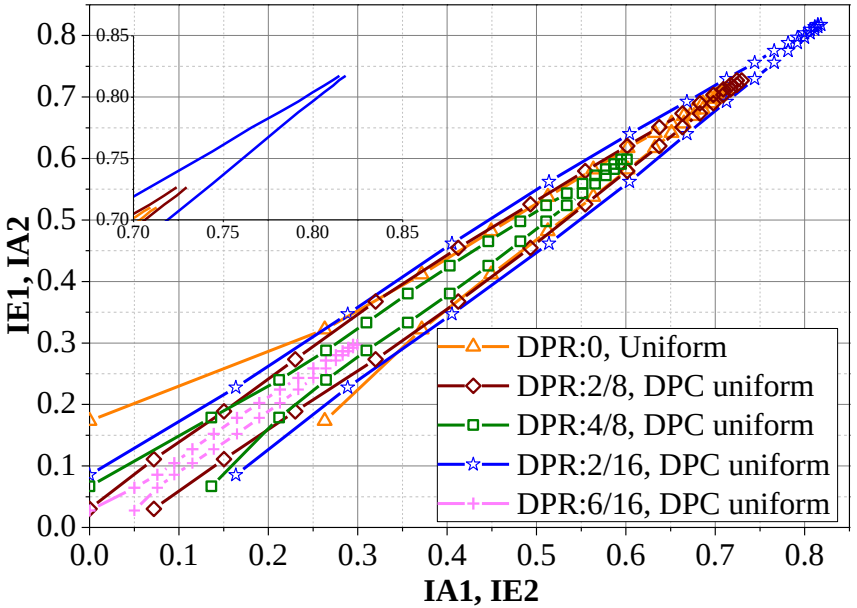
1. Puncturing mask selection using EXIT charts

Application example: *R* = 2/3

Data Puncturing Ratio (DPR)	*Coding rate of constituent code (R_c)*	Puncturing mask: Data/Parity
0	0.8	11111111/10001000
2/8	0.88	01111110/11000001
4/8	1	11001100/10011001

Select the systematic data puncturing ratio that maximizes mutual information in the decoding process

***R* = 2/3, *K*=1504**



Modified EXIT chart (measured MI) for the different *DPR* values

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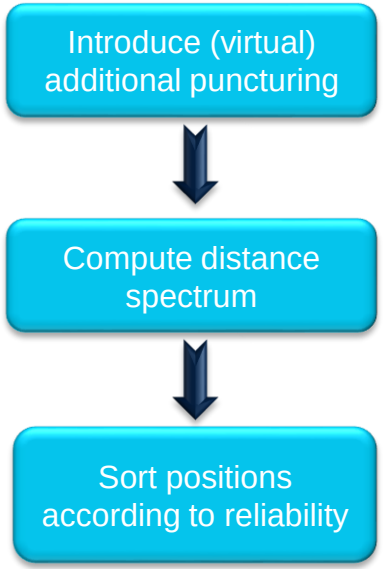
2. Sorting of non-punctured data in the puncturing pattern

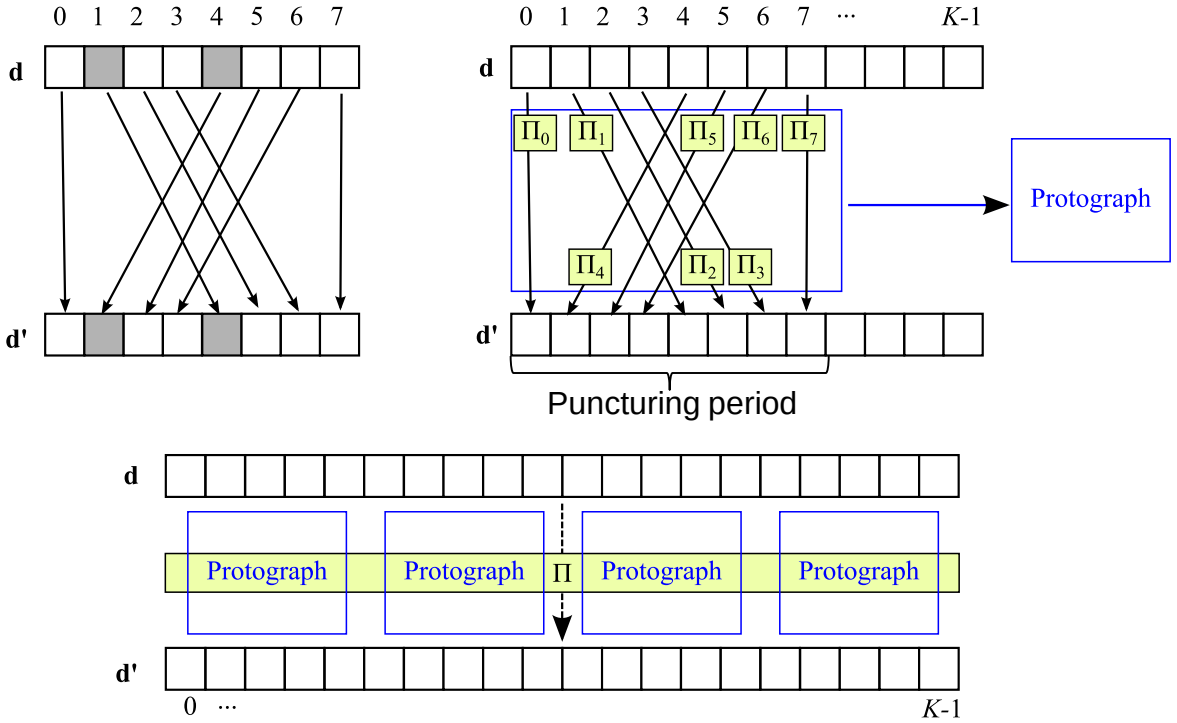


Application example: *R* = 2/3 & *K* = 1504

DPR	Puncturing Mask: Data/Parity							
	0	1	1	1	1	1	1	0
2/8	1	1	0	0	0	0	0	1

	A_0	A_1	A_2	A_3	A_4	Data puncturing mask
1	0	0	1880	1060320	465121494	00111110
2	0	0	4000	2003510	671273377	01011110
4	0	4	3015	1151175	294778989	01101110
6	0	8	140	2229	35176	01110110
3	0	2	2256	1275364	320347391	01111010
5	0	4	3019	1152688	148963135	01111100

3. Cross connection strategy: protograph-based (PB) interleaver [3]



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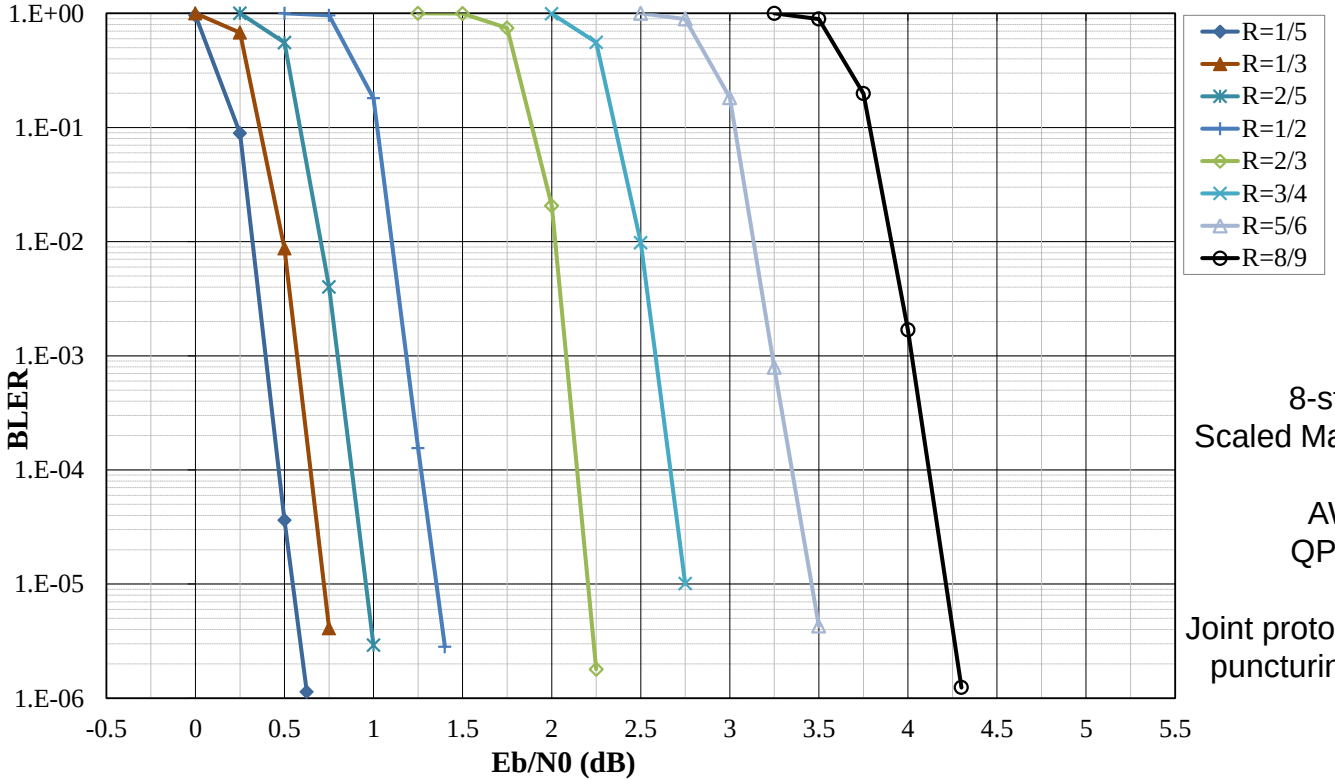
[3] R. Garzon, C. Abdel Nour, C. Douillard, “Protograph-Based Interleavers for Punctured Turbo Codes”, *IEEE Trans. Commun.*, vol. 66 no 5 , May 2018.

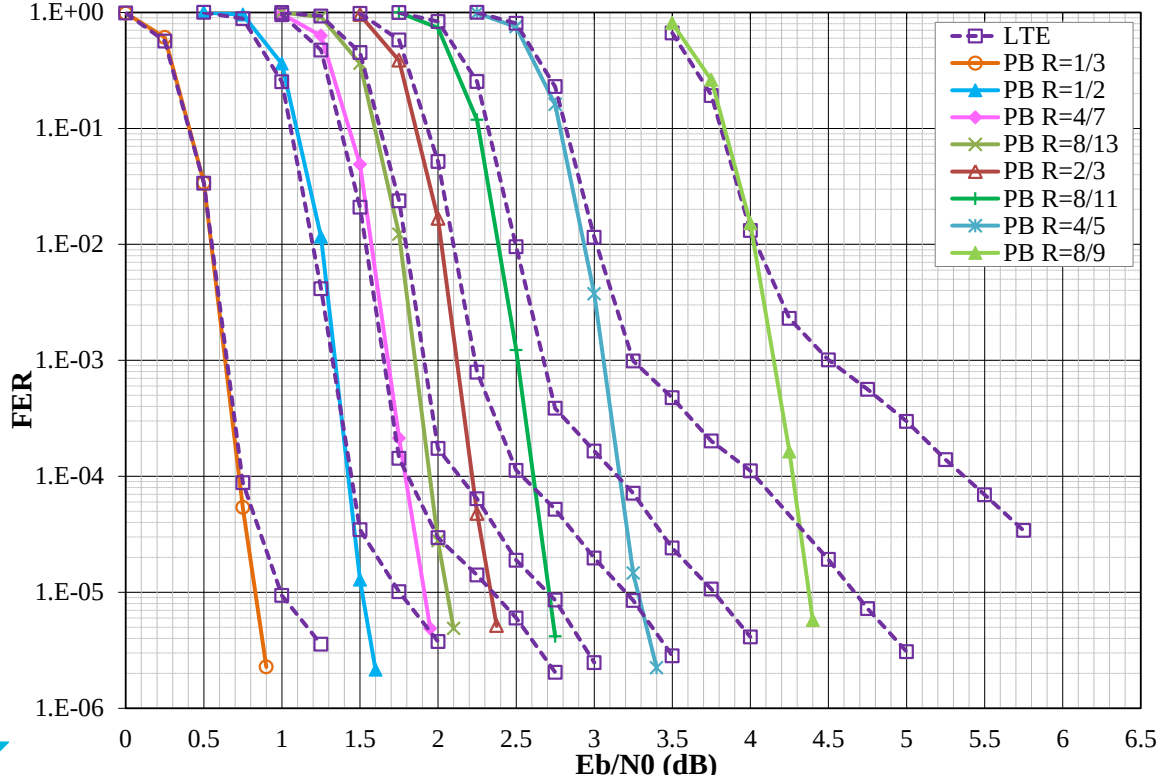
Simulation results



K=8000 bits
8-state turbo code
Scaled Max-Log MAP decoding
8 iterations
AWGN channel
QPSK modulation

Joint protograph interleaving and puncturing for each code rate

Error rate performance of Rate-Compatible TC with PB interleaver for *K* = 4000 bits



K=4000 bits
8-state turbo code
Scaled Max-Log MAP decoding
8 iterations
AWGN channel
QPSK modulation

Joint protograph interleaving and puncturing for code rate R=8/9
IR support

Error floor issue: solved!

2. Decoder architecture

New high-throughput frame flexible architecture

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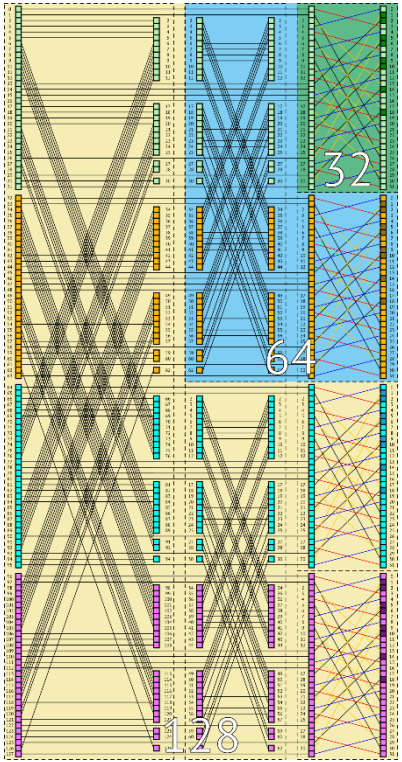
Advantages of the proposed interleaver for high throughput: Flexible ARP interleavers

ARP Interleaving :

$$\pi(i) = P * i + S[i \bmod Q] \bmod K$$

- Let: P = 9, S = [3,13,27,5] and Q = 4
- Information frame size K = 32, 64, 128 bits
- Larger sizes (multiple of) can be constructed from lower sizes with a small overhead
- Regular interleaver for every value of S

Key takeaways:
- Large amount of identical connections
- Simpler interconnect
- Regular structure allows frame size flexibility at minimum hardware cost
- Periodic puncturing
- Improved error correction performance



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Max-Log-MAP decoding

$$\bar{\gamma}_{k,k+1}(x) = \bar{\Lambda}_{u,k}^{a,x^s} + \sum_{i=0}^{\eta-1} \bar{\lambda}_k^{(i)} x^{(i)}$$

Branch Metrics

$$\bar{\alpha}_k^m = \max{}^*{}_{\forall m'} \left(\bar{\alpha}_{k-1}^{m'} + \bar{\gamma}_{k-1,k}^{m',m} \right)$$

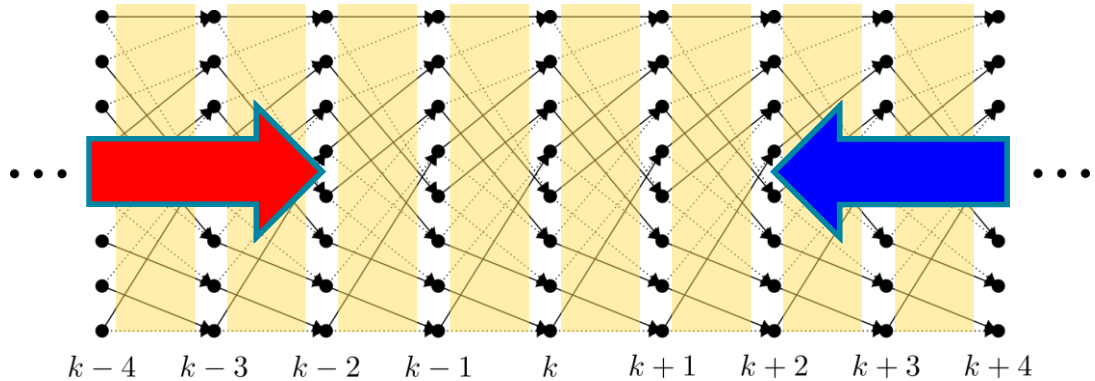
Forward Recursion

$$\bar{\beta}_k^m = \max{}^*{}_{\forall m'} \left(\bar{\beta}_{k+1}^{m'} + \bar{\gamma}_{k,k+1}^{m',m} \right)$$

Backward Recursion

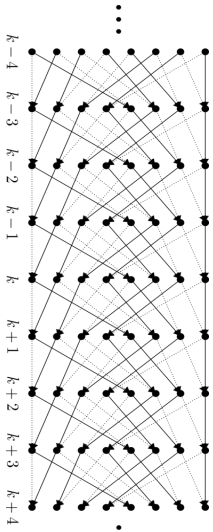
$$\Lambda_k^{(i)} = \max_{\forall m,m' | u_k^{(i)}=0}{}^* \left(\bar{\gamma}_{k,k+1}^{m,m'} + \bar{\alpha}_k^m + \bar{\beta}_{k+1}^{m'} \right) - \max_{\forall m,m' | u_k^{(i)}=1}{}^* \left(\bar{\gamma}_{k,k+1}^{m,m'} + \bar{\alpha}_k^m + \bar{\beta}_{k+1}^{m'} \right)$$

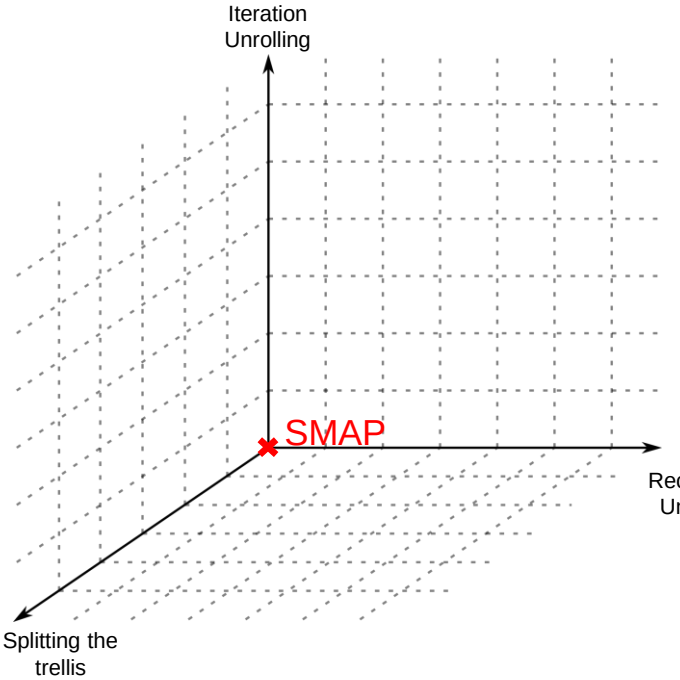
Soft Output

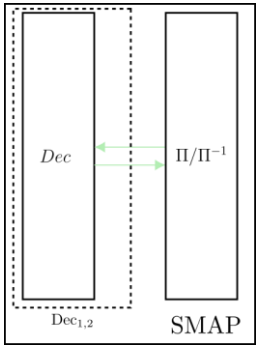


From Mb/s to Gb/s: Hardware architectures

Serial MAP (SMAP): One serial ***max-Log-MAP*** decoder functioning as Dec_1 / Dec_2 alternatingly







Mb/s

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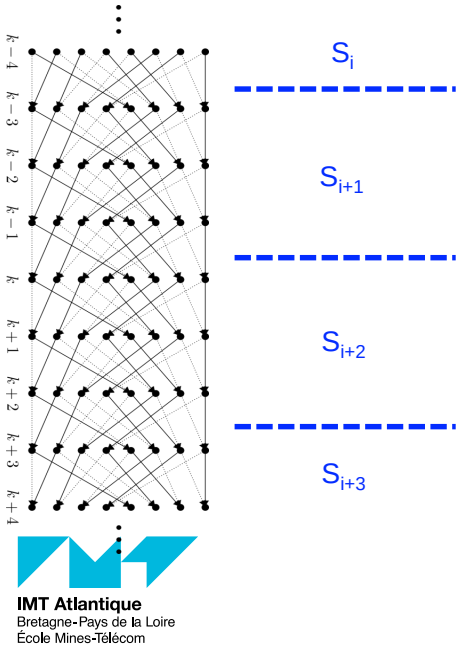
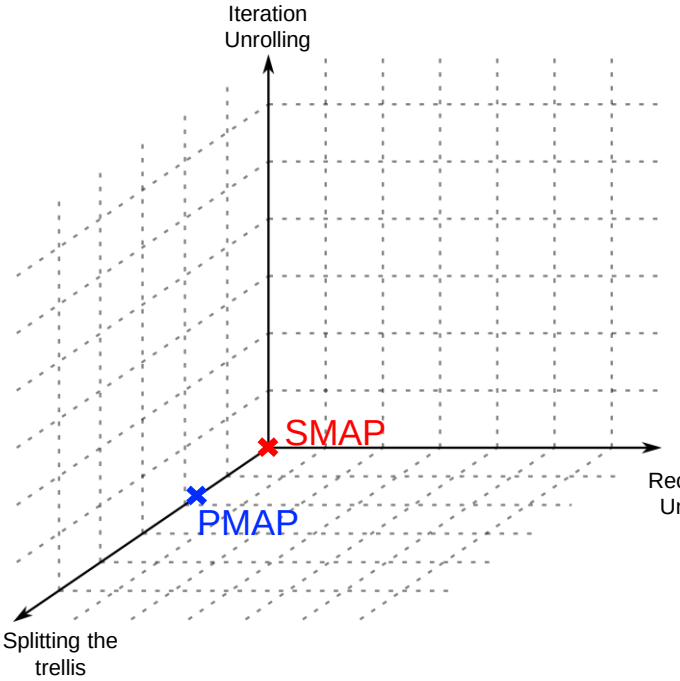
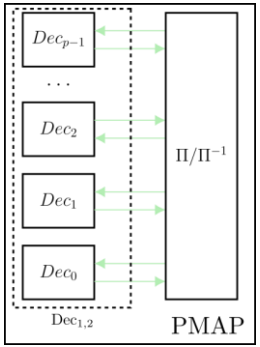
From Mb/s to Gb/s: Hardware architectures

Parallel MAP (PMAP): P serial ***max-Log-MAP*** decoders processing different parts of the trellis







1-5 Gb/s

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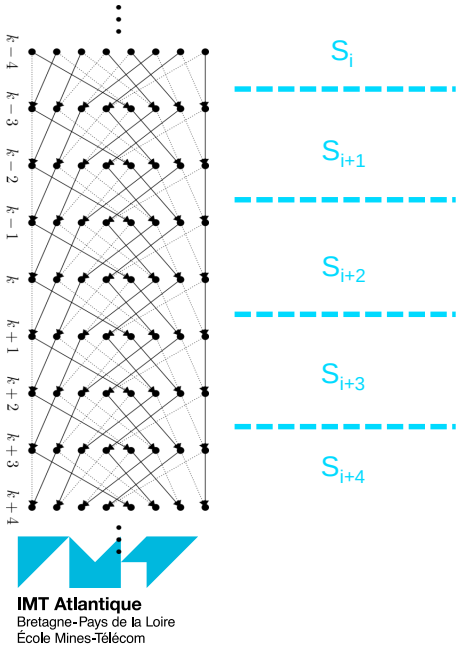
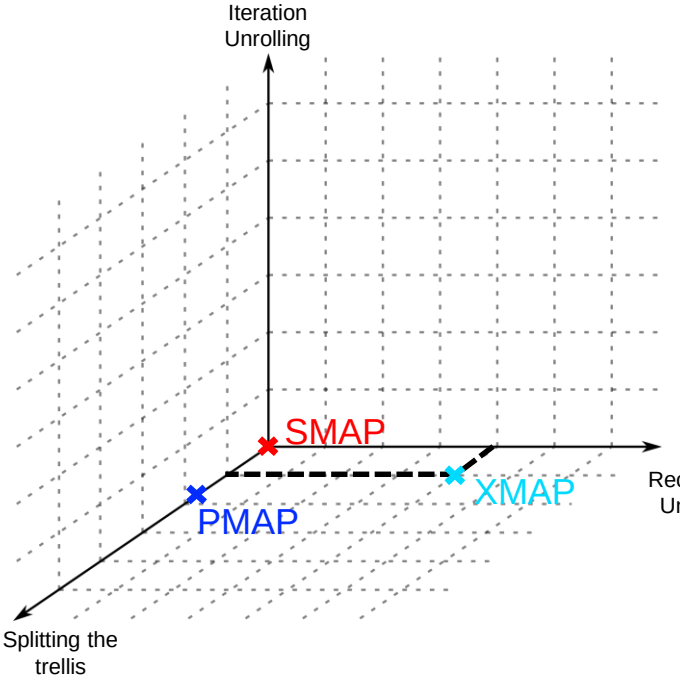
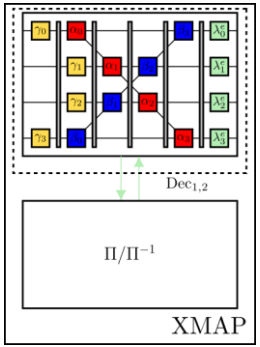
From Mb/s to Gb/s: Hardware architectures

Pipelined MAP (XMAP): Pipelined decoder processing parts of the trellis in a X-shaped pipeline







1-5 Gb/s

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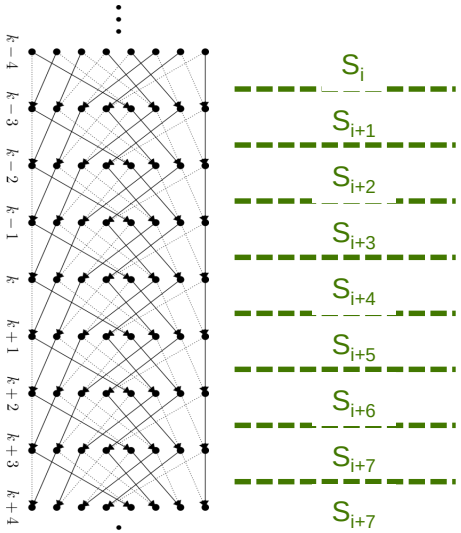
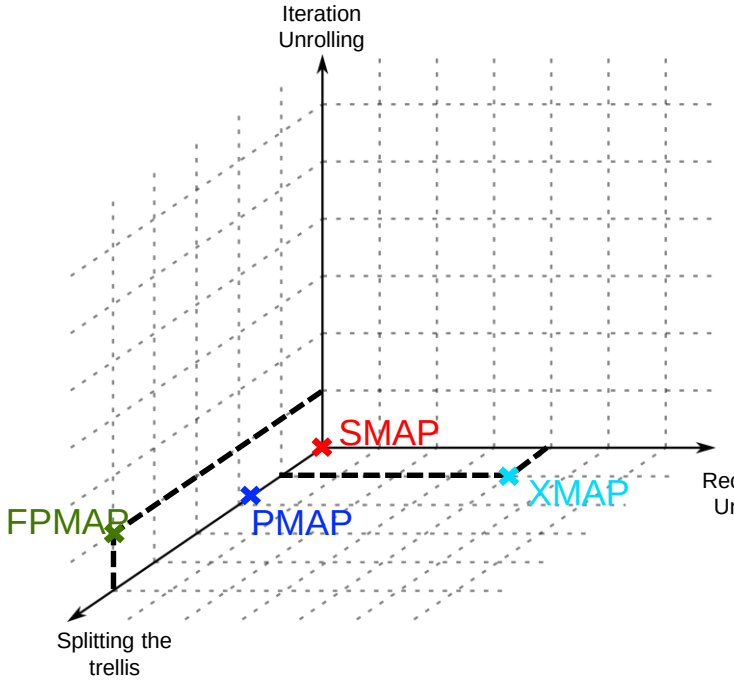
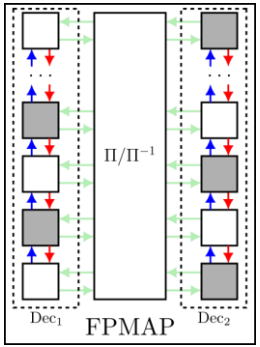
From Mb/s to Gb/s: Hardware architectures

Fully Parallel MAP (FPMAP): Extreme case of the PMAP; hardware instances for both $Dec_{1,2}$







10-40 Gb/s

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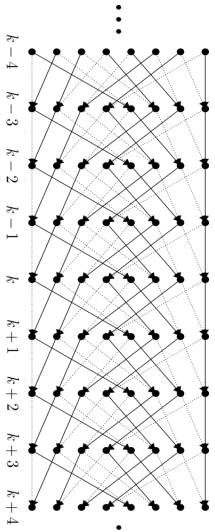
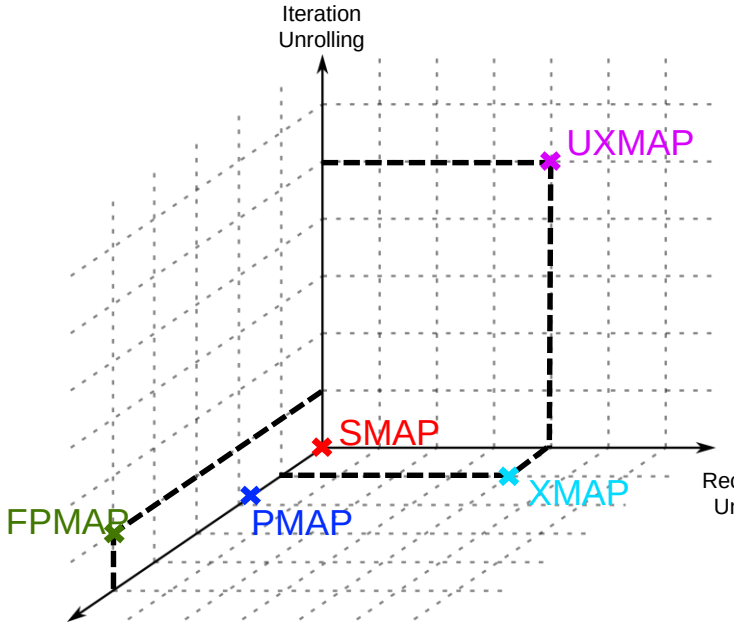
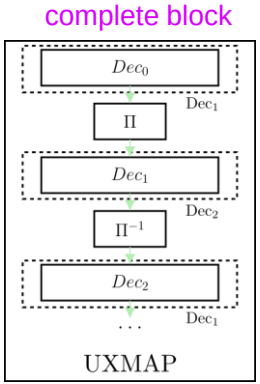
From Mb/s to Gb/s: Hardware architectures

(NEW) Iteration Unrolled Fully Pipelined XMAP (UXMAP): Extreme case of the XMAP







> 100 Gb/s

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[4] S. Weithoffer, , C. Abdel Nour, N. Wehn, C. Douillard, and C. Berrou, "25 Years of Turbo Codes: From Mb/s to beyond 100 Gb/s," in *Int. Symp. on Turbo Codes and Iterative Inf. Process. (ISTC),* Hong-Kong, Dec. 2018.

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New hardware architecture: UXMAP

Fully Pipelined Iteration Unrolled Turbo Decoder (UXMAP)

Functional Units:

Channel value pipeline ■

Branch Metric Units ■

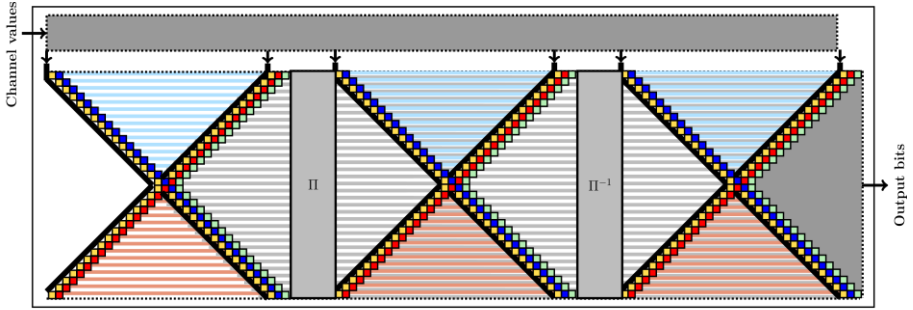
Recursion Units ■ ■

State metric pipelines ■ ■

Branch Metric Re-computation ■

LLR Units ■

Pipelines, π and π^{-1} (hardwired)



- Fully rate compatible
- Uses branch metric re-computation and radix-4 processing to reduce pipelize sizes
- Streaming processing ⇒ one decoding result per clock cycle!

Turbo code case: what's next ?

- **Code design**
  - Study of non-binary turbo codes
  - Spatially-coupled turbo codes
- **Decoding algorithm**
  - Revisiting the decoding algorithm : local SOVA
  - Decoding on the dual trellis
- **Decoder architecture**
  - Pipelined and iteration unrolled architectures

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