Terabits-per-Second Throughput for Polar Codes

Altuğ Süral, E. Göksu Sezer, Yiğit Ertuğrul,
Orhan Arıkan and Erdal Arıkan

Bilkent University and Polaran Ltd.
Ankara, Turkey

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India's moon landing suffers last-minute communications loss

Prime minister Narendra Modi consoles scientists distraught as complex mission goes awry

▲ An ISRO employee reacts after the communication and data were lost from the Vikram Lander. Photograph: Jagadeesh Nv/EPA

Source:

https://www.theguardian.com/world/2019/sep/06/indias-moon-landing-suffers-last-minute-communications-loss

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  - drone-based communications
  - virtual and augmented reality
  - chip-to-chip and intra-chip communications
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- Contribute to the rapidly emerging standardization studies
  - IEEE 802.3ba Ethernet
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  - IEEE 802.11bb Light Communication TG (Li-Fi)
- Provide strong error-resilience for those applications using **polar codes**

What are the requirements of Tb/s FEC?

The ASIC design experts in H2020 EPIC project predicts Tb/s FEC throughput within the limits of KPIs [epi18].

Name of KPI	Requirement
Technology	7nm
Throughput	1 Tb/s
Clock freq.	≤ 1 GHz
Area	≤ 10 mm^2
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Power den.	≤ 0.1 W/mm^2
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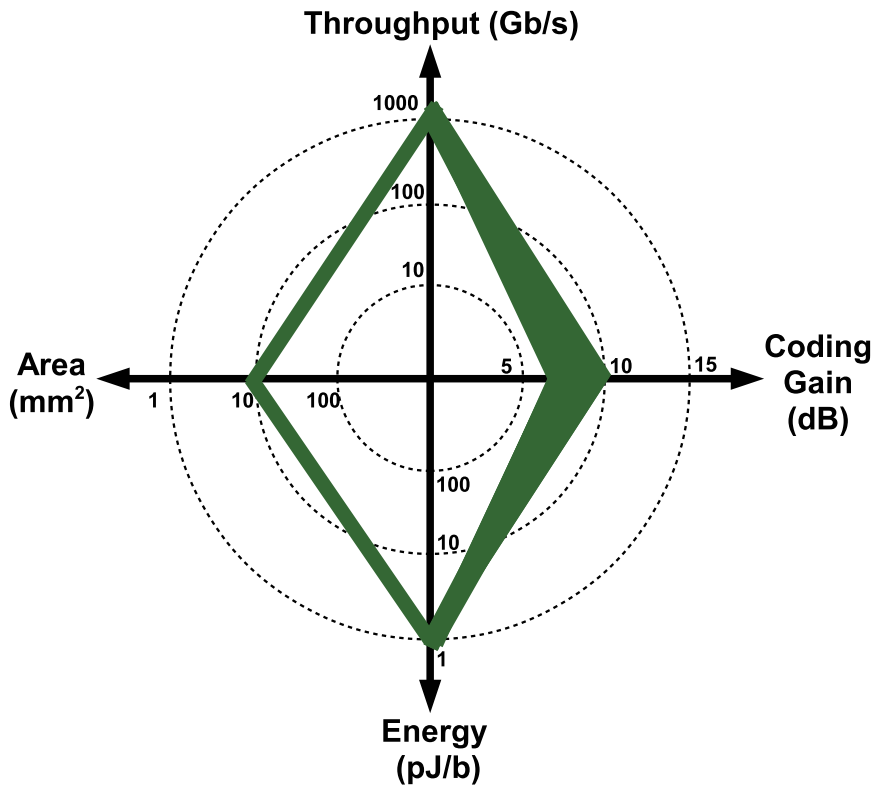

Challenges for Tb/s FEC

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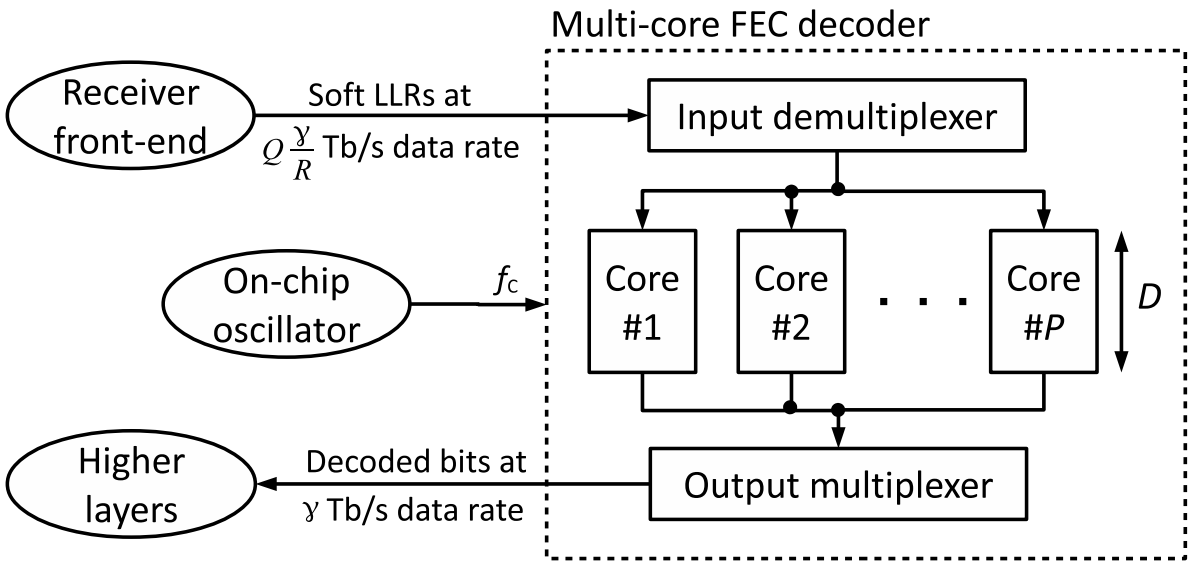

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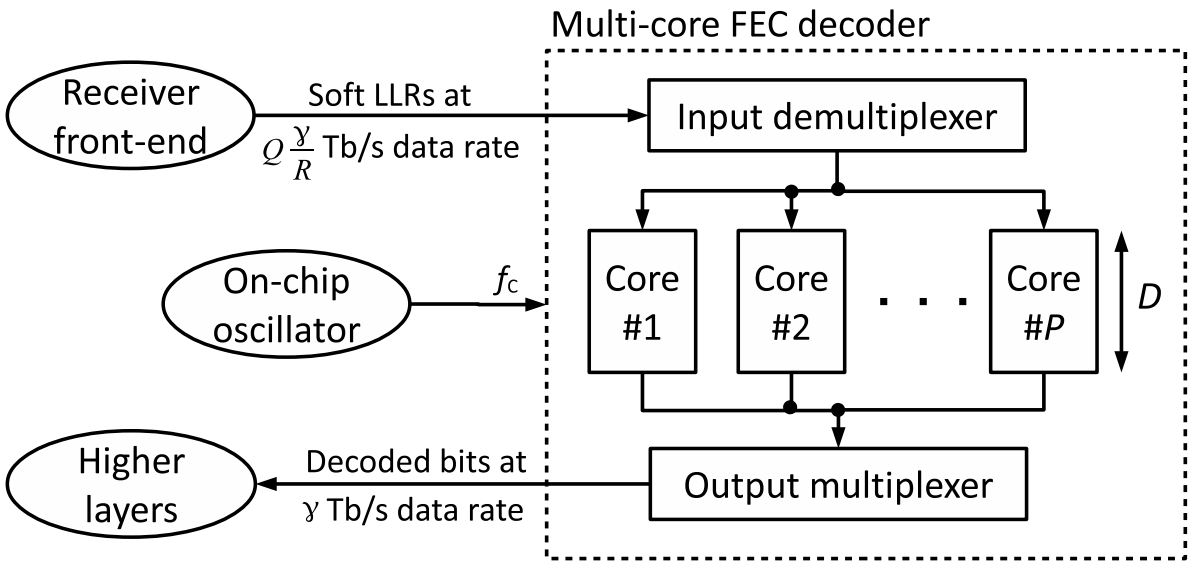

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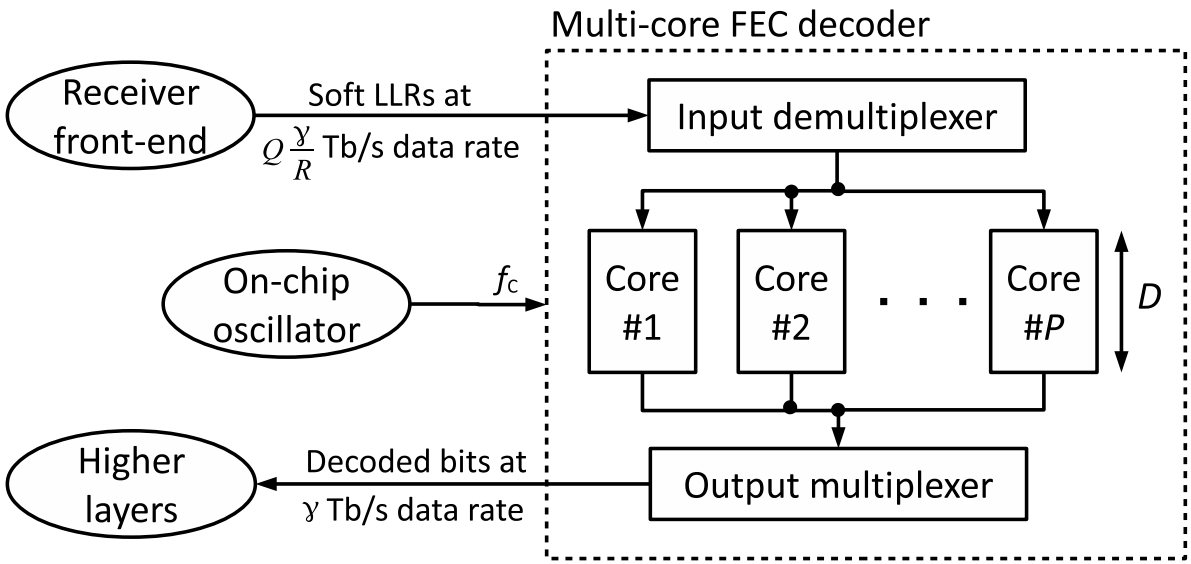

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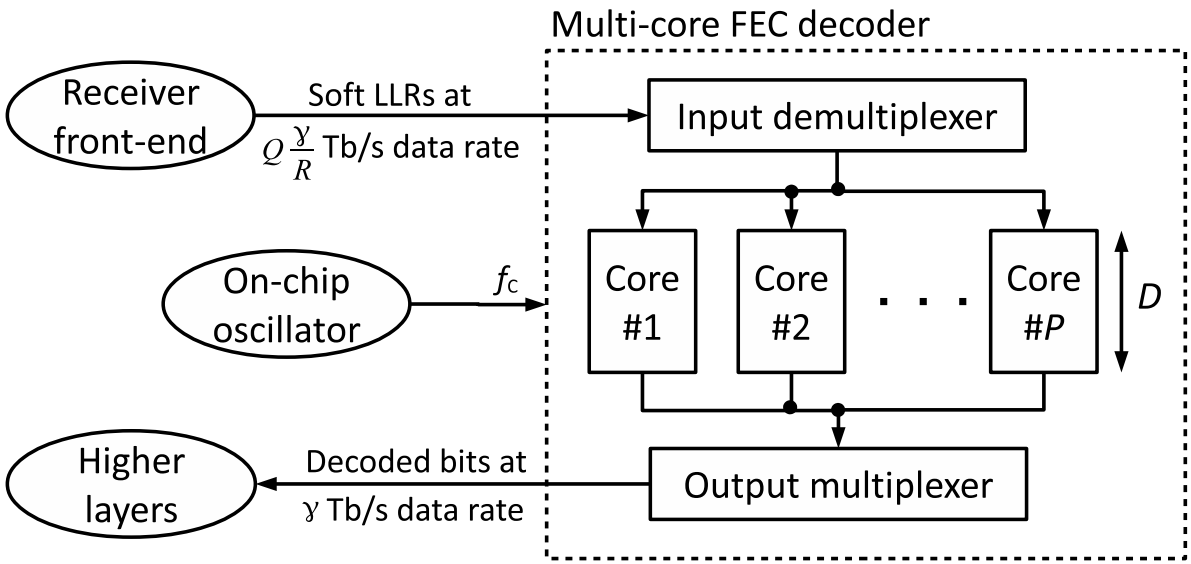

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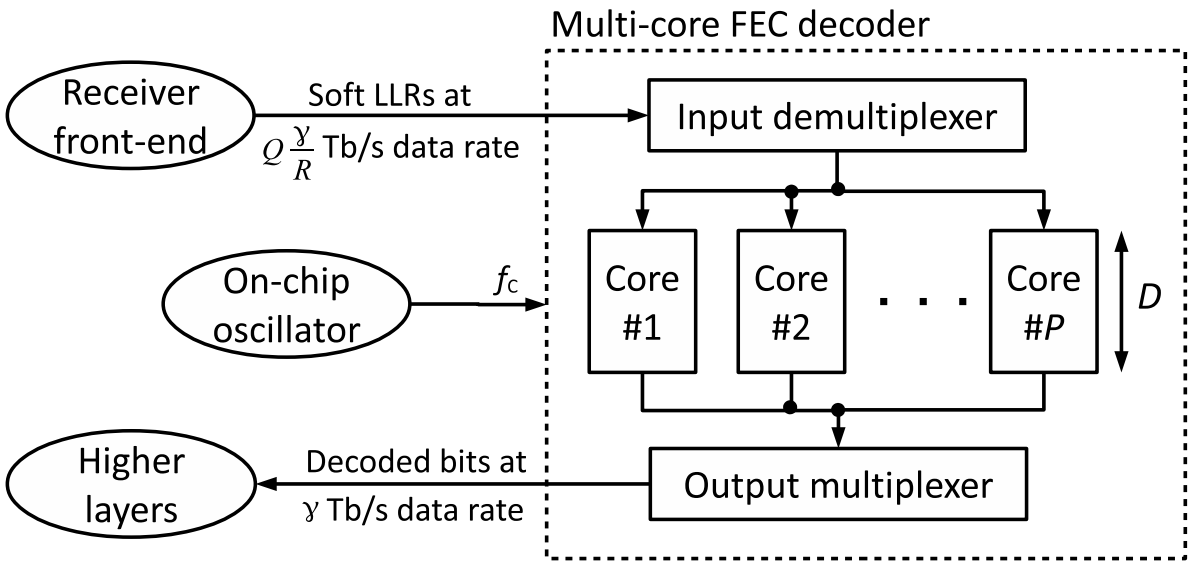

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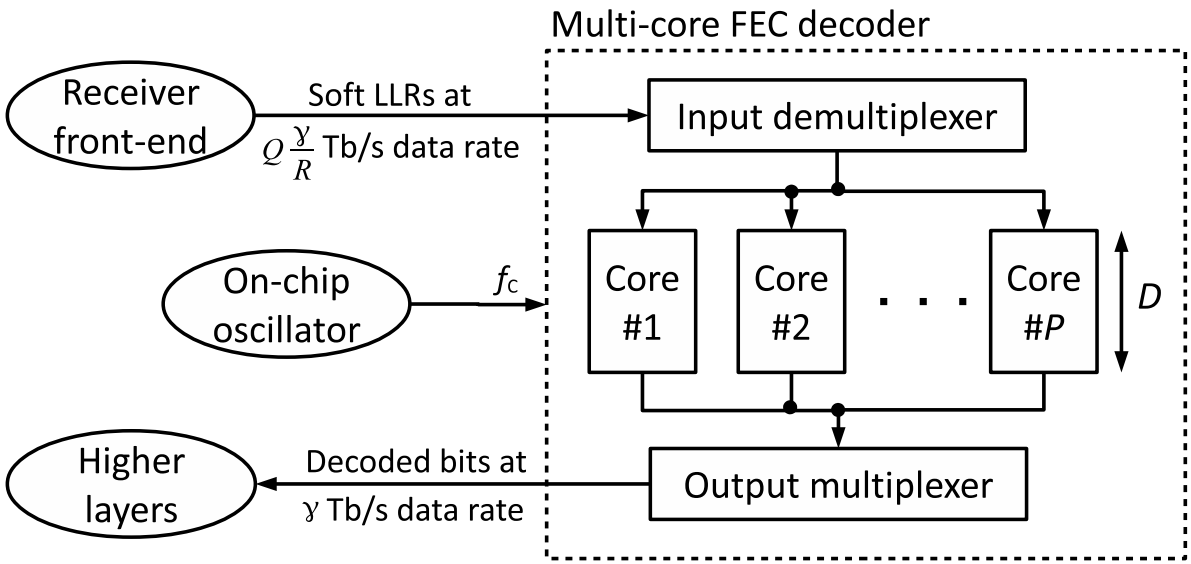

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For example, $W = \frac{\gamma{=}1 \text{ Tb/s}}{f_c{=}1 \text{ GHz}} \times \frac{Q{=}3 \text{ bits}}{R{=}1/2} = 6000$ bits

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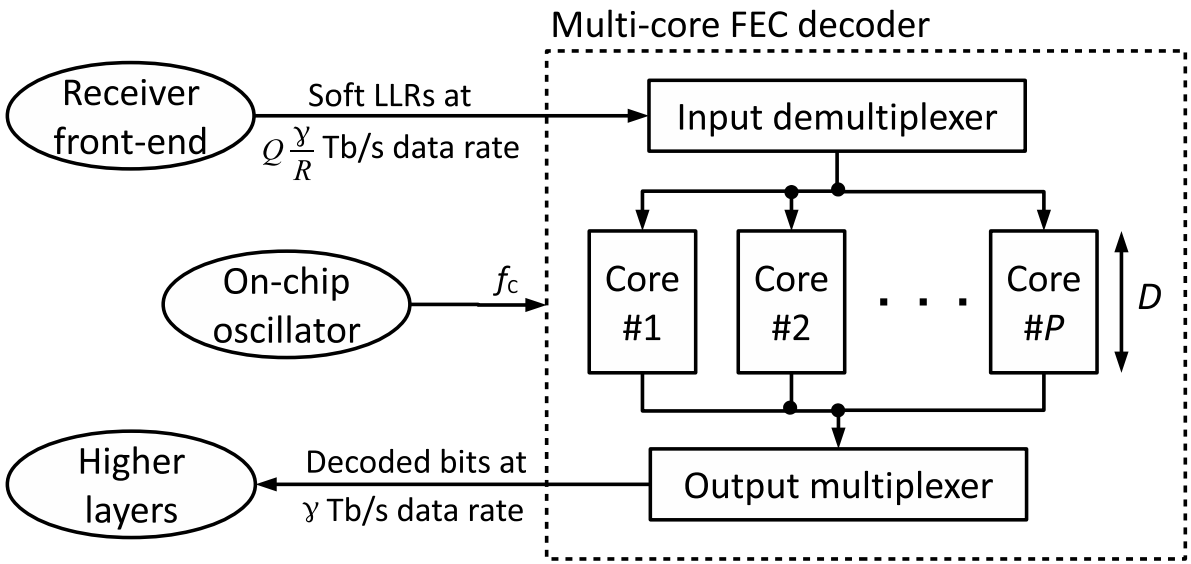

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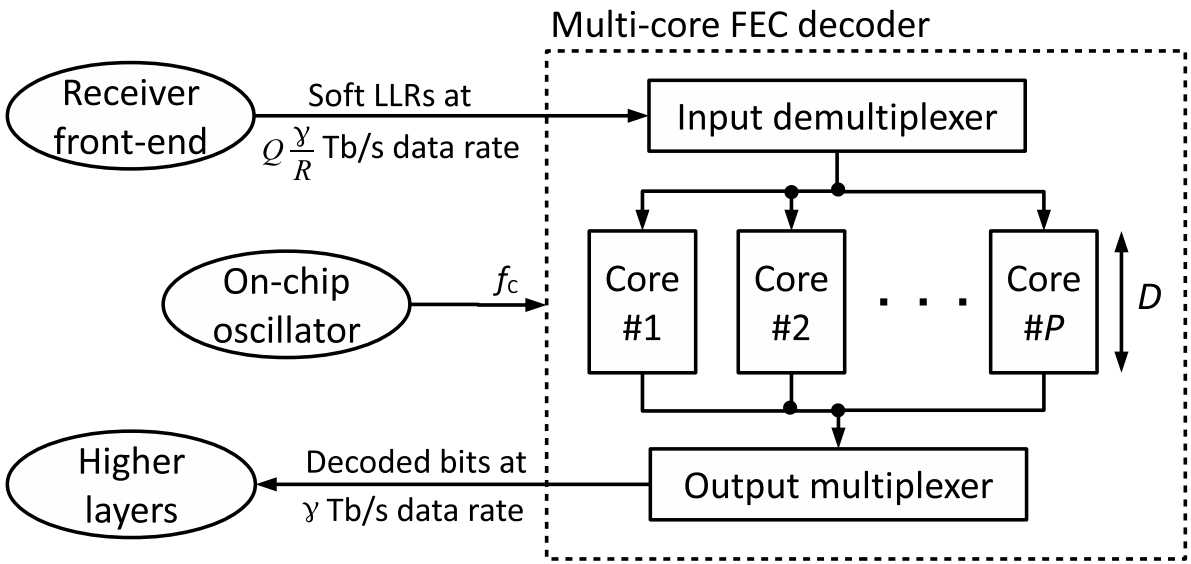

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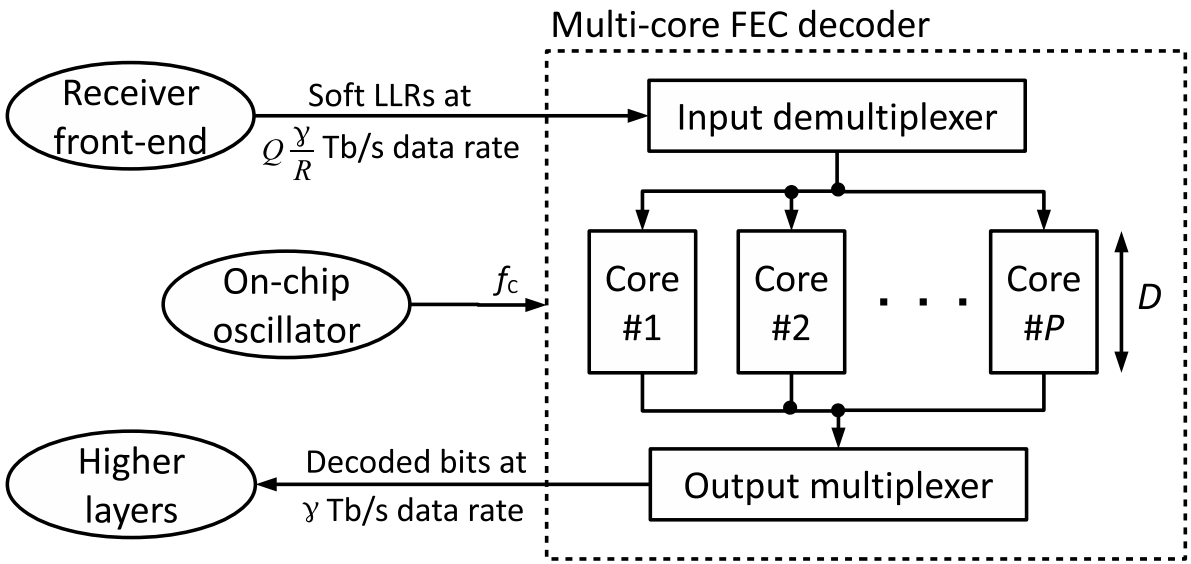

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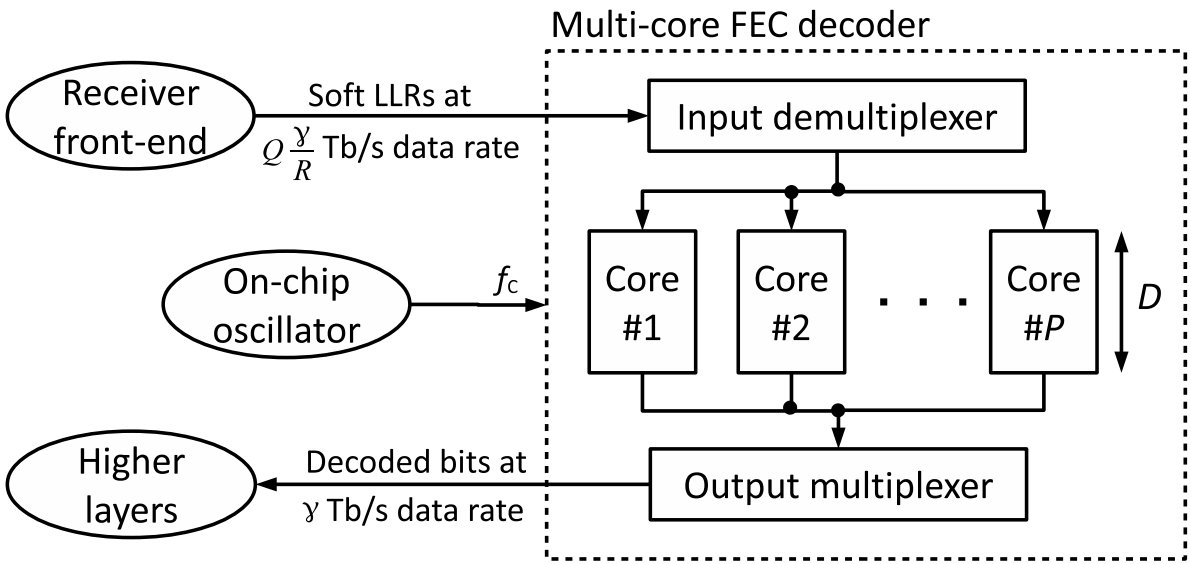

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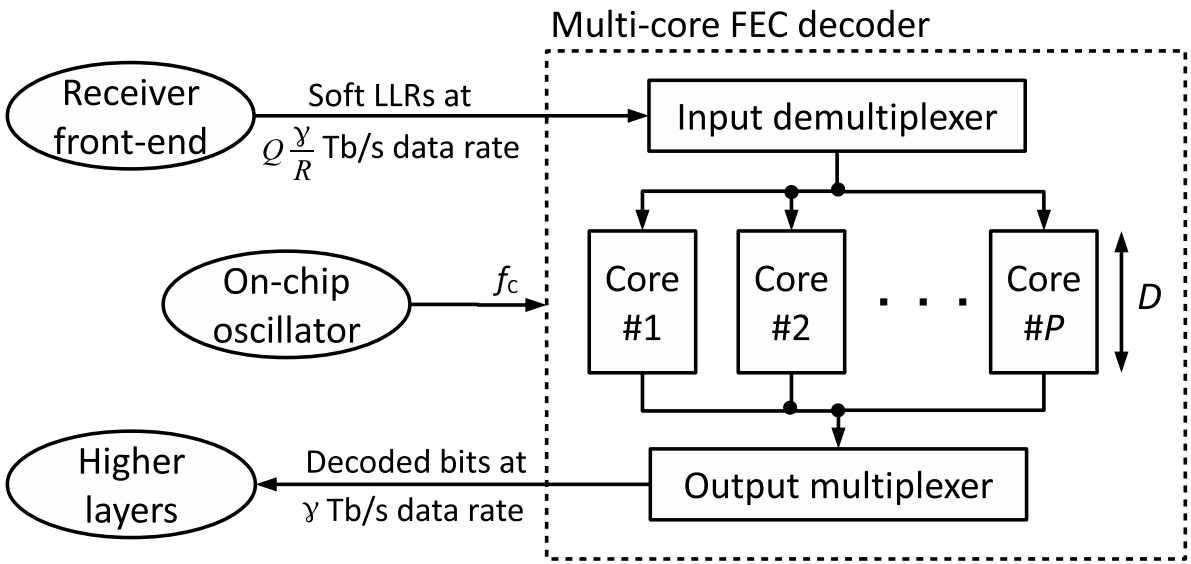

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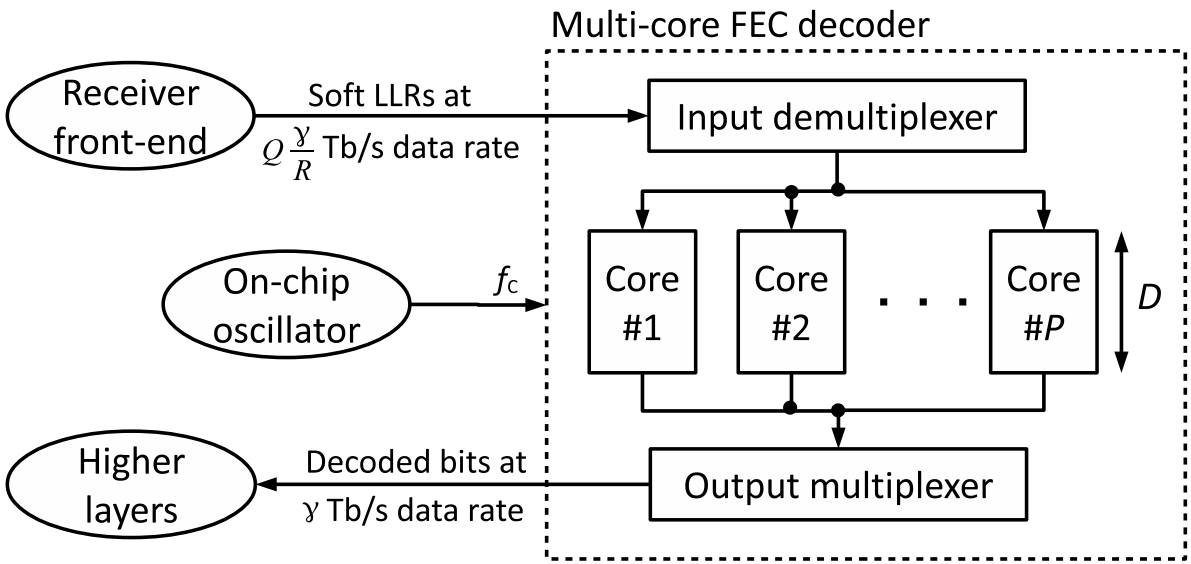

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  In fully-parallel successive cancellation (SC) polar decoder,

$$D = 2N - 2$$

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- Merge pipelined decoding stages for register balancing/retiming

Proposed SC-MJL decoding algorithm

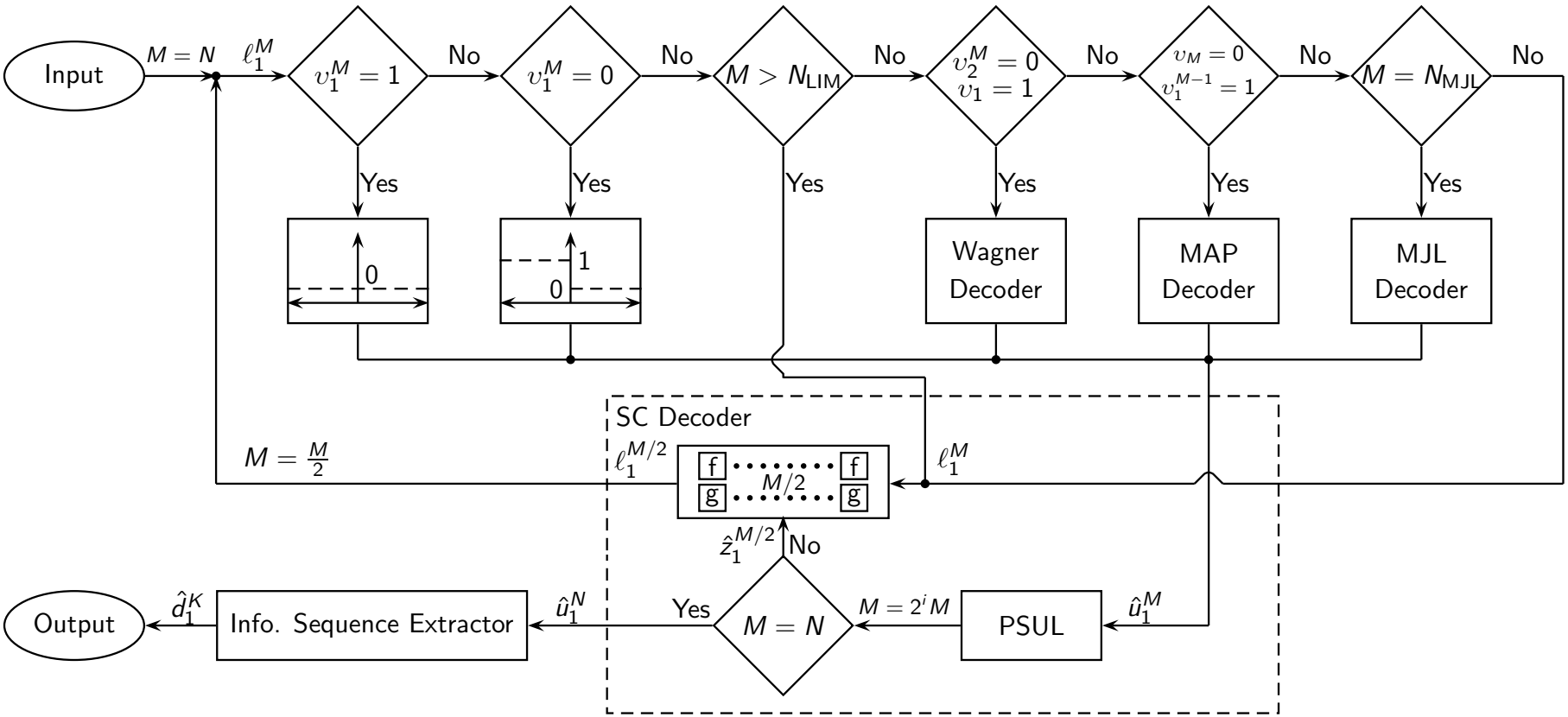
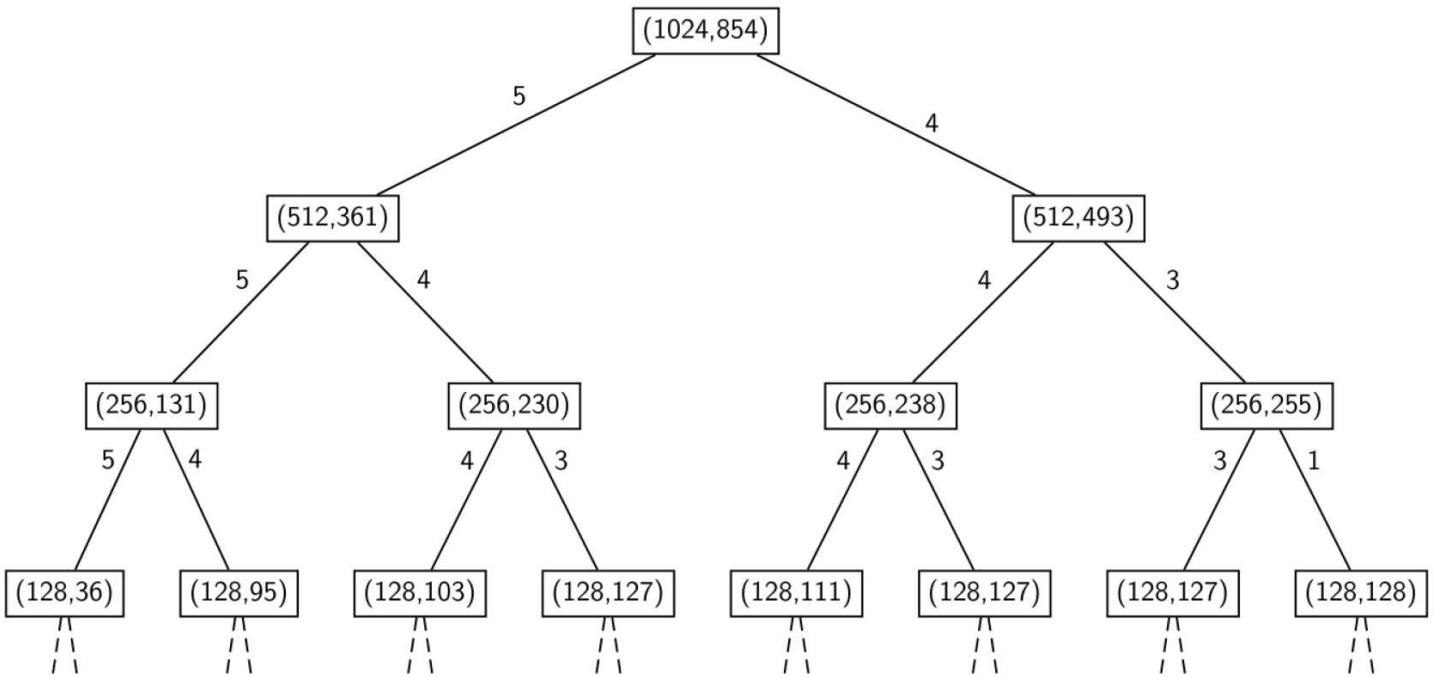


Figure: Data flowchart of SC-MJL decoding algorithm where N is the code block length, K is the number of information bits, v_1^M is the indicator vector of frozen bits with variable constituent block length M, N_{MJL} is the block length of MJL decoder and N_{LIM} is the maximum block length of Wagner and MAP decoders.

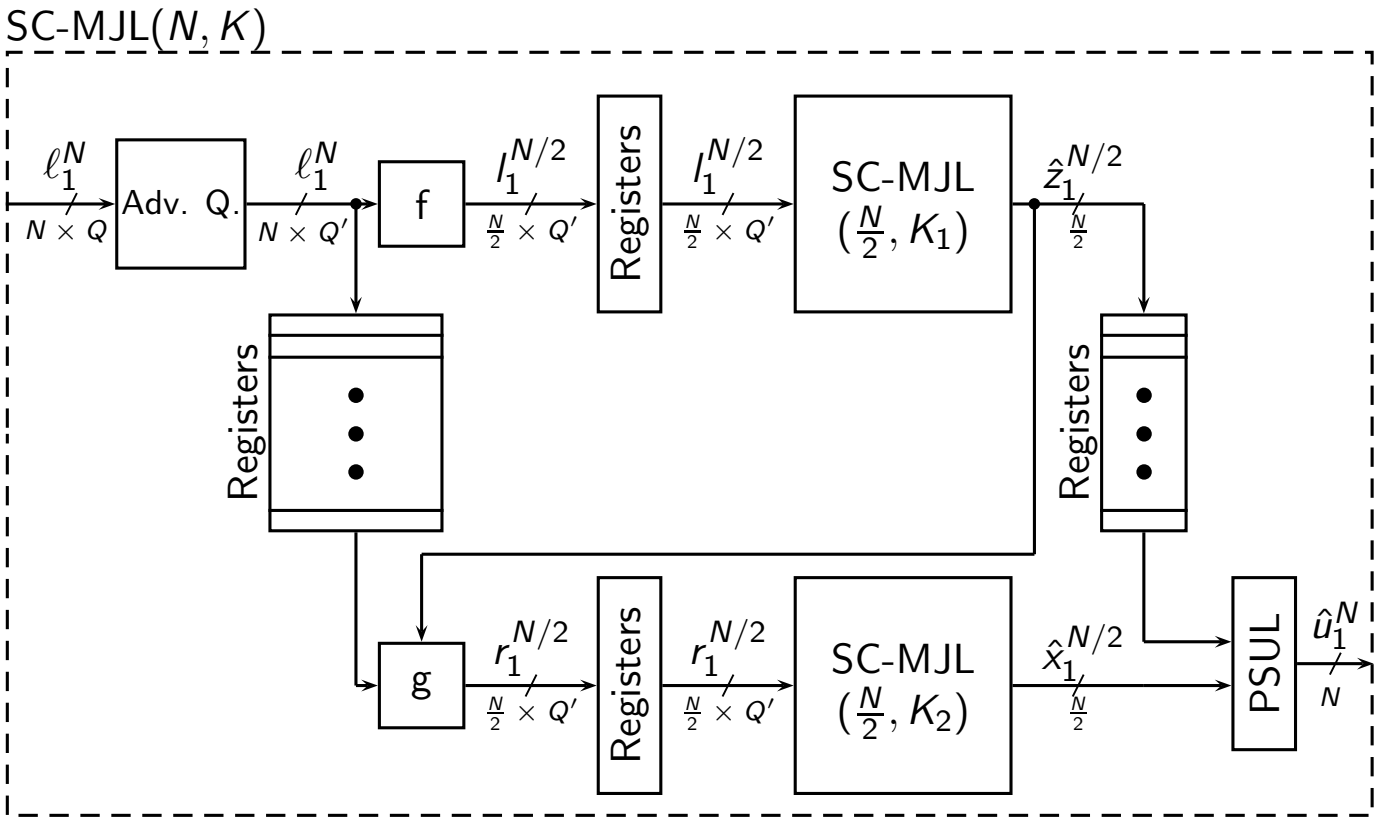
Adaptive quantization of LLRs inside the decoder



- The quantization bits are optimized using input LLR distribution of each polar code segment
- Since polarization takes place, using large number of bits is not necessary for the polarized code segments

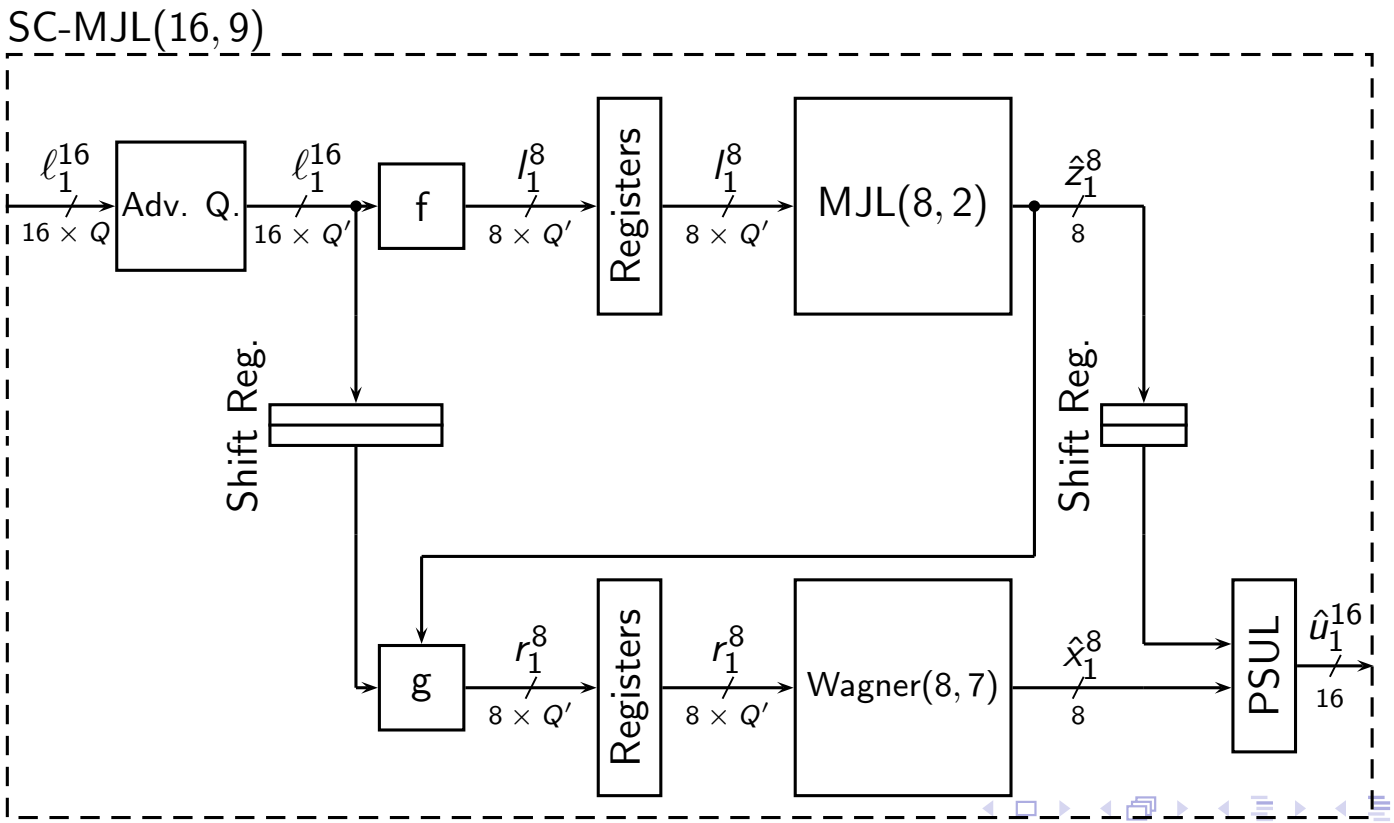
Proposed hardware architecture for SC-MJL

- For an arbitrary block length N, number of information bits K, input quantization Q and internal quantization Q', the SC-MJL architecture is



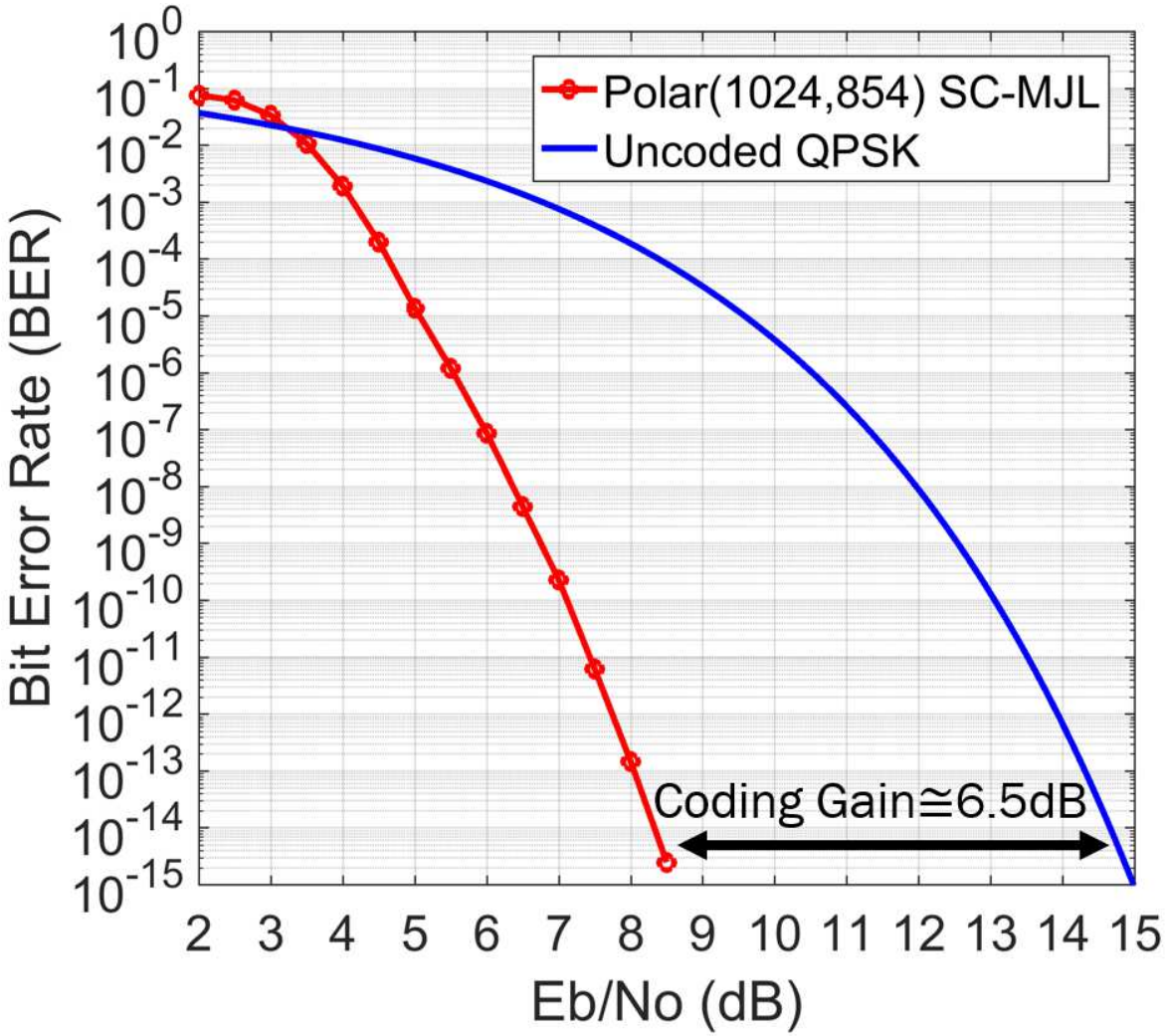
Proposed hardware architecture for SC-MJL

- An example $N = 16$, $K = 9$ design with $N_{\text{MJL}} = 8$ and $N_{\text{LIM}} = 32$ parameters
- Use MJL when $v_1^8 = \{1, 1, 1, 0, 1, 1, 1, 0\}$
- Use Wagner when $v_1^8 = \{1, 0, 0, 0, 0, 0, 0, 0\}$



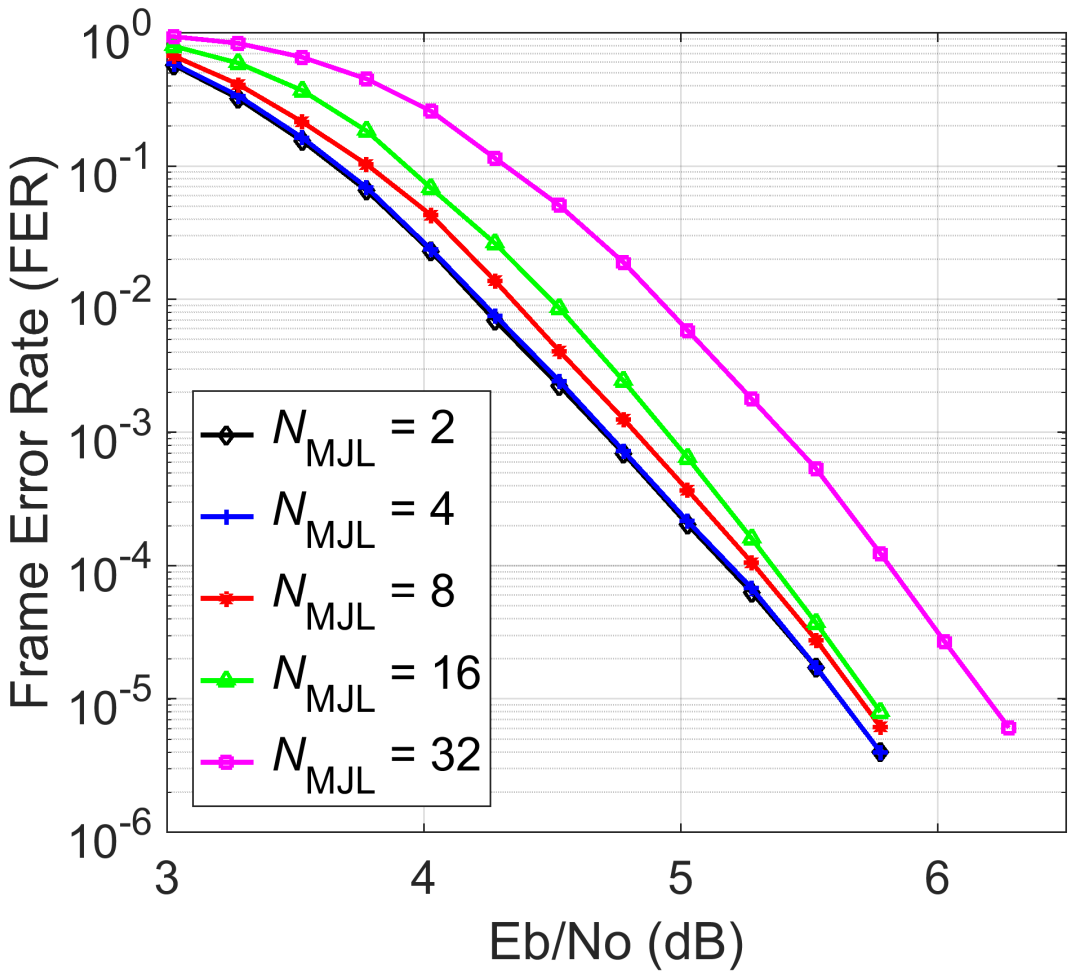
FPGA performance of SC-MJL decoder

- Carried out with an AWGN channel



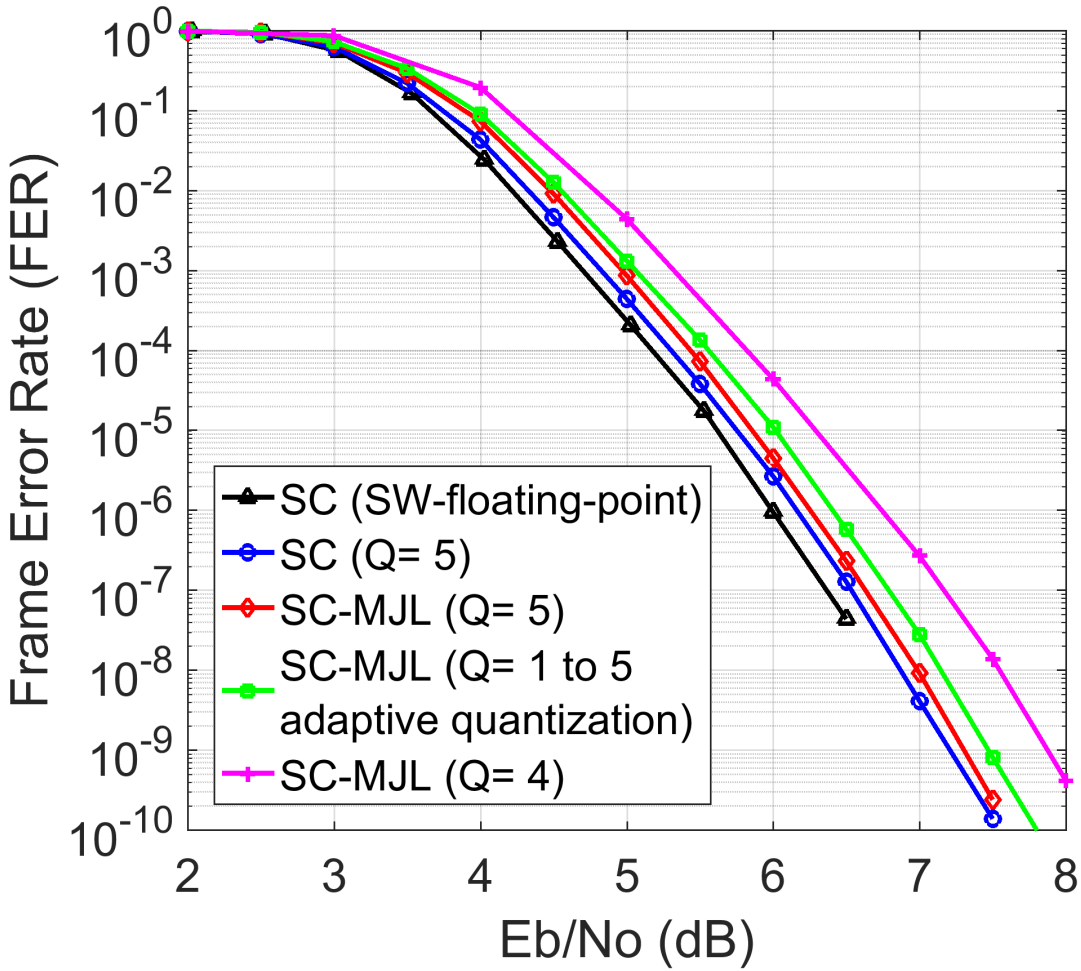
FPGA performance of SC-MJL decoder

- As N_{MJL} increases the performance deteriorates progressively



FPGA performance comparison

- Observed tolerable performance loss under adaptive quantization



ASIC 45nm post-synthesis results of (1024,854) polar code

$N_{\text{MJL}} = 8$ and $N_{\text{LIM}} = 32$

Decoding Algorithm	SC	SC-MJL	SC-MJL	SC-MJL
Quantization (bits)	6	6	5-to-1	5-to-1
Reg. Balancing Arch.	x	x	x	✓
Throughput (Gb/s)			427	
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Area (mm^2)	9.8			
Area Eff. ($Gb/s/mm^2$)	43.5			
Power (W)	4.6			
Pow. Den. (W/mm^2)	0.47			
Energy Eff. (pJ/bit)	10.9			
Latency (μs)	0.31			
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Area (mm^2)	9.8	$\xrightarrow{15\%}$ 8.3		
Area Eff. ($Gb/s/mm^2$)	43.5	51.4		
Power (W)	4.6	3.1		
Pow. Den. (W/mm^2)	0.47	0.38		
Energy Eff. (pJ/bit)	10.9	$\xrightarrow{33\%}$ 7.3		
Latency (μs)	0.31	0.25		
Latency (Clock cycles)	157	$\xrightarrow{19\%}$ 127		

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Area (mm^2)	9.8	15% → 8.3	20% → 6.6	64% → 2.4
Area Eff. ($Gb/s/mm^2$)	43.5	51.4	65.0	175.2
Power (W)	4.6	3.1	2.3	1.0
Pow. Den. (W/mm^2)	0.47	0.38	0.36	0.42
Energy Eff. (pJ/bit)	10.9	33% → 7.3	33% → 5.5	56% → 2.4
Latency (μs)	0.31	0.25	0.25	0.08
Latency (Clock cycles)	157	19% → 127	127	69% → 40

Scaled 7nm results in ASIC

- Use conservative scaling rules in [epi18] from 45nm to 7nm
- Use two identical polar decoders in parallel ($P = 2$)
- Multiply the expected 2.2 GHz clock freq. with 0.27

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Reg. Balancing Arch.	x	x	x	✓
Area Scaling	14.3	16.9	21.4	57.7
Throughput (Gb/s)			1000	
Frequency (MHz)			585.5	
Area (mm^2)			10	
Area Eff. ($Gb/s/mm^2$)			100	
Power (W)	1.69	1.14	0.85	0.37
Pow. Den. (W/mm^2)	0.17	0.11	0.09	0.04
Energy Eff. (pJ/bit)	1.69	1.14	0.85	0.37

Comparison with other implementations

Implementation	This work	[GTG17]	[Diz17]
Architecture	SC-MJL	SC-Fast	SC-Comb.
ASIC Technology	45nm	28nm	90nm
Coded Throughput (Gb/s)	512	1275	2.6
Frequency (MHz)	500	1245	2.5
Area (mm^2)	2.4	4.6	3.2
Power (W)	1.01	8.79	0.19
Converted to 28nm, 1.0 V using the scaling in [WC10], [Diz17]			
Coded Throughput (Gb/s)	823	1275	8.2
Area (mm^2)	0.94^a	4.63	0.31
Area Eff. ($Gb/s/mm^2$)	872	276	26
Power (W)	$0.44^\dagger$	8.79	0.04
Energy Eff. (pJ/bit)	$0.5^\ddagger$	6.9	4.6

[a] Normalized factor for area is $0.39 = (28/45)^2$

[†] Norm. factor for power is $0.43 = (28/45)(1.0/1.2)^2$

[‡] Norm. factor for energy eff. is $0.27 = (28/45)^2(1.0/1.2)^2$

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- List of techniques used in the proposed solution
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  - Adaptive quantization to reduce memory usage
  - Register balancing to reduce pipeline depth

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- Final remarks
  - Main challenges are frequency/throughput imbalance, I/O bottleneck and storage complexity

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Acknowledgements

- This work has been carried out by a support from the EPIC project with the funding from the European Union's Horizon 2020 research and innovation programme under grant No. 760150.

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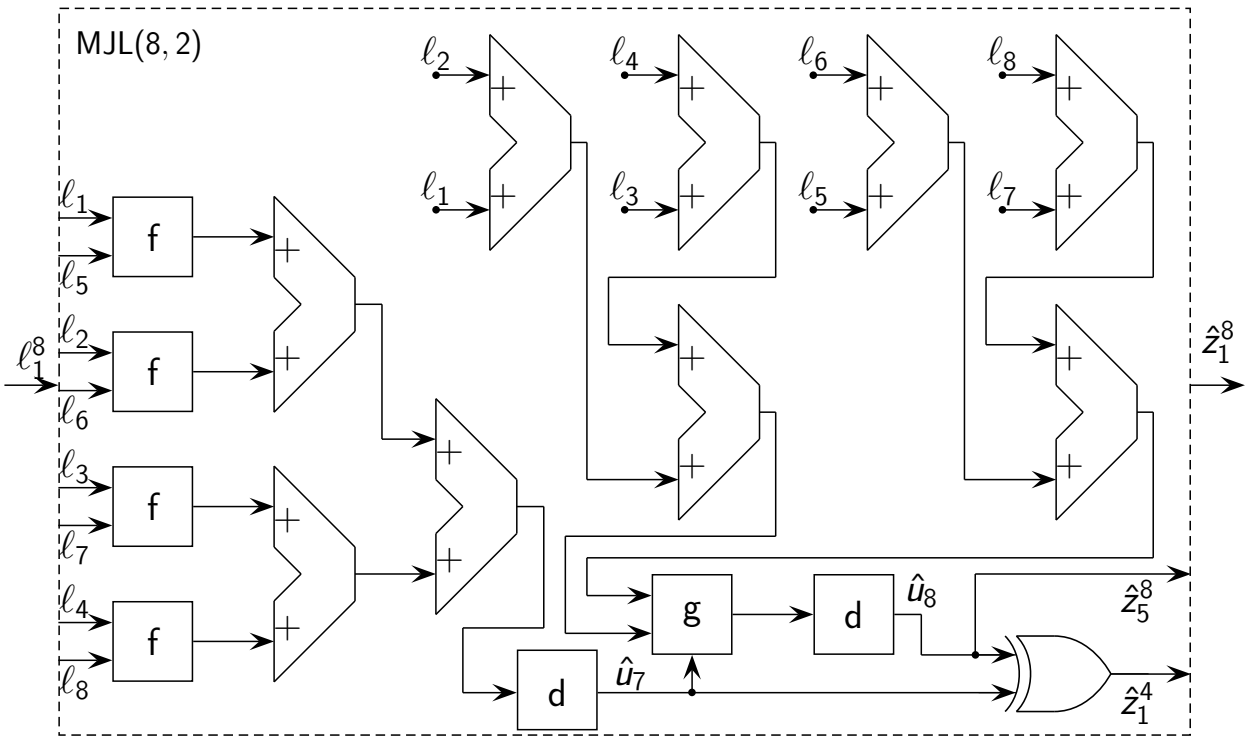
Thank you for your attention!

Extra slides: design details

- MJL(8,2) has nine adders, four f functions, two d functions, one g function and one XOR gate



Extra slides: design details

- Each f function contains a comparator and an XOR gate
- Each g function has two adders and one multiplexer