Polar Codes for Terabit/s Data Rates

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Why do we need Tb/s FEC?

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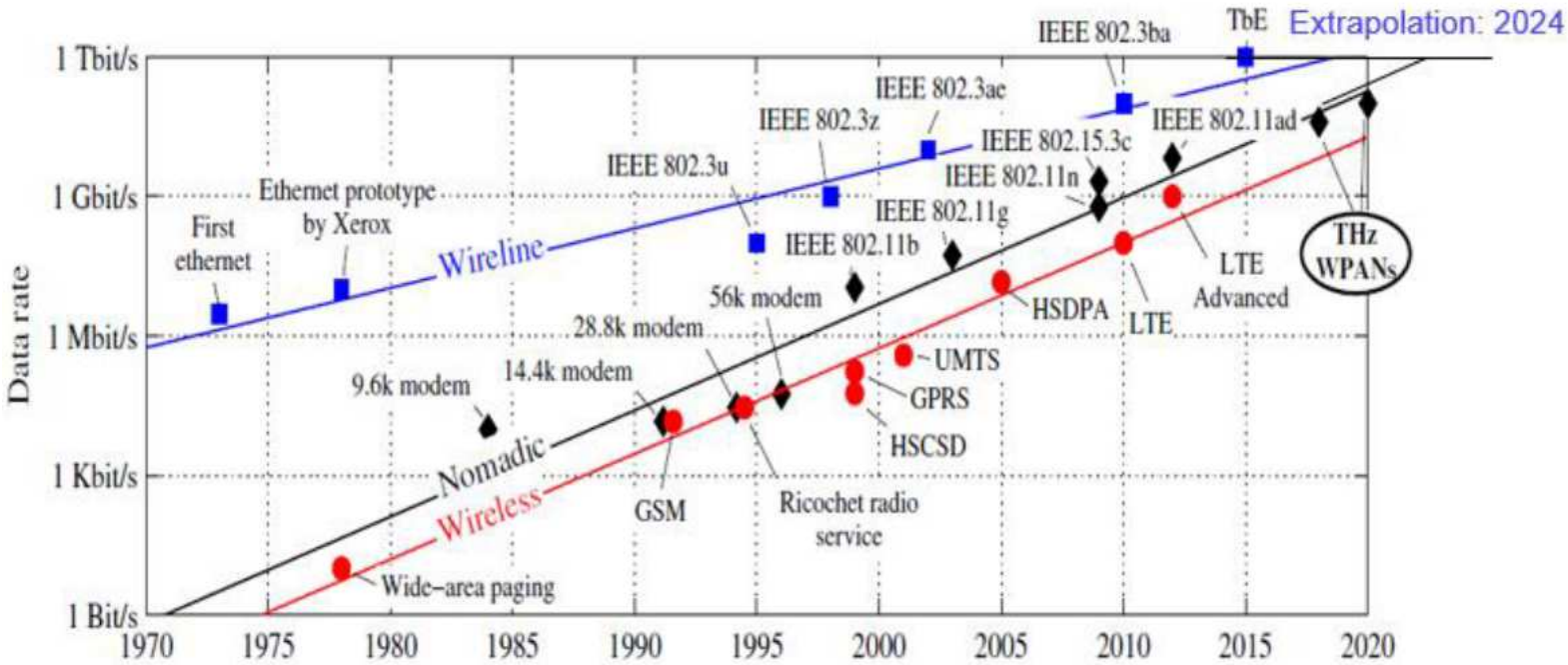
- Provide strong error-resilience for those applications using **polar codes**

When will we exploit Tb/s FEC?

- The experts in the BRAVE project claim that Tb/s links will become a reality within 4 years [Fet11], [Saa18].



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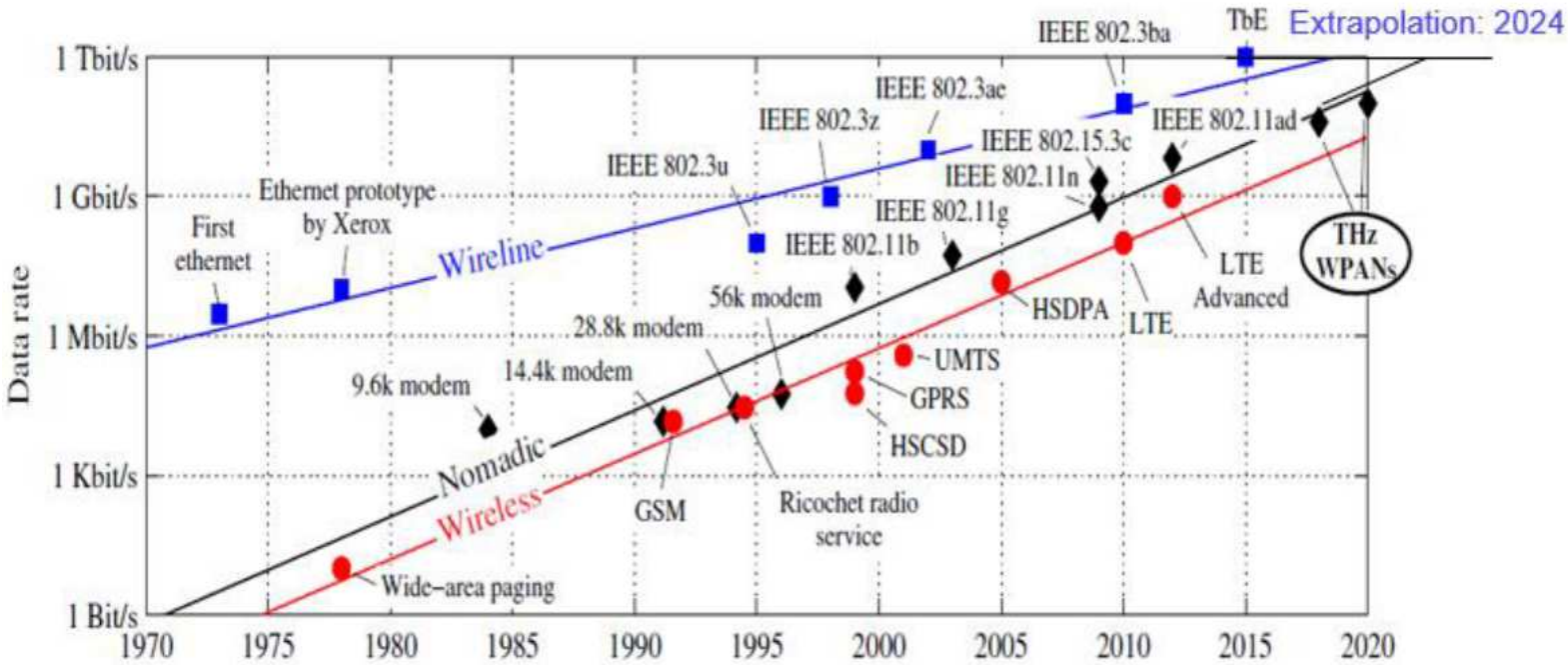
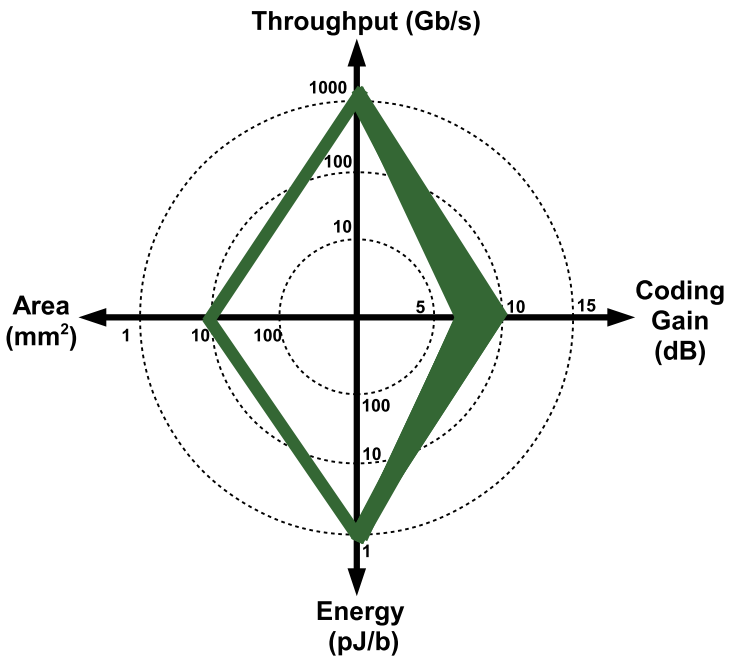


- The 2018 Ethernet Roadmap foresees a demand for Tb/s data rates for 2020 and beyond [Kip18].

What are the requirements of Tb/s FEC?

The ASIC design experts in EPIC project predicts Tb/s FEC throughput within the limits of other important KPIs [Weh17].

Name of KPI	Requirement
Technology	7nm
Throughput	1 Tb/s
Clock freq.	≤ 1 GHz
Core area	≤ 10 mm^2
Power	≤ 1 W
Power den.	≤ 0.1 W/mm^2
Area eff.	≥ 100 Gb/s/mm^2
Energy	≤ 1 pJ/bit



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- Merge pipelined decoding stages for register balancing/timing

Data flowchart of SC-MJL decoding algorithm

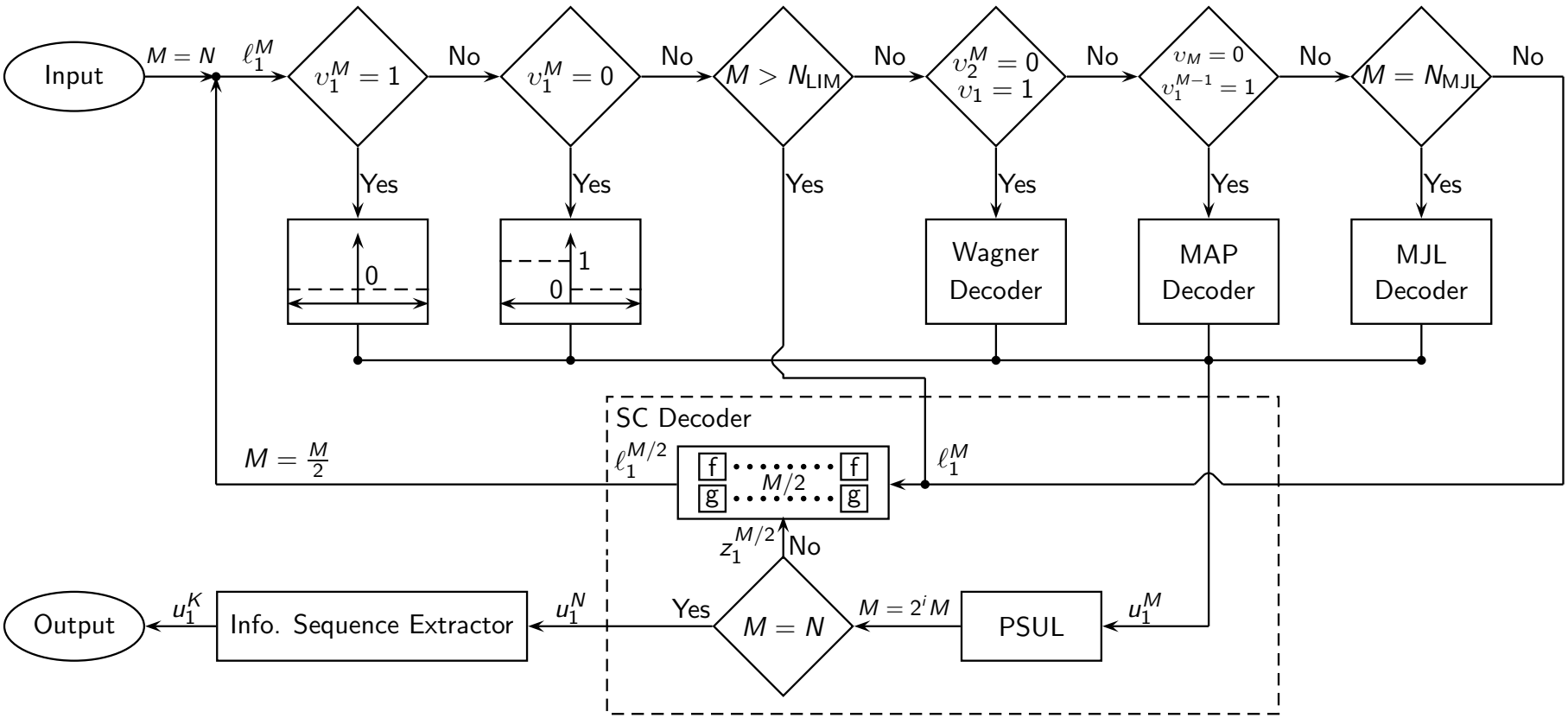
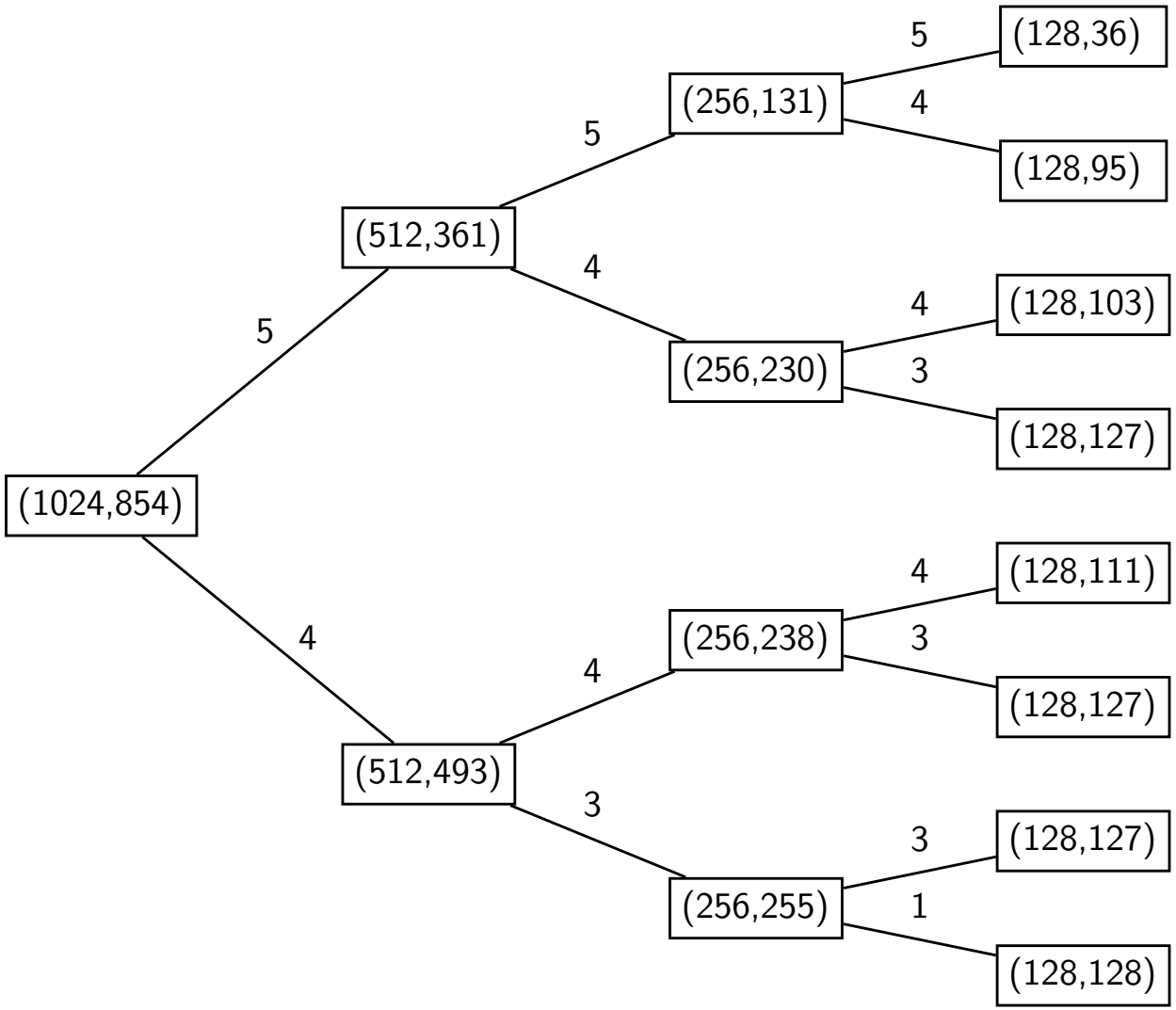


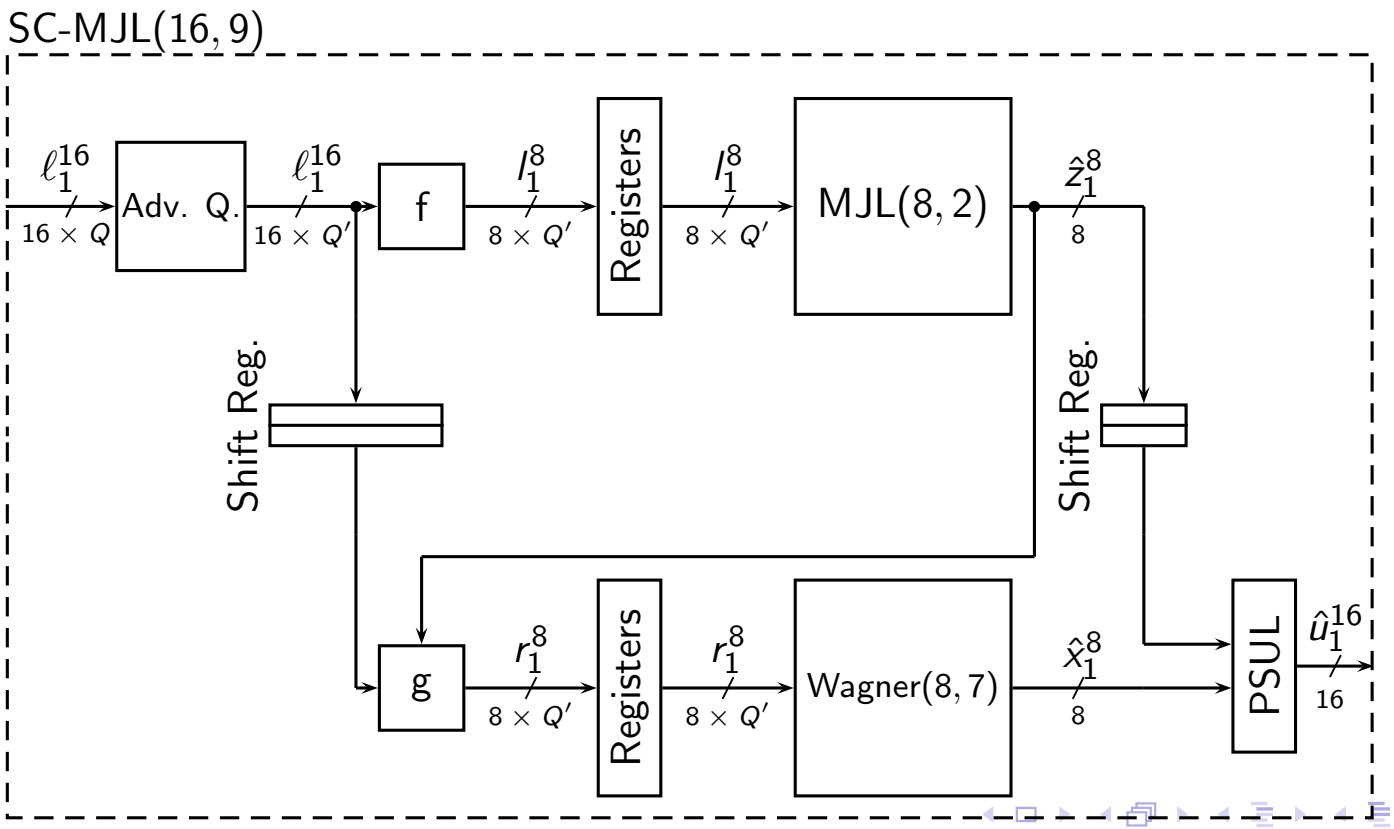
Figure: Data flowchart of SC-MJL decoding algorithm where N is the code block length, K is the number of information bits, v_1^M is the frozen vector with variable constituent block length M, N_{MJL} is the block length of MJL decoder and N_{LIM} is the maximum block length of Wagner and MAP decoders.

Progressive quantization of LLRs inside the decoder



Proposed hardware architecture for SC-MJL

- An example $N = 16$, $K = 9$ design with $N_{\text{MJL}} = 8$ and $N_{\text{LIM}} = 32$ parameters



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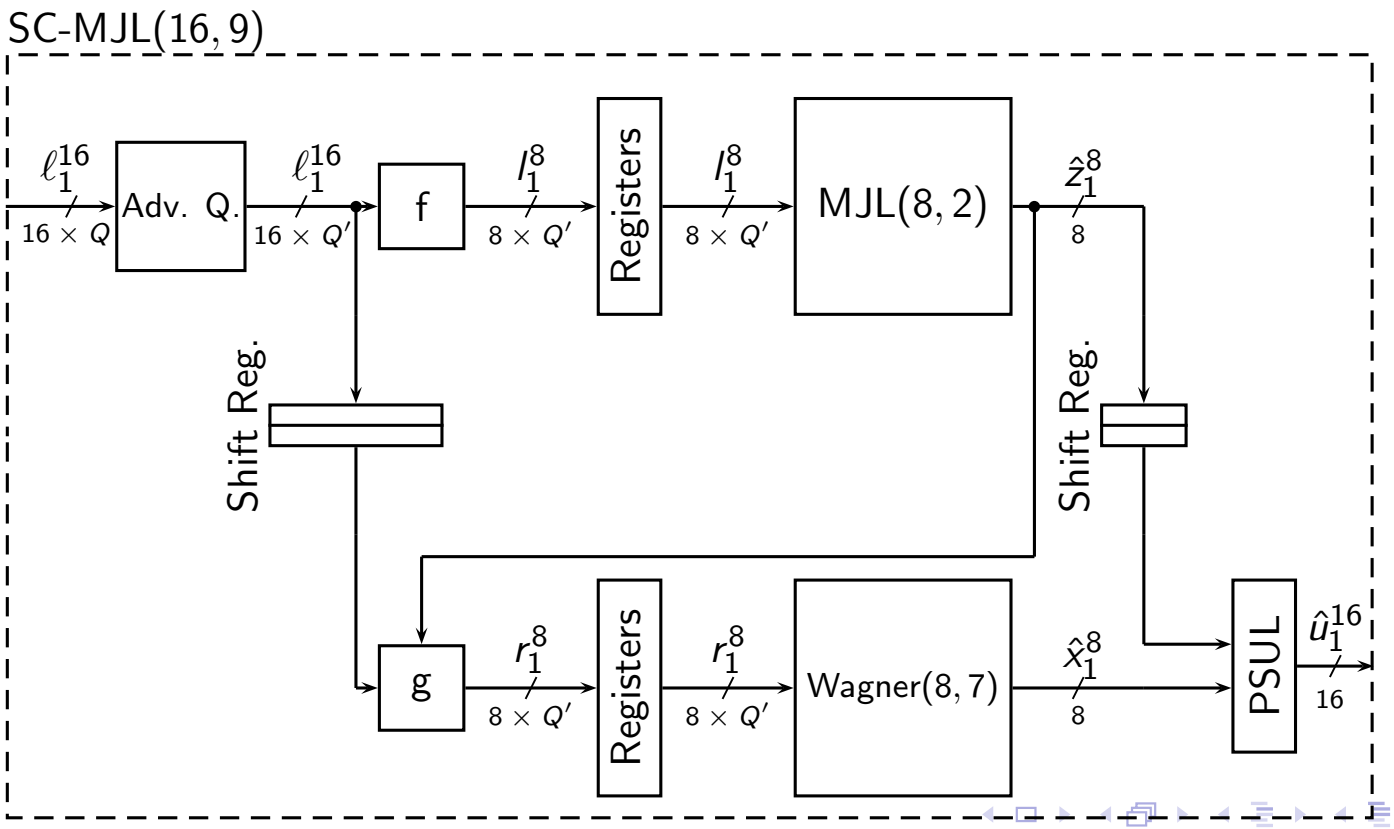
- Use MJL when $v_1^8 = \{1, 0, 0, 0, 1, 0, 0, 0\}$



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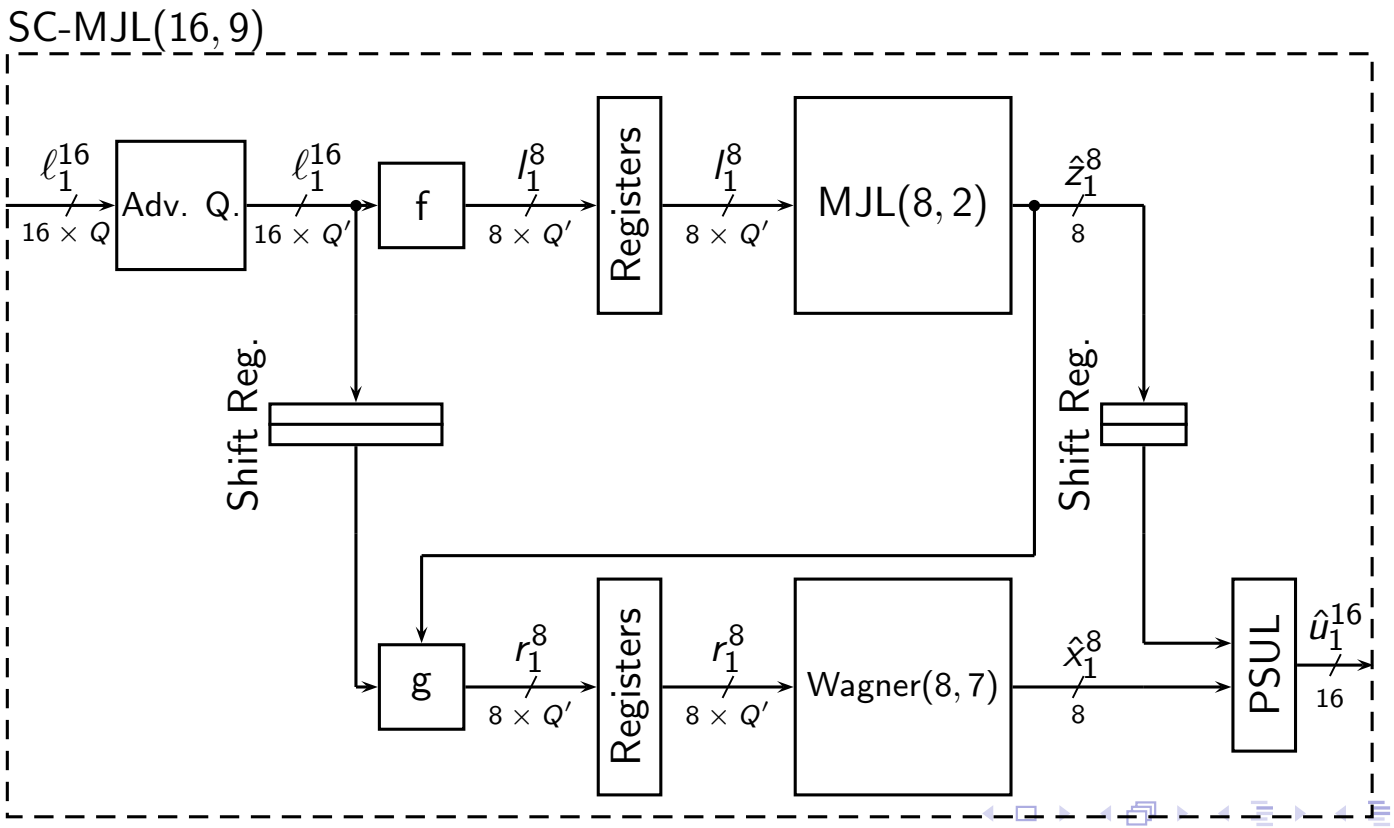
- Use Wagner when $v_1^8 = \{1, 0, 0, 0, 0, 0, 0, 0\}$



Complexity analysis

- For $n' = \log N_{\mathrm{MJL}}$, the time complexity of the fully-parallel SC-MJL decoder is

$$T_{\mathrm{N}} = 2T_{\mathrm{N}/2} + 2 = \sum_{i=1}^{n-n'} 2^i + 2^{n-n'} = 3\frac{N}{N_{\mathrm{MJL}}} - 2 = \Theta(N).$$

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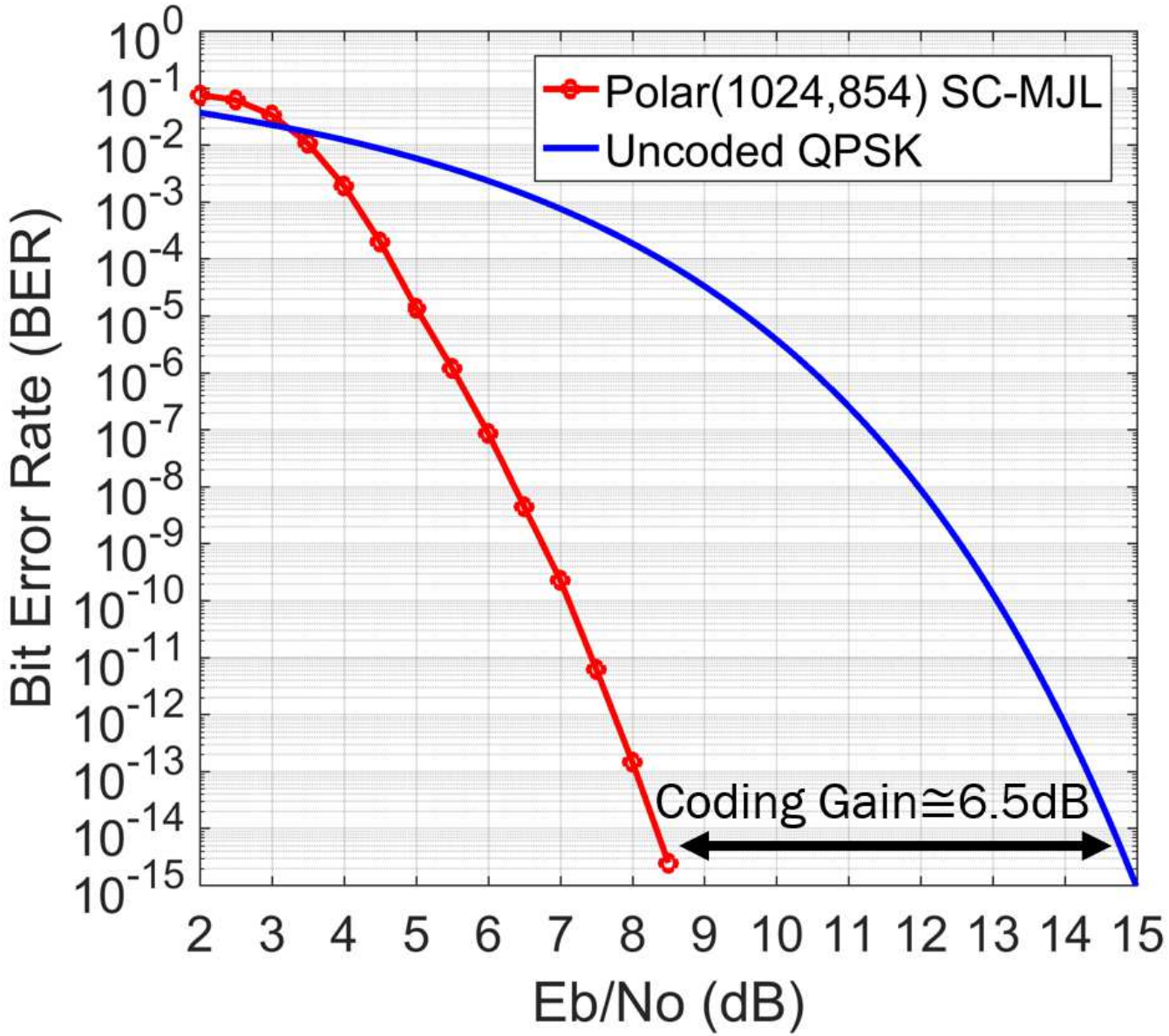
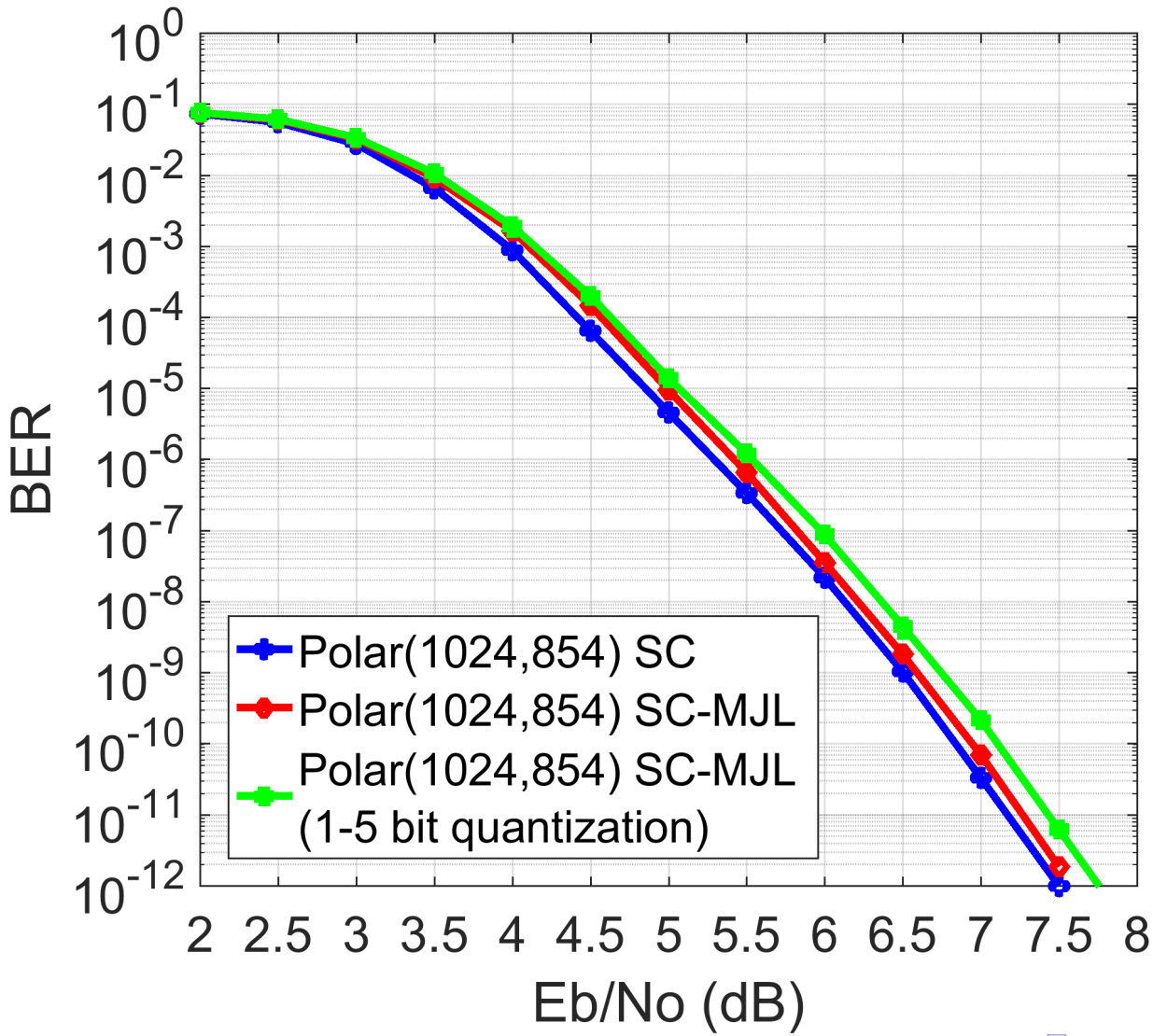
- For $N_{\text{MJL}} \leq N$ and $M_4 = 32Q' + 16$, the memory complexity of the unrolled and fully-pipelined SC-MJL decoder is

$$\begin{aligned} M_{\text{N}} &= 2M_{\text{N}/2} + (Q' + 0.5)\left(1.5\frac{N^2}{N_{\text{MJL}}} - N\right) \\ &= (Q' + 0.5)\left(\frac{1.5}{N_{\text{MJL}}}(2 - 2^{-\log N + \log N_{\text{MJL}}})N^2 - N\log N + 1.5N\right) \\ &= \Theta(N^2 Q'). \end{aligned}$$

FPGA performance of SC-MJL decoder



FPGA performance comparison



ASIC 45nm post-synthesis results of (1024,854) polar code

- Take $N_{\mathrm{MJL}} = 8$ and $N_{\mathrm{LIM}} = 32$

Decoding Algorithm	SC	SC-MJL	SC-MJL	SC-MJL
Quantization (bits)	6	6	5-to-1	5-to-1
Reg. Balancing Arch.	x	x	x	✓
Throughput (Gb/s)			427	
Frequency (MHz)			500	
Latency (μs)	0.31	0.25	0.25	0.08
Latency (Clock cycles)	157	127	127	40
Area (mm^2)	9.8	8.3	6.6	2.4
Area Eff. ($\mathrm{Gb/s/mm}^2$)	43.5	51.4	65.0	175.2
Power (W)	4.6	3.1	2.3	1.0
Pow. Den. ($\mathrm{W/mm}^2$)	0.47	0.38	0.36	0.42
Energy (pJ/bit)	10.9	7.3	5.5	2.4

Scaled 7nm results in ASIC

- Use ITRS CMOS scaling rules in [Gra15] from 45nm to 7nm

Decoding Algorithm	SC	SC-MJL	SC-MJL	SC-MJL
Quantization (bits)	6	6	5-to-1	5-to-1
Reg. Balancing Arch.	x	x	x	✓
Throughput (Gb/s)			1000	
Frequency (MHz)			585.5	
Area (mm^2)			10	
Area Eff. ($Gb/s/mm^2$)			100	
Power (W)	1.69	1.14	0.85	0.37
Pow. Den. (W/mm^2)	0.17	0.11	0.09	0.04
Energy Eff. (pJ/bit)	1.69	1.14	0.85	0.37
Latency (μs)	0.27	0.22	0.22	0.07
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  - Find solutions for flexibility in terms of N and K

Acknowledgements

- We thank Prof. Orhan Arıkan for the valuable discussions and ideas about the progressive quantization method.
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References

Erdal Arikan.
Channel polarization: A method for constructing capacity-achieving codes for symmetric binary-input memoryless channels.
IEEE Transactions on Information Theory, 55(7):3051–3073, July 2009.

Onur Dizdar.
High Throughput Decoding Methods and Architectures for Polar Codes with High Energy-Efficiency and Low Latency.
PhD thesis, Bilkent University, 2017.

Gehard Fettweis.
Entering the path towards terabit/s wireless links.
pages 1 – 6, 04 2011.

Mart Graef.
2015 International Technology Roadmap for Semiconductors (ITRS) Section 5: More Moore.
Technical report, 2015.

Scott Kipp.
EthernetRoadmap-2018-side1-1600x1200.jpg (JPEG image, 1600x120 pixels) - scaled (76%), 2018.

Majed Saad.
Beyond-5G Wireless Tbps Scenarios and Requirements, 2018.

Norbert Wehn.
EPIC - Enabling practical wireless Tb/s communications with next generation channel coding.
https://epic-h2020.eu/results, 2017.

Thank you!