Polar Codes for Terabit/s Data Rates

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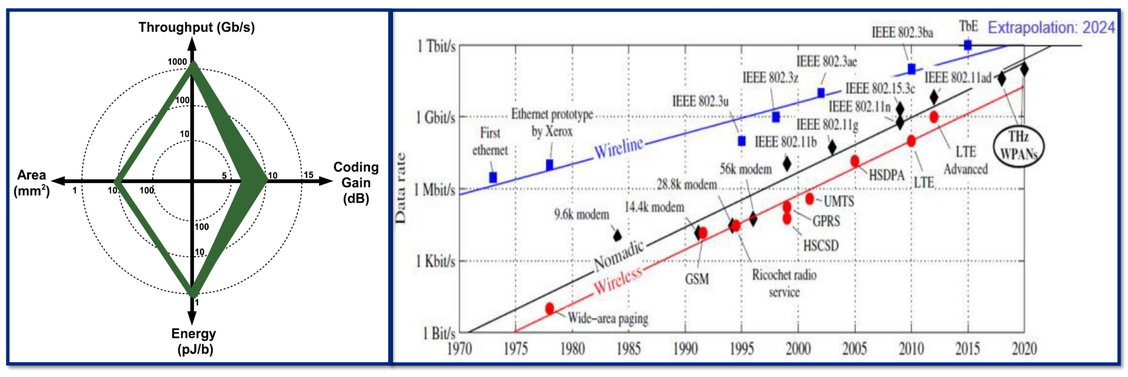
Terabits-per-Second FEC

- **Why do we need Tb/s FEC?**

A new generation of Forward-Error Correction (FEC) codes operating at Terabit-per-second (Tb/s) data rates are necessary to provide a low complexity and strong error-resilience for the beyond-5G (B5G) applications. For example, some B5G applications are wireless fronthauling and backhauling, server farming in data centers, drone-based communications, virtual reality, wireless chip-to-chip communications and data kiosks.

- **When will we exploit Tb/s FEC?**

The recent standardization activities show that there is an increasing demand for higher data rates. For wired connections, the IEEE 802.3ba Ethernet standard specifies 100 Gb/s throughput over optical media [1]. In the wireless domain, the IEEE 802.15.3d standard defines a 100 Gb/s system using frequencies in the range of 252 – 322 GHz [2]. The 2018 Ethernet Roadmap foresees a demand for Tb/s data rates for 2020 and beyond [3]. Furthermore, the experts in the BRAVE Project (for automated vehicles) claim that Tb/s links will become reality within 4 years [4].

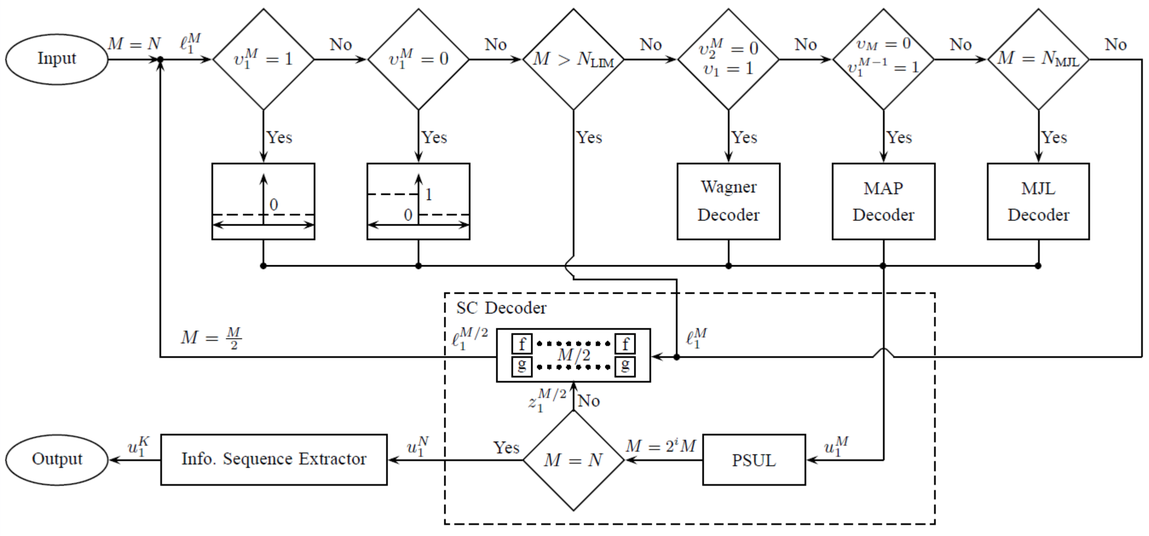


- **What are the requirements of Tb/s FEC?**

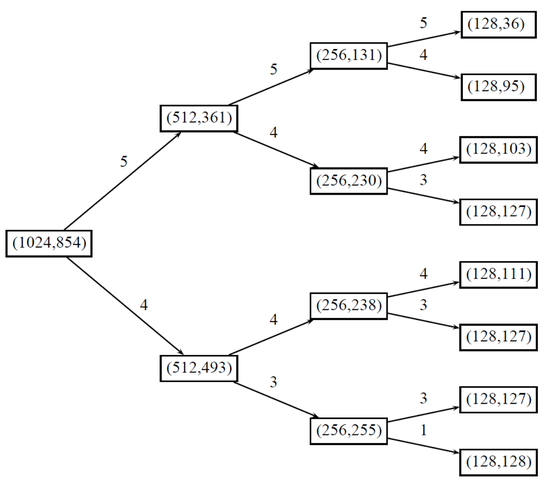
The ASIC design experts in EPIC Project predicts **1 Tb/s** FEC throughput within the limits of other Key-Performance-Indicators (KPIs) as **1 GHz** clock frequency, **10 mm²** core area and **1 W** power dissipation, which brings **1 pJ/b** energy efficiency under **0.1 W/mm²** power density [5].

Decoding Algorithm for Polar Codes

As an energy-efficient Tb/s FEC solution, systematic polar codes [6,7] are proposed. By using Majority-Logic (MJL) aided Successive Cancellation (SC) namely SC-MJL decoding algorithm (firstly proposed in [8]), an hybrid decoding scheme is developed for polar codes. SC-MJL algorithm exploits the low complexity nature of SC decoding and the low latency property of MJL. Similar to [9], the repetition and single parity check code segments of the polar code are decoded by MAP and Wagner decoders respectively. The recursive structure of SC-MJL decoding algorithm is shown below. N is the code block length, K is the number of information bits, v_1^M is the indicator vector of the frozen bits with a variable constituent block length M, N_{LIM} is the maximum block length of Wagner and MAP sub-decoders, and N_{MJL} is the block length of MJL sub-decoders.

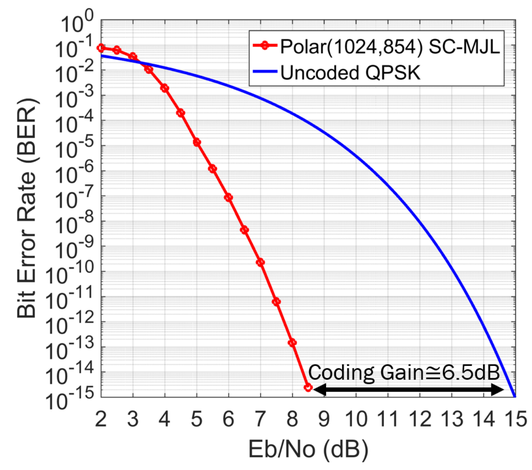


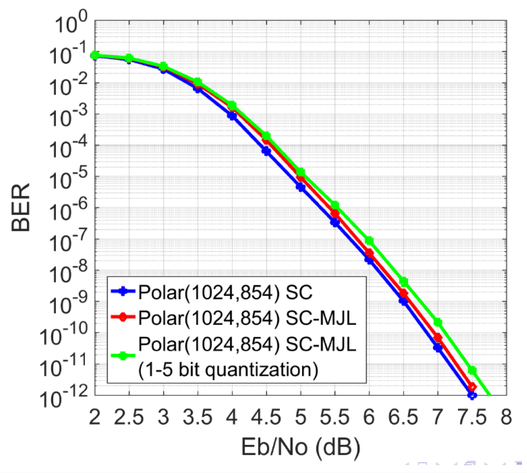
In order to reduce the computation complexity and memory area of the SC-MJL algorithm, an adaptive quantization scheme is developed within 1-5 bits range of internal log-likelihood ratios (LLRs). The bit allocation is based on maximizing the mutual information between the input and output LLRs for each constituent polar code. For (N=1024,K=854) polar code, the adaptive quantization levels are given on the connectors between the constituent polar codes.



Simulation Results

The simulations have been performed on FPGA to obtain the communication performance results of the SC-MJL decoding algorithm and the adaptive quantization method. The simulations have been carried out over an AWGN channel with BPSK modulation of the (1024,854) polar code. The SC-MJL decoder has 5 bit LLR quantization, N_{LIM} = 32 and N_{MJL} = 8 and v_1^M is generated by the density evolution algorithm at 6.5 dB Es/No.

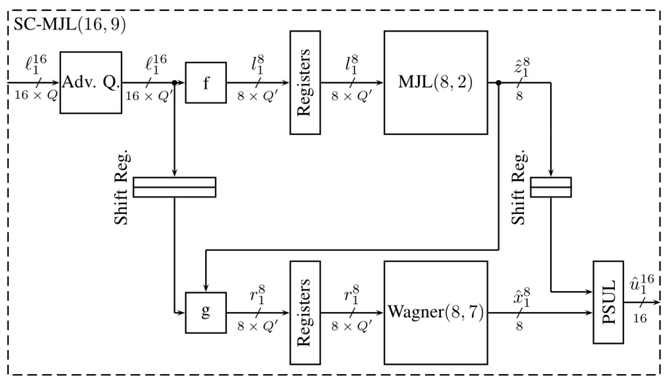


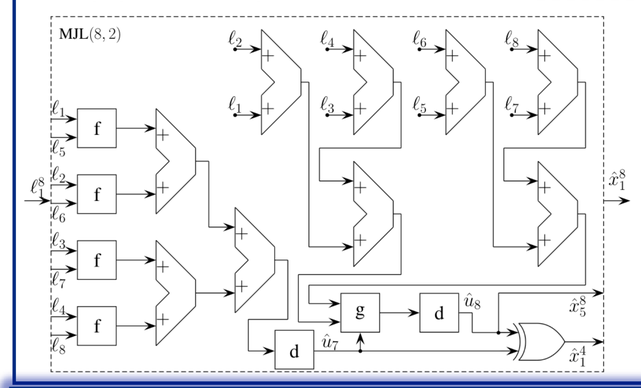


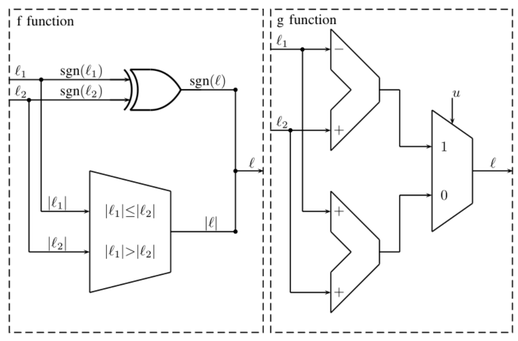
Architecture

We propose an unrolled and deeply pipelined SC-MJL decoder architecture with fully-parallel processing units. The unrolled architecture utilizes a dedicated logic block for each set of operation as shown below.

For example, the SC-MJL(16,9) decoder consists of the combinational MJL(8,2) and Wagner(8,7) sub-decoders. The consecutive pipelined decoding stages are merged by removing registers for register balancing and timing in order to reduce the pipeline depth.







Implementation Results

The ASIC post-synthesis results of (1024,854) polar codes are shown. The PVT parameters are 45nm, 1.2 V and 25°C. The ITRS scaling [10] of the last implementation from 45nm to 7nm shows that **1 Tb/s** throughput is achieved with **585.5 MHz** frequency, **10 mm²** core area and **0.37 W** power dissipation, which brings **0.37 pJ/b** energy efficiency under **0.04 W/mm²** power density.

Decoding Algorithm	SC	SC-MJL	SC-MJL	SC-MJL
Quantization (bits)	6	6	5	5-to-1
Reg. Balancing Arch.	x	x	x	✓
Flexible Code Rate	x	x	✓	x
Throughput (Gb/s)			427	
Frequency (MHz)			500	
Area (mm²)	9.8	8.3	13.7	2.4
Power (W)	4.6	3.1	9.9	1.0
Area Eff. (Gb/s/mm²)	43.5	51.4	31.3	175.2
Pow. Den. (W/mm²)	0.47	0.38	0.73	0.42
Energy Eff. (pJ/bit)	10.9	7.3	23.3	2.4
Latency (μs)	0.31	0.25	0.76	0.08
Latency (Clock cycles)	157	127	382	40

Conclusions

In order to reach high throughput within the physical limits of ASIC technology, we proposed SC-MJL decoding algorithm by using adaptive quantization and register-balancing architecture. The post-synthesis results show that 1 Tb/s polar code based FEC is feasible with a 6.5 dB coding gain.

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