A FPGA Implementation Study of Successive Cancellation List=2 Polar Decoder

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IEEE Bilkent Graduate Research Conference 2019

Introduction

It is foreseen that for some of the beyond-5G applications, there will be demand for data rates up to 1 Tb/s [1]. Polar codes, introduced in [2], is one of the leading code classes for beyond-5G applications for reaching mentioned high throughputs with limited area and power consumption. Therefore polar code implementations, especially successive cancellation (SC), to reach high data rates is frequently studied subject. This study uses the successive cancellation list decoding [3] (SCL) polar decoder for list length equal to 2. The decoder is implemented on Xilinx Virtex-7 Ultrascale+ FPGA available on the Amazon Web Services. Results of our study yields promising results towards reaching high throughput values within the EPIC project limits when the results are scaled to 7nm ASIC.

EPIC Limits

Technology	@7nm
Net TP	≥1 Tb/s
Area	≤10 mm2
Power	≤1 W
Frequency	≤1 GHz

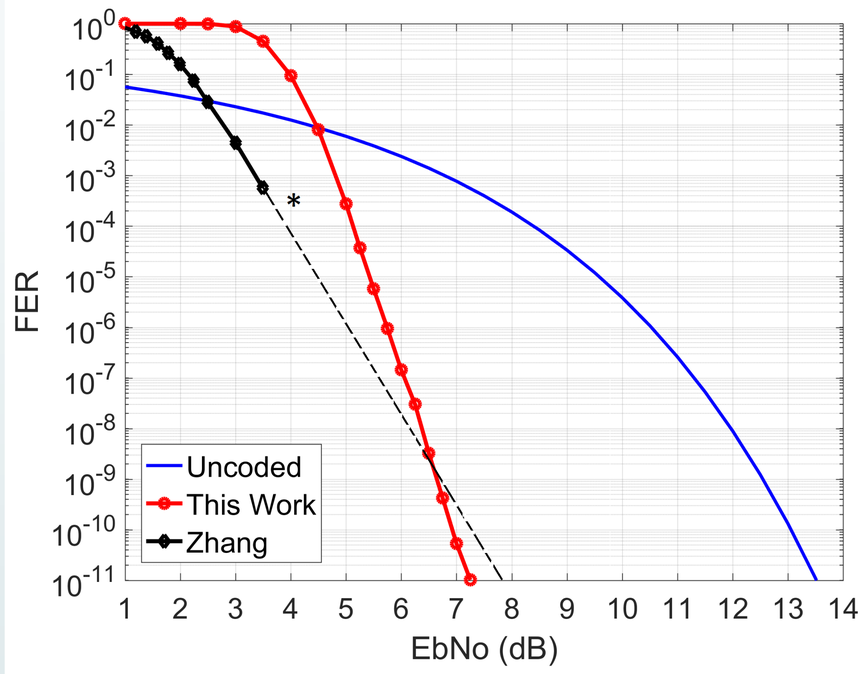
Architecture and Algorithm

This work utilizes following architecture methods:

- **Deep Pipelining:** Pipelining is a method of feeding the decoder with a new input codeword before previous codeword is fully decoded. If a decoder supports decoding a codeword at each clock cycle it reaches highest degree of pipelining which is called deep pipelining. Pipelining is required for reaching high throughput.
- **Unrolling:** Unrolled architecture utilizes dedicated logic blocks which reduces complexity and latency but sacrifices flexibility.
- **Register Balancing:** The critical path of the decoder limits the frequency and throughput. Since simpler paths are also limited by the frequency, efficiency of the decoder reduces. In order to avoid reducing the efficiency, proposed architecture merges the consecutive short paths by removing the registers in between. This approach reduces the latency and memory usage of the decoder. This method is especially effective for polar decoders due to their high locality.

When we compare this work to two other high throughput polar decoders, results show that this work has similar complexity to other decoders but it has lower latency and better communication performance even with a much higher code rate.

	This Work	P. Giard[4]	X. Zhang[5]
Algorithm	SCL	Fast-SSC	Fast-SSC
Technology (nm)	16	40	28
Code Rate	0.87	0.50	0.50
Net TP (Gb/s)	89	118	157
Logic Units	214,252	156,450	81,498
Memory Units	609,421	437,244	2,464,250
Latency (us)	0.62	2.40	1.16
Frequency (MHz)	100	231	300



* Extrapolated data shown as dashed lines.

Using the netlist provided by the Vivado and TSMC library, we calculated and scaled the estimated ASIC complexity of this work when implemented at 7nm technology. Results show that our decoder consumes slightly more power than the EPIC limits.

	EPIC	This Work
Num. of Decoders	-	2
Throughput (Gb/s)	1000	1000
Area (mm2)	10	10
Power (W)	1	1.24
Latency (us)	-	0.11
Freq. (MHz)	1000	563

Conclusion

This work shows that with the implementation of register balancing, SCL polar decoders are contenders for beyond 5G applications. Their complexity is close to SoA SC decoders and SCL counter-parts performs better.

Acknowledgements

The study has been supported by EPIC project funded by the European Unions Horizon 2020 research and innovation programme under grant agreement No 760150.
We also thank Prof. Orhan Arıkan, Altuğ Süral and Yiğit Ertuğrul for their help and valuable feedback.

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