COMBINED SKEWED CMOS RING OSCILLATOR

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ABSTRACT

A combined skewed ring oscillator by different type of delay stages is presented. This paper aims to drive a high stable and relatively high frequency but still use a full transistor circuit for ring oscillator with combined delay stages and skewed connections. First we propose two types of common inverters then calculate their delay time and analysis their dependence of delay time to variation of power supply voltage. The simulation results verify that delay time of these two CMOS inverters show opposite behaviour versus power supply changing. So a combined structure can obtain more appropriate frequency stability versus power supply noise. Also in order to increase oscillation frequency we have used the negative skewed delay connections. The simulation results using HSPICE for 0.18 µm CMOS shows a good agreement with analysis results. In addition in this paper the mathematical justification for improved functioning of this combined skewed ring oscillator has been proved. This justification shows appropriate agreement with the simulation results. From mathematical point of view the proposed ring oscillator has better frequency stability in comparison with other types of ring oscillators. In fact, the oscillation frequency sensitivity to supply voltage noise is reduced considerably.

KEYWORDS

CMOS, ring oscillator, frequency stability, delay time

1. INTRODUCTION

Oscillators are the essential part of any digital and analog systems [1, 11]. And ring oscillator is a circuit usually uses transistors without using passive elements [4]. The main reason of the tendency to design full transistor CMOS circuits is the ability of easy integration with absence of passive elements which reduces the die area [12-20]. The most significant feature of a ring oscillator is lower cost due to lower die area and design simplicity [1, 4, 5]. However the highest possible oscillation frequency is lower for ring oscillators than LC oscillator, negative skewed delay connections can improve the speed of ring type oscillators.

Several designs for ring oscillator have been reported in literature. In [1], a frequency stable oscillator is designed based on the opposite direction of delay time changing, which increase frequency stability but oscillation frequency reduce due to using current starved inverter. In [6] a method to enhance frequency operation of ring oscillators by negative skewed delay connections presented. Overall, most of the reported ring oscillators cannot improve both frequency stability and oscillation frequency. In this paper a novel design as combined skewed ring oscillator is presented to improve frequency stability an oscillation frequency simultaneously.

Usually a single ended ring oscillator can be implement using odd number of delay stages (Fig.1). Considering oscillation criterion the loop gain must be equal or bigger than unity and also the

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loop gain must be negative which odd number of inverters can satisfy these conditions. By assuming that all stages are similar we can extract oscillation frequency from (1).

$$A_1(j\omega) = A_2(j\omega) = \ldots = A_N(j\omega) = \frac{-g_m R}{1 + j\omega RC}$$

$$\left|A_1(j\omega).A_2(j\omega).\ldots.A_N(j\omega)\right| = 1 \qquad (1)$$

$$\angle \mathrm{A1}(\mathrm{j}\omega) = \theta = \tan^{-1}(\omega \mathrm{RC}) = \frac{2K\pi}{RC}$$

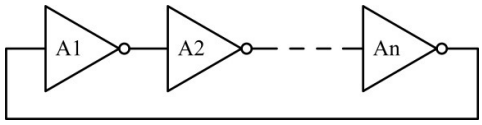

Fig.1. A typical ring oscillator by odd number of inverters [2]

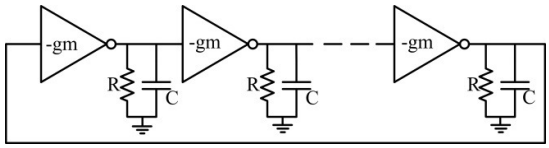

Fig.2. general linear model of a ring oscillator [1]

The above equation can leads us to estimate oscillation frequency in initial stage of oscillation but the stable oscillation frequency can be obtain from large signal analysis not from small signal mode in fig.2, since the start oscillation frequency is different with stable oscillation frequency.

A stage is an inverter and has t_d seconds delay. Since the similarity between stages is assumed, oscillation frequency can be obtained as (2).

$$f_0 = \frac{1}{2Nt_d} \qquad (2)$$

In (2) we assume that N is an odd number and illustrates the number of delay stages. In fact the starting frequency of oscillation is determined by Barkhausen criteria and stable oscillation frequency specified by inverters delay time [2]. According to (2) oscillation frequency strongly depends on delay time of delay stages. Also knowing that the number stages in a fixed structure is constant then the most significant parameters for oscillation frequency calculation is delay time. Two configurations for five stage conventional ring oscillator are shown in fig.3 and fig.4. According to fig.4 we have an option to change the oscillation frequency by adjusting Vctrl, so by using current starved inverter, voltage controlled oscillator can be designed.

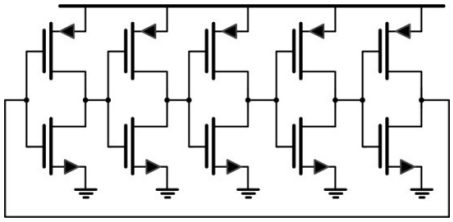

Fig.3. Five stage basic ring oscillator

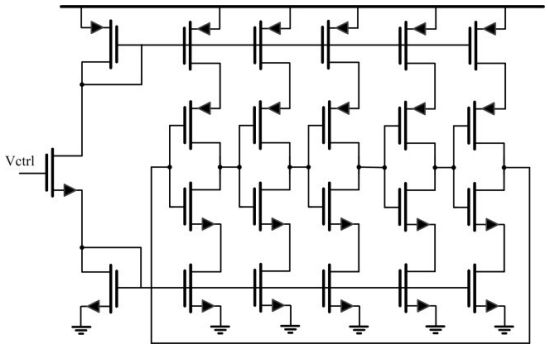

Fig.4. Five stage Current Starved ring VCO

In this paper we've calculated the delay time of basic and Current Starved inverters and based on the equations a combined skewed ring VCO will be presented.

2. DELAY TIME OF INVERTERS

General conditions of ring oscillators were discussed in previous part. In this section delay time calculations are presented since this parameter is the only parameter which can determine the oscillation frequency. By assuming two types of inverters, basic type inverter and current starved inverter (Fig.5).By applying an ideal pulse to both of these inverters, we obtain the output signal depicted in Fig.6.

Details of calculations are brought in the appendix A.

$$t_{delay} \propto \frac{\tau_{PHL}+\tau_{PLH}}{2}$$

$$\tau_{PHL} = t_2 - t_0$$

$$\tau_{PLH} = t_5 - t_3$$

$$\tau_{PHLbasic} = \frac{2C_L(1-\alpha)V_{DD}}{\mu_n c_{ox}\frac{W}{L}(V_{DD}-V_{th-nmos})^2} + \frac{C_L}{\mu_n c_{ox}\frac{W}{L}(V_{DD}-V_{th-nmos})}\ln\left(\frac{2\alpha-\beta}{\beta}\right)$$

$$\tau_{PLHbasic} = \frac{-2C_L\gamma V_{DD}}{\mu_p c_{ox}\frac{W}{L}(V_{DD}-V_{th-pmos})^2} \qquad (3)$$

$$+\frac{C_L}{\mu_p c_{ox}\frac{W}{L}\left(V_{DD}-V_{th-pmos}\right)}\ln\left(\frac{\beta-2\gamma}{\beta}\right)$$

$$\tau_{PHLCS}\propto\frac{2C_L(1-\alpha)V_{DD}}{\mu_n c_{ox}\frac{W}{L}\left(V_{GS1}-V_{th-nmos}\right)^2}+\frac{C_L}{\mu_n C_{ox}\frac{w}{L}\left(V_{DD}-V_{th-nmos}\right)}\ln\left(\frac{\alpha-\beta}{\beta}\right)$$

$$\tau_{PLHCS}\propto\frac{-2C_L\gamma V_{DD}}{\mu_p c_{ox}\frac{W}{L}\left(V_{SG2}-V_{th-pmos}\right)^2}+\frac{C_L}{\mu_p C_{ox}\frac{w}{L}\left(V_{DD}-V_{th-pmos}\right)}\ln\left(\frac{\beta-\gamma}{\beta}\right) \quad (4)$$

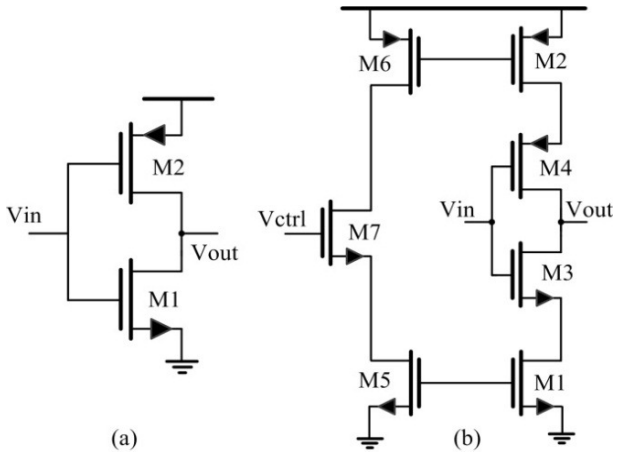

Fig.5. Basic inverter (a) and Current Starved inverter (b)

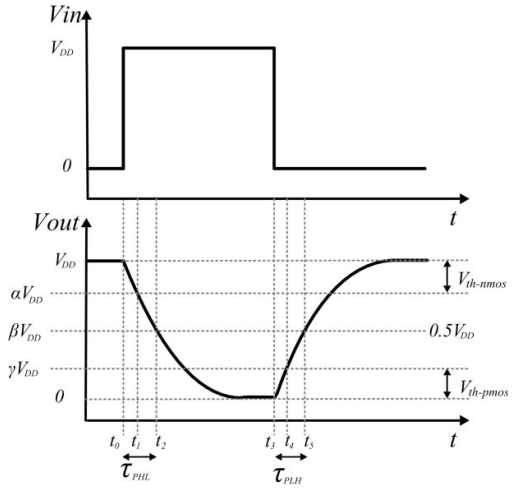

Fig.6. Input and output of inverters

In the other word:

$$\Delta t_{Basic} \propto \frac{1}{\Delta V_{DD}} \,\&\, \Delta t_{\text{CurrentStarved}} \propto \Delta V_{DD}$$

As can be seen we can conclude that delay time of these two inverters show different behaviour versus power supply changing. According to (3) and (4) delay time of basic inverter depends on power supply changing in opposite direction which delay time of current starved inverter depends on power supply changing. By considering this fact it is obvious that combined ring oscillator depicted in fig.7 can provide more stable oscillation frequency versus power supply variation. The whole loop delay in this type of oscillator can be introduce as sum of all delay times. In this case first and fifth stages are basic type inverters and other stages are current starved inverters. By summing these delay times the total delay time is less sensitive to power supply variation in comparison with basic type inverter delay time or current starved inverter delay time.

$$t_d = t_{d1} + t_{d2} + t_{d3} + t_{d4} + t_{d5} \qquad (5)$$

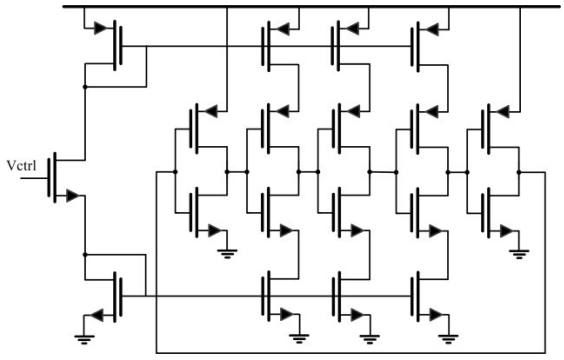

Fig.7. Combined ring VCO

Then, if all inverters are the same type t_1 , … , t_n will have the same variation. Meaning that all become smaller or bigger. In the other words changing oscillation frequency is inevitable. But in combined structure two types of inverters show opposite behaviours to power supply changing which considerably reduces the dependence of whole circuit to power supply noise. However combined ring VCO has the lower oscillation frequency compared with simple ring oscillators. By using NSD stages we can increase oscillation frequency of combined ring VCO.

3. NEGATIVE SKEWED DELAY SCHEME

In conventional inverters both PMOS and NMOS have the same input signals. NSD is a technique that reduces delay of inverters. Fig.8 shows the concept of NSD. In fact in NSD inverter input signal to PMOS arrives earlier than to the NMOS and output changing become faster as illustrated in fig.8.[6].

By using NSD stage to design a ring oscillator we need to modify the connections as shown fig.9. Also for combined ring VCO the circuit of fig.10 is suggested. The minimum number of stages in

skewed ring oscillator is five because when the number of stage is tree, the skewed ring oscillator yields a PMOS diode- connected load. By using NSD connection for combined ring oscillator we can compensate decreased oscillation frequency by changing configuration.

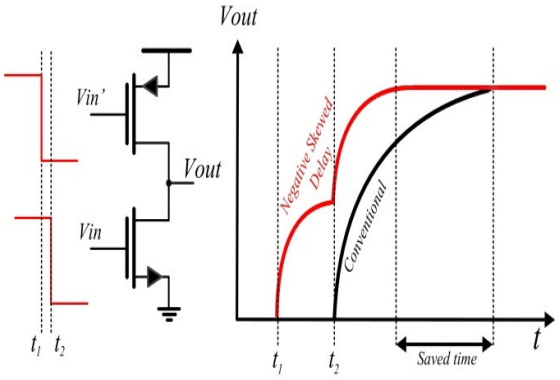

Fig. 8. NSD inverter

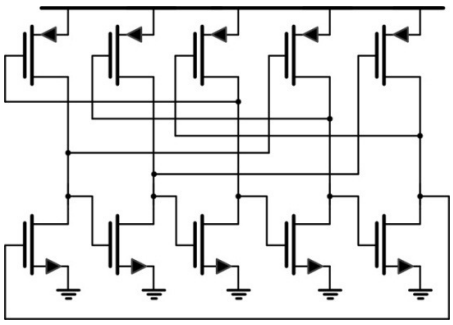

Fig. 9. Skewed ring oscillator

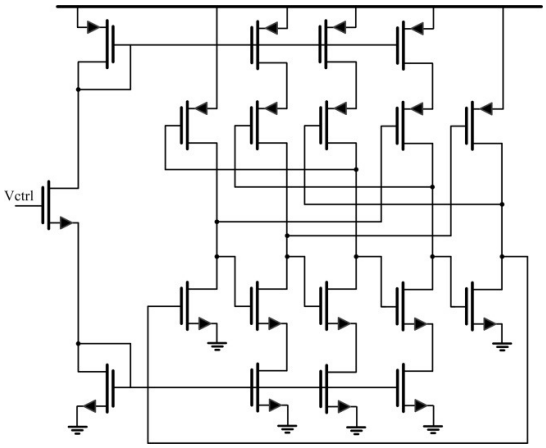

Fig. 10. Proposed Combined Skewed ring VCO

4. SIMULATION RESULTS

In order to validate the previous discussion, five structures in fig.3, fig.4, fig.7, fig.9 and fig.10 have been simulated with HSPICE using TSMC 180 nm technology. The nominal supply voltage and Vctrl have been selected equal to 1.8 V and 1.5 V respectively. Also a factor as frequency deviation is defined in [1] to compare operational performance of simulated circuits. This factor is described in (6).

$$\frac{\Delta f}{f} = \frac{f\left(V_{DD} + \Delta V_{DD}\right) - f\left(V_{DD}\right)}{f\left(V_{DD}\right)} \qquad (6)$$

In this definition f (V_{DD}+ΔV_{DD}) is the oscillation frequency when supply voltage is V_{DD}+ΔV_{DD} [1].

Fig. 11 shows frequency deviation factor for five ring oscillator that obtained from simulation. And table.1 presents a comparison between these five type ring oscillators. The simulation results verify the analysis and mathematical justifications since simple combined structure and combined structure with NDS connections show considerable reduction in frequency deviation factor. In addition using NDS connection increases the oscillation frequency for combined ring oscillator from 960MHz to 3.31GHz. The proposed combined skewed ring oscillator is a VCO due to using current starved inverter. Table.1 reports the important parameters for simulated oscillators. According to this table the proposed ring oscillator can work in higher frequencies with lower frequency deviation in compared with simple structures.

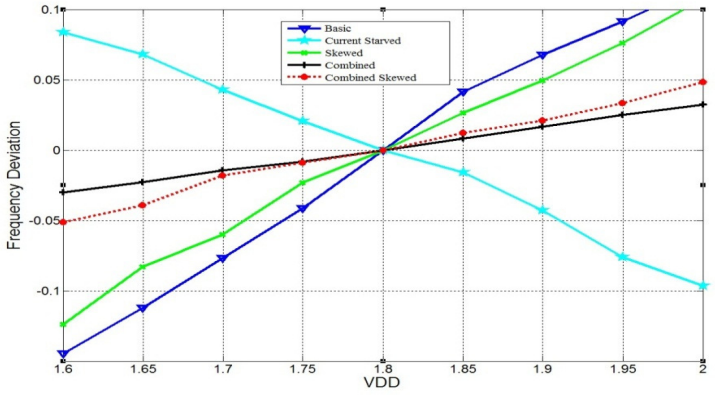

Fig. 11. Frequency deviation factor of five ring oscillators.

Tab. 1. Simulation results for five type ring oscillators

5 Stage Ring Oscillator	Baic [2]	Current Starved [4]	Skewed [6]	Combined[1]	**Combined skewed (this work)**
Number of basic type	5	0	5	2	**2**
Number of Current Starved	0	5	0	3	**3**
Number of Transistor	10	23	10	19	**19**
$\Delta f / f\,(V_{DD} \pm 0.2V_{DD})$	%13	14%	%12	%3	**%5**
$\Delta f / f\,(temp \pm 25°)$	%4	5%	%4	%0.6	**%0.8**
Oscillation Frequency	3.39GHZ	632MHz	5.65GHz	960MHz	**3.31GHz**
Is VCO?	No	Yes	No	Yes	**Yes**

5. CONCLUSION

Ring oscillators are one of the basic blocks of integrated circuits. This paper presents two types of CMOS inverters with detailed delay time calculations and then suggests combined structure for implementing an efficient VCO regarding frequency deviation. Oscillation frequency of combined ring VCO is low in respect to simple one. For increasing oscillation frequency we used NSD stages in combined structure that significantly increased oscillation frequency. The results of simulation by HSPICE for 0.18µm CMOS approve the analysis results. According to simulation results the proposed VCO can work in higher frequencies with less frequency deviation.

A.1. Appendix A

$$\alpha = \frac{V_{DD} - V_{th-nmos}}{V_{DD}}$$

$$\beta = \frac{V_{DD}}{2}$$

$$\gamma = \frac{V_{th-pmos}}{V_{DD}}$$

In order to calculate delay time of Basic type inverter (Fig.5 (a)) we can write:

$for\ t_0 < t < t_1 \qquad nmos \rightarrow saturation$

$$I_{Dn} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{th-nmos})^2 = -I_{CL} = -C_L\frac{dV_{out}}{dt}$$

$for\ \ V_{DD} - V_{th-nmos} < V_{out} < V_{DD}$

$$V_{DD} - V_{th-nmos} = \alpha V_{DD} \ \rightarrow\ 0 < \alpha < 1$$

$$\int_{t_0}^{t_1} dt = -C_L \int_{V_{DD}}^{\alpha V_{DD}} \frac{1}{I_{Dn}}\, dV_{out}$$

$$\int_{t_0}^{t_1} dt = \frac{-2C_L}{\mu_n C_{ox} \frac{W}{L}(V_{DD} - V_{th-nmos})^2} \int_{V_{DD}}^{\alpha V_{DD}} dV_{out}$$

$$t_1 - t_0 = \frac{2C_L(1-\alpha)V_{DD}}{\mu_n c_{ox} \frac{W}{L}(V_{DD} - V_{th-nmos})^2} \qquad (1A)$$

$$t_1 < t < t_2 \quad nmos \rightarrow Linear$$

$$I_{Dn} = \mu_n C_{ox} \frac{W}{L}(V_{in} - V_{th-nmos})V_{out} - \frac{1}{2}V_{out}^2$$

$$\mu_n C_{ox} \frac{W}{L}(V_{in} - V_{th-nmos})V_{out} - \frac{1}{2}V_{out}^2 = -C_L \frac{dV_{out}}{dt}$$

$$for \quad V_{out} < V_{DD} - V_{th}$$

$$\int_{t_1}^{t_2} dt = -C_L \int_{\alpha V_{DD}}^{\beta V_{DD}} \frac{1}{I_{Dn}} dV_{out}$$

$$\int_{t_1}^{t_2} dt = -\frac{2C_L}{\mu_n C_{ox} \frac{W}{L}} \int_{\alpha V_{DD}}^{\beta V_{DD}} \frac{1}{2(V_{DD} - V_{th-nmos})V_{out} - V_{out}^2} dV_{out}$$

$$t_2 - t_1 = \frac{C_L}{\mu_n C_{ox} \frac{W}{L}(V_{DD} - V_{th-nmos})} \ln\left(\frac{2\alpha - \beta}{\beta}\right) \qquad (2A)$$

$$\tau_{PHL} \propto t_2 - t_0 = (t_2 - t_1) + (t_1 - t_0)$$

$$(1A) + (2A) \overset{yields}{\rightarrow} \tau_{PHL}$$

$$\tau_{PHL} = \frac{2C_L(1-\alpha)V_{DD}}{\mu_n c_{ox} \frac{W}{L}(V_{DD} - V_{th-nmos})^2}$$

$$+ \frac{C_L}{\mu_n c_{ox} \frac{W}{L}(V_{DD} - V_{th-nmos})} \ln\left(\frac{2\alpha - \beta}{\beta}\right)$$

or

$$\tau_{PLH} \propto t_5 - t_3 = (t_5 - t_4) + (t_4 - t_3)$$

$$\tau_{PLH} = \frac{-2C_L \gamma V_{DD}}{\mu_p c_{ox} \frac{W}{L}(V_{DD} - V_{th-pmos})^2}$$

$$+ \frac{C_L}{\mu_p c_{ox} \frac{W}{L}(V_{DD} - V_{th-pmos})} \ln\left(\frac{\beta - 2\gamma}{\beta}\right)$$

Then

$$\Delta t_{Basic} \cong \frac{A_1}{\Delta V_{DD}} + \frac{A_2}{\Delta V_{DD}} + \frac{A_3}{\Delta V_{DD}} + \frac{A_4}{\Delta V_{DD}}$$

Where A_1, A_2, A_3, A_4, are constant value as follow:

$$A_1 = \frac{2C_L(1-\alpha)}{\mu_n c_{ox} \frac{W}{L}}$$

$$A_2 = \frac{C_L}{\mu_n c_{ox} \frac{W}{L}} \ln\left(\frac{2\alpha - \beta}{\beta}\right)$$

$$A_3 = \frac{-2C_L \gamma}{\mu_p c_{ox} \frac{W}{L}}$$

$$A_4 = \frac{C_L}{\mu_p c_{ox} \frac{W}{L}} \ln\left(\frac{\beta - 2\gamma}{\beta}\right)$$

to calculate delay time of Current Starved inverter (Fig.5(b)) we can write equally.

$t_0 < t < t_1$

$V_{in} = V_{DD}$,$V_{out} \in [V_{DD}$,$V_{DD} - V_{th}]$

$M3 \rightarrow saturation$,$M1 \rightarrow saturation$

$M4 \rightarrow cut\ off$

$for\ V_{DD} - V_{th-nmos} < V_{out} < V_{DD}$

$$I_{D1} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS1} - V_{th-nmos})^2$$

$$dt = -\frac{C_L}{\frac{1}{2}\mu_n C_{ox} \frac{w}{L}(V_{GS1} - V_{th-nmos})^2} dV_{out}$$

$$\int_{t_0}^{t_1} dt = -C_L \int_{V_{DD}}^{\alpha V_{DD}} \frac{1}{I_{Dn}} dV_{out}$$

$Know\ \ that\ (V_{GS1} - V_{th-nmos}) = cte$

$$\int_{t_0}^{t_1} dt = \frac{-2C_L}{\mu_n\ C_{ox}\ \frac{\mathrm{w}}{\mathrm{L}}(V_{GS1} - V_{th-nmos})^2} \int_{V_{DD}}^{\alpha V_{DD}} dV_{out}$$

$$t_1 - t_0 = \frac{2C_L(1-\alpha)V_{DD}}{\mu_n C_{ox} \frac{w}{L}(V_{GS1} - V_{th-nmos})^2} \qquad (1B)$$

$for\ \ t_1 < t < t_2$

$M3 \rightarrow linear$, $M1 \rightarrow saturation$

$$I_{D3} = \mu_n C_{ox} \frac{w}{L}(V_{GS3} - V_{th-nmos})V_{DS3} - \frac{1}{2}V_{DS3}^2$$

$$I_{D1} = \frac{1}{2}\mu_n C_{ox} \frac{w}{L}(V_{GS1} - V_{th-nmos})^2$$

$$I_{C_L} \cong -I_{D3} = C_L \frac{dV_{out}}{dt}$$

$$for V_{out} < V_{DD} - V_{th-nmos}$$

$$\int_{t_1}^{t_2} dt = -C_L \int_{\alpha V_{DD}}^{\beta V_{DD}} \frac{1}{I_{D3}} dV_{out}$$

$$\int_{t_1}^{t_2} dt = -\frac{C_L}{\mu_n C_{ox} \frac{w}{L}} \int_{\alpha V_{DD}}^{\beta V_{DD}} \frac{1}{(V_{GS3} - V_{th-nmos}) V_{DS3} - \frac{1}{2} V_{DS3}^2} dV_{out}$$

$$V_{DS3} = V_{out} - V_{DS1} \cong V_{out} \text{ and } V_{GS3} \cong V_{in} = V_{DD}$$

$$\int_{t_1}^{t_2} dt = -\frac{C_L}{\mu_n C_{ox} \frac{w}{L}} \int_{\alpha V_{DD}}^{\beta V_{DD}} \frac{1}{(V_{DD} - V_{th-nmos}) V_{out} - V_{out}^2} dV_{out}$$

$$t_2 - t_1 = \frac{C_L}{\mu_n C_{ox} \frac{w}{L}} \frac{1}{(V_{DD} - V_{th-nmos})} \ln\left(\frac{\alpha - \beta}{\beta}\right) \qquad (2B)$$

$$\tau_{PHL} \propto t_2 - t_0 = (t_2 - t_1) + (t_1 - t_0)$$

$$(1B) + (2B) \xrightarrow{yields} \tau_{PHL}$$

$$\tau_{PHL} \propto \frac{2C_L (1-\alpha) V_{DD}}{\mu_n c_{ox} \frac{W}{L} (V_{GS1} - V_{th-nmos})^2}$$

$$+ \frac{C_L}{\mu_n C_{ox} \frac{w}{L} (V_{DD} - V_{th-nmos})} \ln\left(\frac{\alpha - \beta}{\beta}\right)$$

or

$$\tau_{PLH} \propto t_5 - t_3 = (t_5 - t_4) + (t_4 - t_3)$$

$$\tau_{PLH} \propto \frac{-2C_L \gamma V_{DD}}{\mu_p c_{ox} \frac{W}{L} (V_{SG2} - V_{th-pmos})^2}$$

$$+ \frac{C_L}{\mu_p C_{ox} \frac{w}{L} (V_{DD} - V_{th-pmos})} \ln\left(\frac{\beta - \gamma}{\beta}\right)$$

Then

$\Delta t_{\text{CurrentStarved}} \cong \mathrm{B}_1 \cdot \Delta V_{DD} + \frac{B_2}{\Delta V_{DD}} + \mathrm{B}_3 \cdot \Delta V_{DD} + \frac{B_4}{\Delta V_{DD}}$ where B_1, B_2, B_3, B_4, are constant value as follow:

$$B_1 = \frac{2C_L (1-\alpha)}{\mu_n c_{ox} \frac{W}{L} (V_{GS1} - V_{th-nmos})^2}$$

$$B_2 = \frac{C_L}{\mu_n C_{ox} \frac{w}{L}} \ln\left(\frac{\alpha-\beta}{\beta}\right)$$

$$B_3 \propto \frac{-2C_L\gamma}{\mu_p c_{ox} \frac{W}{L}\left(V_{SG2} - V_{th-pmos}\right)^2}$$

$$B_4 = \frac{C_L}{\mu_p C_{ox} \frac{w}{L}} \ln\left(\frac{\beta-\gamma}{\beta}\right)$$

Or we can write:

$$B_1 + B_3 > B_2 + B_4$$

Since

$$0 < \left|V_{GS,SG} - V_{th-n,p}\right| < 1 \rightarrow \left|V_{GS,SG} - V_{th-n,p}\right|^2 \square\ 1$$

$$\frac{2C_L(1-\alpha)}{\mu_n C_{ox} \frac{w}{L}\left(V_{GS1} - V_{th}\right)^2} > \frac{2C_L(1-\alpha)}{\mu_n C_{ox} \frac{w}{L}}$$

$$\frac{2C_L(1-\alpha)}{\mu_n C_{ox} \frac{w}{L}\left(V_{GS1} - V_{th}\right)^2} > \frac{C_L}{\mu_n C_{ox} \frac{w}{L}} \ln\left(\frac{\alpha-\beta}{\beta}\right)$$

$$\frac{-2\gamma C_L}{\mu_p C_{ox} \frac{w}{L}\left(V_{SG2} - V_{th-pmos}\right)^2} > \frac{C_L}{\mu_p C_{ox} \frac{w}{L}} \ln\left(\frac{\beta-\gamma}{\beta}\right)$$

Then

$$B_1 > B_2 \;\&\; B_1 > B_4$$

$$B_3 > B_2 \;\&\; B_3 > B_4$$

So $B_1 + B_3 > B_2 + B_4$

In summary

$$\Delta t_{Basic} \propto \frac{1}{\Delta V_{DD}}$$

$$\Delta t_{\text{CurrentStarved}} \propto \Delta V_{DD}$$

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