Synchronization of multiple USRP SDRs for coherent receiver applications

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Abstract—This paper describes the necessary means to combine multiple Ettus Research USRP X310 software-defined radios to a multichannel coherent receiver for direction-of-arrival (DoA) and passive radar applications. The requirements to combine several software-defined radios to a multichannel coherent receiver are examined in general. In particular the requirement of phase coherence necessitates a closer look on the receiver synchronization, since the straightforward approach of synchronizing the systems with a common reference clock will in most cases lead to phase ambiguities between the channels. The mechanism inducing these phase ambiguities between several systems that are phase-locked to a common reference is discussed in detail. Results regarding the achieved phase stability and a preliminary measurement demonstrating the DoA capabilities of the system are shown.

I. Introduction

Software-defined radios (SDRs) provide a great degree of freedom for various transceiver applications and are also used for multichannel applications like passive radar systems and direction-of-arrival (DoA) measurement setups [1], [2]. For such multichannel receiver applications, coherence between the individual channels is a fundamental requirement [3], [4]. To achieve coherence, most SDR systems are capable of synchronization with a common 10 MHz reference and some are also equipped with the means to share the local oscillator (LO) signals directly.

In this paper we describe the necessary means to combine multiple commercially-available software-defined radios to a multichannel coherent receiver system, using two Ettus Research USRP X310 SDRs. We will take a closer look on the mechanisms that lead to phase ambiguities in systems that are synchronized with a common reference signal. We will explain in which cases this approach suffices for a phase-ambiguity-free setup and when further steps for the synchronization are necessary. These effects are also clarified with exemplary measurements. Finally, we will demonstrate a setup that ensures reliable synchronization of an arbitrary number of SDR systems. We will demonstrate this setup with two Ettus X310 SDRs, combining four TwinRX daughterboards, resulting in an eight channel system with fixed initial phase relation. For this system long-term phase drift and a phase deviation on startup measurement are shown. An exemplary DoA measurement, conducted with the described setup, completes this paper.

II. System description

A software-defined radio receiver is composed of an analog front-end and a subsequent analog-to-digital conversion. The analog front-end, which is basically a configurable analog receiver, converts a specified part of the spectrum down to a lower frequency band, where it can be converted to the digital domain. The digital receiver then performs baseband processing and, if necessary, demodulation by means of digital signal processing, which offers a great degree of flexibility.

The Ettus Research USRP X310 SDR features several ADCs and DACs as well as an Kintex 7 FPGA, which provides the platform's digital signal processing capabilities. Various high-speed interfaces can be used to offload the baseband data to a computer, which performs further data processing, and at the same time controls the SDR.

Each USRP is equipped with two slots for various analog front-ends, which are called daughterboards. One slot can handle a signal bandwidth up to 160 MHz.

To allow basic synchronization between several USRP devices, the hardware is equipped with signal sources and distribution capabilities for a 10 MHz reference signal and a one pulse per second (1 PPS) signal. However, as we will see in Sec. III, synchronization by means of the 10 MHz reference signal does not ensure a well-defined phase relation between the individual channels.

The setup presented in this paper combines two Ettus Research USRP X310 SDRs with a total of four TwinRX daughterboards to build an 8-channel coherent software-defined receiver. The Ettus Reseach TwinRX daughterboards support a frequency range from 10 MHz to 6 GHz and a bandwidth of up to 80 MHz per channel. Each channel is set up as a two-stage superheterodyne receiver.

III. Synchronization of the analog front-ends

The first and major task in building a coherent SDR setup is, similar to the setup of any coherent multichannel receiver, the synchronization of the analog receiver front-ends. To achieve this, we take a closer look on the TwinRX architecture [5], [6]. Figure 1 shows a simplified block diagram of a single channel of a TwinRX daughterboard. It can be seen that the LO signals for the two mixers can either be generated by two internal oscillators or can be provided by the other daughterboard using the connectors depicted on the left. This option shall be referred to as LO sharing. A third option is
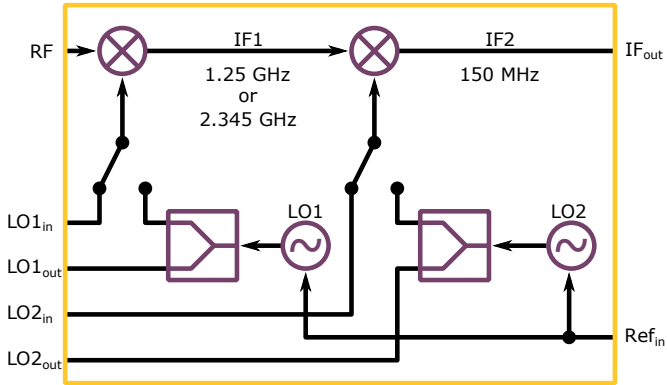
Fig. 1. Simplified block diagram of a single channel of a TwinRX daughter-board

to use internal switches (not shown in Fig. 1) to feed one channel of a daughterboard with the LOs generated by the daughterboard's other channel.

A. LO generation using the internal PLLs

If the daughterboard's internal PLLs are used, the LO signals are derived from a common reference signal (Ref$_{\text{in}}$ in Fig. 1). As a consequence the LOs' phases are locked among each other. Regarding synchronization, the problem with this method is that a locked phase does not necessarily mean that there is no phase ambiguity between the reference signal and the LO signal, which would result in a phase ambiguity between the system's channels.[1] To avoid these phase ambiguities, it would be possible to use an additional synchronization signal or to restrict the divider ratios to certain special cases, where no additional synchronization is necessary (cf. [7]).

To elaborate this point, consider the well-known block diagram of a standard PLL circuit depicted in Fig. 2.[2] Two dividers, namely the reference divider with a divider ratio R and the feedback divider with a divider ratio of N realize the relation

$$f_{LO} = \frac{N}{R} \cdot f_{ref} \tag{1}$$

between the reference signal and the LO signal.[3]

If the PLL is locked, the phase relation

$$\frac{1}{N}\varphi_{LO} + \frac{2\pi}{N}c_1 = \frac{1}{R}\varphi_{ref} + \frac{2\pi}{R}c_2, \tag{2}$$

applies at the phase detector where $2\pi/N \cdot c_1$ and $2\pi/R \cdot c_2$ represent phase ambiguities introduced by the frequency dividers. The coefficients $0 \leq c_1 \leq N-1$ and $0 \leq c_2 \leq R-1$ are integers which are arbitrarily determined during the PLL's startup.

[1]For completeness, it should be mentioned that such a phase ambiguity could be corrected by performing a calibration of the system after each frequency change, as is demonstrated in [4].

[2]We are considering only integer-N PLLs here.
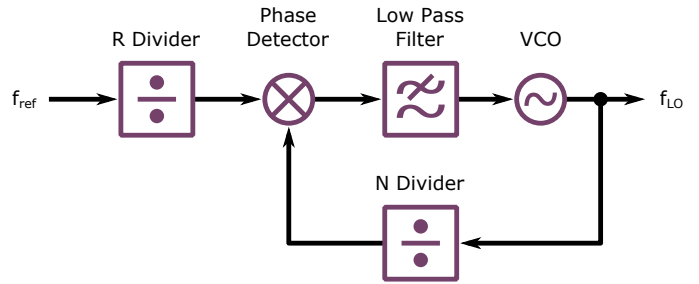
[3]Both dividers are integer values.

Fig. 2. Block diagram of an integer-N PLL, after [8]

Rearranging (2) for φ_{LO} yields

$$\varphi_{LO} = \frac{N}{R}\varphi_{ref} + 2\pi\left[\frac{N}{R}c_2 - c_1\right] \tag{3}$$

and by defining

$$O = 2\pi\left[\frac{N}{R}c_2 - c_1\right] \tag{4}$$

for the additional arbitrary phase offset, (3) is rewritten as

$$\varphi_{LO} = \frac{N}{R}\varphi_{ref} + O. \tag{5}$$

For the given applications, a well-defined phase relation between φ_{ref} and φ_{LO} is mandatory and thus we require

$$O = 2\pi\left[\frac{N}{R}c_2 - c_1\right] \stackrel{!}{=} 2\pi k \tag{6}$$

where k is an arbitrary integer. From (6) follows directly that

$$k = \left[\frac{N}{R}c_2 - c_1\right] \tag{7}$$

applies, which may only be an integer value if the ratio N/R is integer.

Several important conclusions can be drawn from this finding: If the reference divider is disabled ($R = 1$), a well-defined phase relation is guaranteed for every N. In contrast, if both the reference and feedback divider are used, only integer ratios N/R ensure the desired phase relation.

For the general case of arbitrary (i.e. possibly non-integer) ratios N/R the number of the PLL's ambiguous locking states can be determined by careful analysis of (4).

By rearranging (4) as

$$O = 2\pi \cdot \frac{N}{R}c_2 - 2\pi \cdot c_1 \tag{8}$$

it can be seen that only the arbitrary coefficient c_2 introduced by the reference divider can cause a phase ambiguity which is not an integer multiple of 2π while the coefficient c_1 introduced by the feedback divider leads to a negligible ambiguity of integer multiples of 2π.

We thus define the non-negligible phase offset as
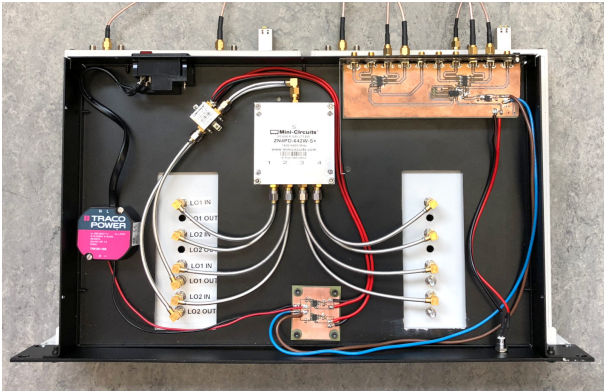
$$O' = 2\pi \cdot \frac{N}{R} \cdot c_2. \tag{9}$$

Fig. 3. LO and reference distribution with two USRPs X310 beneath

Fig. 4. Simplified block diagram of an Ettus Research USRP X310

From (9) it is obvious that the number of possible ambiguous states is equal to

$$M = \frac{R}{\gcd(N, R)} \qquad (10)$$

which is in fact the denominator of the reduced fraction N/R. While using PLLs with N and R being chosen correctly ensures both coherence and ambiguity-free phase relations between the individual channels, the limitations regarding proper values for N and R drastically decrease the system's flexibility because the output frequency is limited to integer multiples of the reference frequency as can be seen from (1).

At first sight, using fractional-N PLLs rather than integer-N PLLs might alleviate those limitations to some extend. However, because the internal state of the fractional-N feedback dividers can usually not be synchronized [9] a well-defined phase relation is not guaranteed.

B. LO sharing between daughterboards within one USRP

As already mentioned earlier, LO sharing allows to provide the four channels of the USRP's two daughterboards with the LOs generated by one of the system's channels. Thus, a single URSP equipped with two TwinRX daughterboards can be used as a 4-channel coherent receiver, which does not exhibit any phase ambiguity between the individual channels. LO sharing is well documented in [10].

C. Synchronization of the front-ends of more than one USRP

If more than four coherent receiver channels with a well-defined phase relation are needed, the LO signal, which is generated by one of the TwinRX daughterboards, has to be distributed using additional external hardware. To realize a system with 8 coherent receivers, we distribute the LO signals of one TwinRX channel using two 1:4 power dividers. Two additional amplifiers are used to mitigate the drop of signal power. The hardware setup is depicted in Fig. 3.

We use Minicircuits ZN4PD-642W+ 4 Way 0 degree power splitters, which are specified for a frequency range from 1600 MHz to 6400 MHz and therefore cover all possible LO frequencies provided by the TwinRX daughterboards. The amplifiers used are Minicircuits ZX60-V83+ with a frequency range from 20 MHz to 4700 MHz and a typical gain of 15 dB.
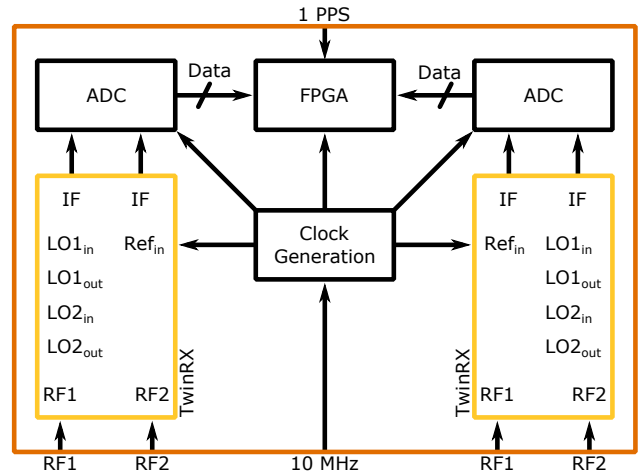
IV. SYNCHRONIZATION OF THE ADCS AND FPGAS

Using the LO distribution setup described in the previous section ensures that the received signals are coherent and exhibit a well defined phase relation at the interface between analog and digital domain. To realize a fully coherent receiver, it is furthermore necessary to ensure synchronization of the ADCs and the digital domain.

The clock for the FPGAs and the ADCs is derived from a common 10 MHz reference signal, which can be fed into each USRP as shown in the simplified block diagram of the USRP depicted in Fig. 4. In our setup, the 10 MHz reference signal is generated externally and distributed to both USRPs in order to achieve synchronous operation.

Because the ADCs run at a fixed frequency of 200 MHz, no frequency ambiguity occurs between the ADCs, since the ADCs' operating frequency is an integer multiple of the 10 MHz reference signal. Additionally, the USRP provides a 1 PPS input, which is used to align the operations within the FPGAs. Once aligned, each FPGA has an internal counter, which can be used to synchronize commands like the begin of a recording or a switch in frequency.

The system's overall LO and clock distribution architecture is shown in Fig. 5. The 10 MHz reference clock is generated by an IQD temperature-compensated crystal oscillator (IQXT-220-1) and distributed using a Texas Instruments bus buffer IC (SN74LS125A). The 1 PPS signal is derived from this reference frequency using a microcontroller (ATTiny44) and also distributed using the SN74LS125A buffer IC.

V. CALIBRATION

The clock distribution architecture introduced in Sec. III and IV allows the receiver's eight channels to operate in a fully coherent fashion with a well-defined, that is, ambigious-free phase relationship between the individual channels.

Nevertheless, there is a remaining constant phase difference between the channels, which is mainly caused by length
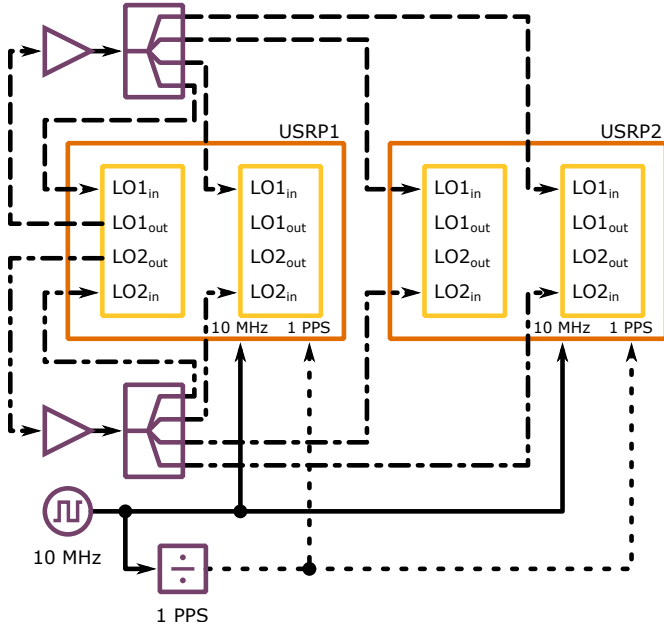
Fig. 5. Block diagram of the proposed LO and clock distribution architecture

Fig. 6. Block diagram of the phase ambiguity measurement setup

Fig. 7. Distribution of the phase error of two integer-N PLLs in steps of $90°$ for different divider values

mismatch in the LO distribution network.[4] In order to correct this phase difference a one-time calibration of the system is still necessary. Typically, this calibration is performed by recording a continuous-wave test signal, which is applied to each channel with a known phase offset. Then, by aligning the phases of the signals received on the individual channels, the constant phase errors of the channels are determined.

VI. MEASUREMENTS

To illustrate the effect of phase ambiguity with integer-N PLLs and to verify the performance of the LO-sharing synchronization, we conducted several measurements. The first set of measurements regarding the phase ambiguities between synchronized integer-N PLLs were carried out with two Analog Devices ADF4159 evaluation boards. As these boards allow complete control of the device down to setting of individual registers, operation in integer-N mode was guaranteed for the measurements. The second set, regarding the synchronization between the SDR channels were carried out using the Ettus X310 SDR system described above configured in the LO sharing synchronization scheme.

A. Phase ambiguities of integer-N PLLs

For this measurement, two ADF-4159 evaluation boards were used, to achieve a synchronized setup. Both boards were driven with a common 100 MHz reference frequency, generated with a TTI TGR6000 signal source. To evaluate the phase relationship between the two signals, the VCO outputs

[4]Another problem with the LO distribution is that the mixers of the channel generating the LO can only be supplied with the LO using the channel's internal routing facilities rather than via the channel's input for external LOs. While from our understanding of the hardware the latter approach should be possible as well, the firmware does not allow this option.
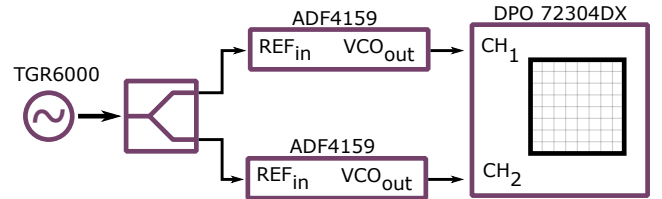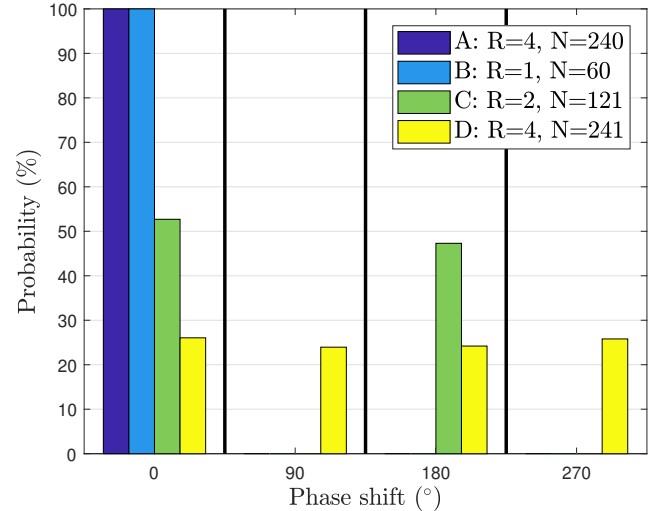
were recorded with a Tektronix DPO72304DX oscilloscope. The measurement setup is depicted in Fig. 6. For each data point, the PLLs were forced to re-lock, by toggling the reference signal. After the PLLs had sufficient time to lock again, the phase difference between the two VCO signals was examined. Each measurement consists of 2000 data points, where the phase difference of each data point relative to the first measurement is evaluated. In Fig. 7 the probability of the phase difference is shown for different settings of the R and N divider. It is clear, that if the restrictions described in Sec. III are met (measurement A and B) there is no phase ambiguity. For the divider combination R=2 and N=241 (measurement C), two phase states are possible ($0°$ and $180°$), as it is described in equations 9 and 10. The same is true for measurement D, where we can observe four phase states ($0°$, $90°$, $180°$ and $270°$) for a divider combination of R=4 and N=121.

B. USRP phase deviation for multiple power-up cycles

Firstly, the phase deviation between the eight USRP channels was measured for 80 power-up cycles of the system using a common test signal at 2.45 GHz. For each start-up, the calibrated phase of the channels 2-8 is compared to the system's first channel, thus giving a total of $(8−1)·80 = 560$ data points for the phase deviation.

The distribution of the calibrated phase deviation of channels 2-8 is depicted in Fig. 8. From this figure, it can be seen that the maximum phase deviation is below $±0.8$ degrees,
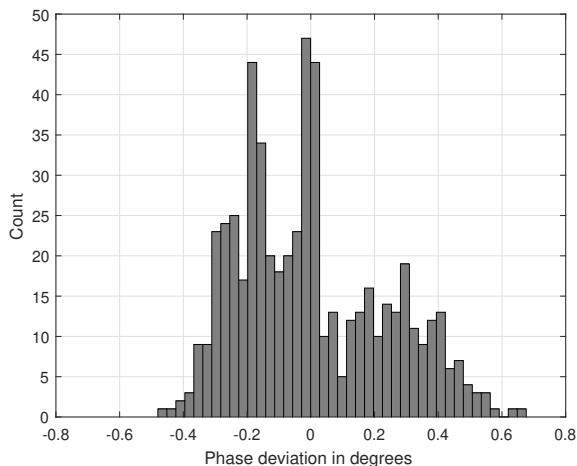
Fig. 8. Phase distribution for multiple starts of the system including a full restart of the hardware after every measurement

Fig. 9. Phase drift of the channels over time referenced to the average phase of all 8 channels

which shows that the receiver's synchronization works both accurate and reliable.

C. USRP phase stability over time

Additionally, we measured the phase error over a period of 60 minutes to verify phase stability over time. For this measurement, again a 2.45 GHz test signal was used. Fig. 9 depicts the phase drift of the individual channels referred to the average phase of all 8 channels. The drift of all channels over the observed period of time is well below ± 0.2 degrees, which is a very good result that again underlines the reliability of the system's synchronization.
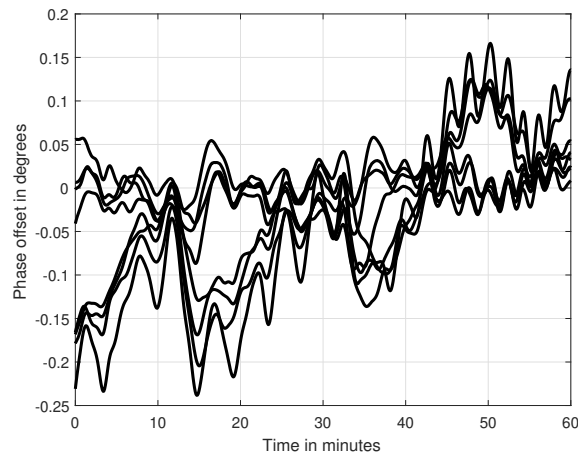
VII. APPLICATION: EXEMPLARY DoA MEASUREMENTS

The main application of the presented system are DoA measurements. In order to demonstrate the capabilities of the system, DoA measurements using an 8-element uniform linear patch antenna array for the 2.4 GHz ISM band were carried out. A quadrocopter, which emits a video downlink in this frequency band, was used to mimic the target to be detected.

Figure 10 shows two DoA measurements for the quadrocopter being located at 90 and 120 degrees. Our system is both capable of detecting the target as well as of correctly determining the DoA of the target's emission. For completeness, it should be mentioned that the DoA determination is implemented using a narrowband phaseshift delay-and-add beamforming approach [11, pp. 23–32].

VIII. CONCLUSION

In this paper, we examined possible synchronization schemes for multiple SDR receivers. We described a way for phase unambiguous synchronization using only a common reference signal under the restriction of using integer-N PLLs and limiting the LO frequencies to integer multiples of the reference frequency and described the effects leading to an ambiguous phase in systems synchronized with a common reference signal.

Fig. 10. DoA measurement with one target at 90 degrees and 120 degrees

We also described a costlier, but unrestrained usable synchronization scheme, in which the LO signal is distributed between the receivers using additional external hardware. For this synchronization scheme, we presented an LO and clock distribution architecture, which allows to synchronize multiple USRPs in order to set up an 8 channel coherent receiver system.

We investigated both the phase deviation for multiple power-up cycles (± 0.8 degrees) as well as the phase stability over time (± 0.2 degrees over 60 minutes) of this setup and confirmed the aptitude of our setup for coherent receiver applications.

Finally, an exemplary DoA measurement confirms the suitability of the system for the applications considered in this paper.

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