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A Series-Resonant Charge-Pump-Based Rectifier with Inherent PFC Capability

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Abstract—This paper presents a power factor correction (PFC) rectifier for single-phase offline converters. With the addition of a charge pump circuit comprised of a capacitor and a diode to a class-DE series-resonant converter, PFC is achieved inherently. The converter operation is based on soft-switching, and a 1 MHz 50 W prototype employing wide bandgap devices is implemented, achieving a power factor of 0.99 and a total harmonic distortion (THD) of 8.6 %, at an efficiency of 84 %, with substantially low input current harmonic magnitudes compared to the limits set by the IEC 61000-3-2 standard.

Keywords—AC-DC power conversion, rectifiers, power factor correction, resonant power conversion, wide bandgap semiconductors.

I. INTRODUCTION

With the recent advancements in industrial electronics that aim for added performance, reliability, and portability, there exists a great demand for new technologies in power converters that can cope with such trend. Pulse-width-modulated (PWM) converters have been the primary candidate for offline converters for years, thanks to their high efficiency and power quality. However, they typically operate at low frequencies in order to limit the switching losses, as their operation is based on hard-switching. On the other hand, resonant converters allow for the utilization of soft-switching techniques through the intrinsic alternating behavior of the currents and voltages through the switches, thus expensing substantially lower switching losses, making them a good candidate for operation at higher frequencies, which has many benefits including the smaller sizes for the passive components, higher power densities, higher loop-gain bandwidths, and faster transient responses. This has led to the investigation of their adoption into different applications typically dominated by PWM converters [1]-[5].

The typical solution for offline converters is a two-stage architecture, as shown in fig. 1, where the first stage is an AC-DC power factor correction (PFC) rectifier, followed by an energy storage capacitor to filter the double-the-line (100/120 Hz) frequency component, while the second stage is a DC-DC converter providing the voltage and current levels that apply to the load electrical characteristics. This conversion has to comply with a number of regulations dictating the shape of the input current and harmonic limits to reduce the mains voltage distortion [6][7].

This paper presents a resonant PFC rectifier for the first stage in single-phase offline converters. The proposed rectifier, shown in fig. 2, incorporates an input filter and bridge, a charge pump

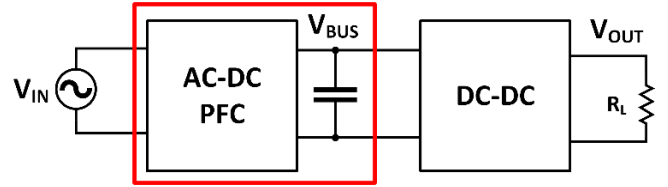


Fig. 1. Offline converter structure. The red box outlines the focus of this work.

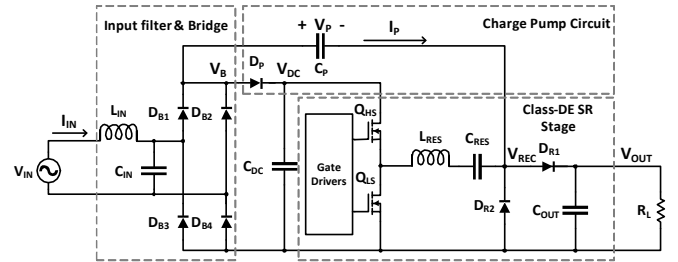


Fig. 2. Proposed PFC rectifier.

circuit, a DC energy storage capacitor, and a class-DE series-resonant converter.

The paper is organized as follows. Section II overviews the principle of operation. The implementation process is illustrated in section III. Experimental results and waveforms are presented in section IV. Eventually, conclusion is provided in section V.

II. PRINCIPLE OF OPERATION

A. Class-DE Resonant Stage Operation

A resonant converter is comprised of two stages [8], as shown in fig. 3. First, an inverter that employs a switch network which converts the DC (or low frequency AC) input to a high frequency AC output, followed by a resonant tank that provides AC-AC gain. The second stage is a high frequency AC-DC rectifier, where energy is tapped off the resonant tank and delivered to the load. In this work, a class-DE stage is used in the converter, which combines the low-voltage stress of class-D converters and the zero voltage switching (ZVS) capabilities of class-E converters [9]. Accordingly, the half-bridge switches are rated for the converter peak input voltage, and with a proper switching frequency and dead-time adjustment, the resonant tank current charges/discharges the output capacitances of the switches, such that their voltages reach the appropriate rail voltage before switching the gate, thus ensuring ZVS. That, in turn, allows for design at higher switching frequencies while achieving high efficiencies.

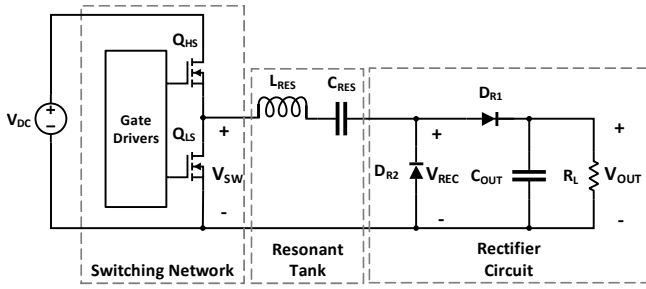


Fig. 3. Class-DE series-resonant converter.

B. Charge Pump Circuit Operation

A charge pump electronic ballast circuit was reported in [10]. Through the addition of a capacitor and a diode to a conventional high-frequency inverter circuit, the input current can be regulated to follow the input voltage. In this design, a series-resonant inverter circuit is used and a high-frequency rectifier is added for enabling use in AC-DC converters, where the energy storage capacitor is moved to the converter input to allow for soft-switching operation with the varying AC line voltage.

An equivalent circuit for the charge pump is shown in fig. 4, with C_P and D_P referring to the pump capacitor and diode, D_B to the input bridge, C_{DC} to the energy storage capacitor, while the rectifier input, to which the pump capacitor is coupled, is modelled by an independent high frequency voltage source V_{REC} . The DC capacitor C_{DC} is designed in accordance with the pump capacitor C_P , such that the voltage V_{DC} is always higher than V_{IN} , and thus the diode bridge D_B and the pump diode D_P do not cross-conduct. Consequently, the input current is equal to the positive charging current of the pump capacitor C_P .

Fig. 5 shows the low-frequency operation of the pump circuit, where the pump capacitor is charged and discharged within the fall and rise times of V_{REC} respectively, and the charge ΔQ_P is proportional to the voltage difference across the capacitor V_P , which varies between a low-frequency high-value V_{P_high} and a constant low-value V_{P_low} . The circuit design ensures that the charge variation of C_P , which is proportional to the voltage variation across it ($V_{P_high} - V_{P_low}$), follows the input voltage V_{IN} across the line cycle (50/60 Hz). Accordingly, the average input current follows the input voltage and a unity power factor can ideally be obtained.

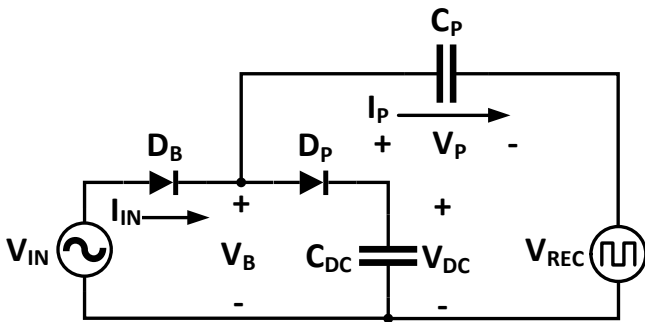


Fig. 4. Charge pump equivalent circuit.

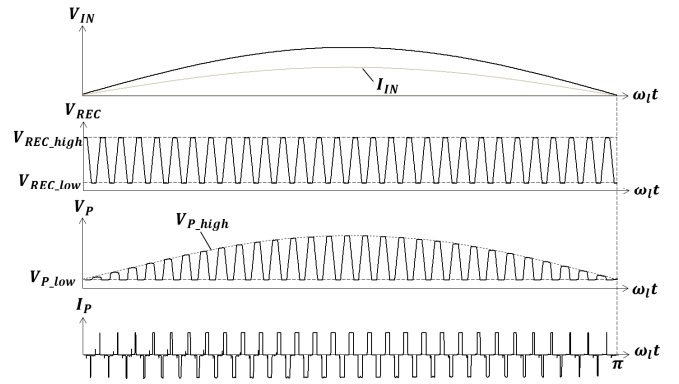


Fig. 5. Low-frequency operation across half a line cycle (50 Hz).

Fig. 6 shows the high-frequency operation across two switching cycles, and includes waveforms illustrating the converter operation at the maximum power point ($\omega_l t = \pi/2$, with ω_l being the line frequency) to illustrate the charge pump circuit operation. Across every switching cycle, at steady-state, the operation spans four intervals as follows.

In the first interval, the voltage V_B is lower than the DC capacitor voltage V_{DC} and higher than the input voltage V_{IN} , so both the diode bridge and the pump diode are off and no current flows through the pump capacitor C_P and the voltage V_P is constant (V_{P_low}). The V_{IN} waveform in figure refers to the voltage on the node interfacing the LC-filter and the diode bridge.

The second interval takes place across the fall time of V_{REC} . Once V_{REC} starts to decrease, V_B has to decrease along, until D_B gets forward biased and V_B gets pulled to V_{IN} . While V_{REC} continues decreasing, with V_B constant (as the grid frequency is significantly lower than the frequency of V_{REC}), V_P increases and C_P is charged by the line current I_{IN} , until V_{REC} reaches its low-value and V_P reaches its high-value, where

$$V_{P_high} = V_{IN} - V_{REC_low} \quad (1)$$

The third interval begins once V_{REC} settles at the low-value, where C_P stops charging while D_P still blocks. Similar to the first interval, no current flows through the pump capacitor and V_P is constant.

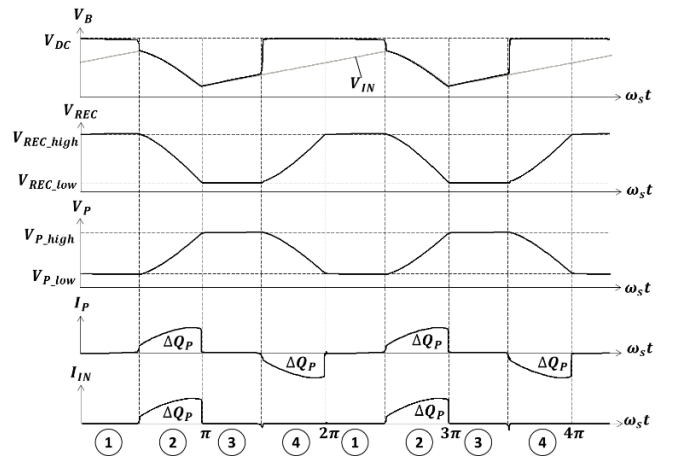


Fig. 6. Operation across two switching cycles.

Eventually, the fourth interval takes place across the rise time of V_{REC} . Once V_{REC} starts to increase, V_B has to increase along until D_P gets forward biased and V_B gets pulled to V_{DC} . While V_{REC} continues increasing, with V_{DC} constant, V_P decreases and C_P discharges into the resonant tank, until V_{REC} reaches its high-value, V_{REC_high} , and V_P reaches its low-value, where

$$V_{P_low} = V_{DC} - V_{REC_high} \quad (2)$$

By the end of the fourth interval, operation enters interval 1 again and the cycle repeats. The analysis shows that the input current is discontinuous and only flows into the circuit during the second interval.

For a series-resonant converter, the voltage V_{REC} varies between V_{OUT} and 0 V, where (1) and (2) can be evaluated as follows

$$V_{P_high} = V_{IN} - V_{REC_low} = V_{IN} - 0 = V_{IN} \quad (3)$$

$$V_{P_low} = V_{DC} - V_{REC_high} = V_{DC} - V_{OUT} \quad (4)$$

The equations show that the high-values for the voltage across the pump capacitor take the envelope of the input voltage, while the low-values take the envelope of the difference between the resonant converter input and output voltages, which can be considered constant in high frequency. Across one switching cycle, the variation of charge in the capacitor is

$$\begin{aligned} \Delta Q_P &= C_P \cdot \Delta V_P = C_P (V_{P_high} - V_{P_low}) \\ &= C_P (V_{IN} - V_{DC} + V_{OUT}) \end{aligned} \quad (5)$$

The pump capacitor charging current, which is equal to the input current, averaged across one switching cycle is equal to

$$I_{IN} = \frac{\Delta Q_P}{T_s} = f_s \cdot \Delta Q_P = f_s \cdot C_P (V_{IN} - V_{DC} + V_{OUT}) \quad (6)$$

where f_s is the converter switching frequency. Considering that the class-DE stage operates near resonance with a high gain close to 1, the difference between V_{DC} and V_{OUT} will be very small. Therefore, at steady state, for a constant switching frequency, the pump capacitor charging current, and accordingly the input current, become proportional to the input voltage, resulting in a high power factor and low total harmonic distortion (THD).

III. IMPLEMENTATION

A prototype is designed and implemented, targeting low to mid power range applications supplied from European mains. A switching frequency of 1 MHz is specified for the design, as it constitutes a good trade-off between converter size and efficiency, with respect to the range of frequencies that the state-of-the-art magnetic materials allow for. The converter is implemented and assembled on a two-layer printed circuit board (PCB). Fig. 7 shows a photograph of the implemented prototype power stage.

Considering the charge pump circuit operation, high frequency AC current runs through the input bridge, which is implemented using four fast-recovery diodes. In addition, as the resonant tank carries both the charge pump circuit current as well as the current to the output load, high current stress takes place at the peak of the input power, which requires custom design of the resonant inductor. For such application with high

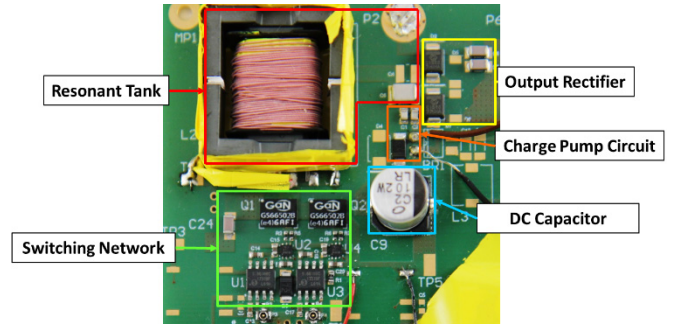


Fig. 7. Prototype power stage.

frequency AC current, the choice of the magnetic material is of key importance. Fig. 8 shows a comparison of several high-frequency magnetic materials in terms of core losses at 1 MHz [11][12]. The 3F46 material is chosen as it shows the lowest core losses at the operational switching frequency. The inductor is designed with 52 turns of two parallel layers of 20×0.05 mm Litz wire wound on an EFD 25/13/9 core. An airgap of 1.2 mm, distributed across the three legs of the core, adjusted the desired inductance.

With respect to the selection of switches, fig. 9 shows a comparison based on datasheet parameters between the best-in-class switches figures of merit [13]-[15], where gallium nitride FETs show superior performance in that voltage range compared to the silicon super-junction and silicon carbide counterparts. Device 6 (GS66502B) is used for the inverter half-bridge design. For the rectifier side, silicon carbide schottky diodes (GB01SLT06-214) are employed, as they result in higher efficiency compared to the silicon high-voltage counterparts.

Table I lists the proposed converter power-stage bill of materials (BOM). The switches gate driving circuit is comprised of a digital isolator (Si8610BC by Silicon Labs) and a gate driver (UCC27611 by Texas Instruments) for each of the high side and low side switches. For the high side driver supply, a bootstrap network of a diode (GB01SLT06-214, SiC Schottky) and a capacitor (1 μ F, ceramic X7R) is used, in addition to a peripheral

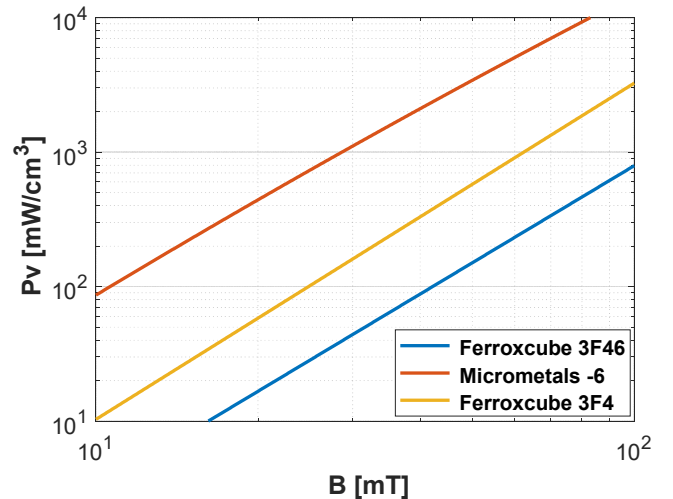


Fig. 8. Core power loss density (P_v) vs. magnetic flux density (B) for different magnetic materials at 1 MHz.

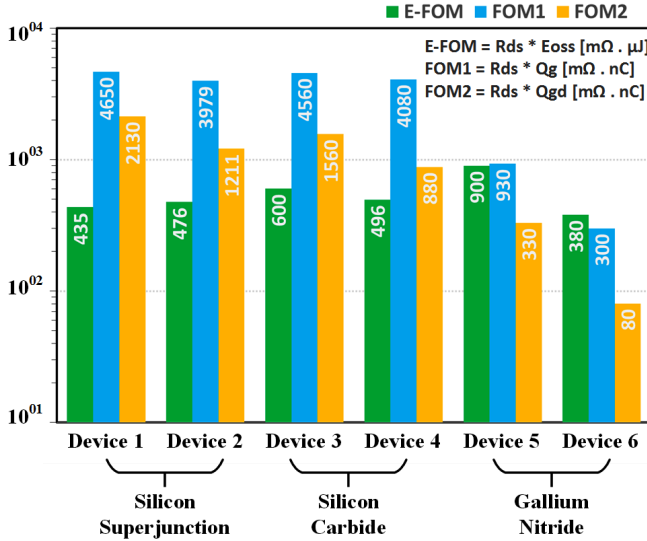


Fig. 9. Summary of the best-in-class switching devices figures of merit.

solution comprised of isolated power supplies (MTE1S0506MC by Murata), and both circuits are equally operational.

IV. EXPERIMENTAL RESULTS

A. Lab Setup

A thermal camera (Flir T650SC) continuously monitors the converter operation and a 1 GHz scope (LeCroy Wavesurfer 104MXS-B) displays the high frequency signals including switching node voltage, inductor current, and gate-signals, where the dead-time is adjusted and fixed at a point where soft-switching is achieved and the average devices temperature is minimal. Another 200 MHz scope (LeCroy Wavesurfer 24Xs-A) is used to display the low frequency signals, which include the input and output voltages and input current. A low voltage DC power supply (Rohde & Schwarz HMP2020) supplies the driving circuit, while a high voltage AC power supply (Keysight AC6802A) emulates the AC mains. A 120 MHz dual-channel waveform generator (Keysight 33622A) generates the driving circuit signals. A DC electronic load (Itech IT8812B) acts as an active load for the circuit under test. Finally, a precision power analyzer (N4L PPA5530) measures efficiency, power factor, displacement factor, THD, and the magnitudes of input current harmonics.

TABLE I. PROPOSED CONVERTER BOM

Component	Value	Type
L_{IN}	100 μH / 0.5 A	Inductor
C_{IN}	2 * 15 nF / 450 V	Ceramic (C0G)
Diode Bridge	4 * ESH1GM RSG	Si Fast Recovery
C_{DC}	1 * 10 μF / 450 V	Electrolytic
	3 * 0.1 μF / 450 V	Ceramic (C0G)
D_P	RF201LAM4S	Si Fast Recovery
C_P	2 * 680 pF / 500 V	Ceramic (C0G)
Q_{HS}, Q_{LS}	GS66502B	GaN Switches
L_{RES}	152 μH / 1.7 A	Custom design
C_{RES}	220 pF / 3 kV	Ceramic (C0G)
D_{R1}, D_{R2}	GB01SLT06-214	SiC Schottky
C_{OUT}	2 * 15 nF / 450 V	Ceramic (C0G)

B. Results

The converter is tested for operation from 230 V_{RMS} , achieving 50 W of output power, with an efficiency of 84%, a power factor of 0.99 and a THD of 8.6 % at 0.96 MHz. Fig. 10 shows a scope capture for the switching node voltage, the resonant tank current, and the signals to the gate drivers at full-load operation. The capture is taken with infinite persistence to visualize the variations across the input voltage range, which is the low-frequency ripple on the DC capacitor voltage. The switching node voltage V_{SW} is measured using a 500 MHz 10x voltage probe with 9 pF capacitance, while the resonant circuit current I_{RES} is measured using a 50 MHz current probe (LeCroy AP015). The figure illustrates inductive mode of operation, with the resonant current lagging the switching node voltage. The driving signals are synchronized with the same duty-cycle and extended dead-time to avoid cross conduction between the two switches and achieve ZVS. It is noted that the converter is partially soft-switching for the low voltages across the DC capacitor, which can be alleviated by employing a larger energy storage capacitor (C_{DC}).

Fig. 11 shows the input voltage and current and the output voltage at full-load. The input voltage is displayed using a high voltage differential probe (Testec SI 9001), while the input current is measured using a 50 MHz current probe (Hioki CT6700), and the output voltage is measured using a 500 MHz voltage probe with 9 pF capacitance. The figure shows an almost sinusoidal input current with a phase difference of 5.7° with the input voltage, and an average output voltage of 300 V.

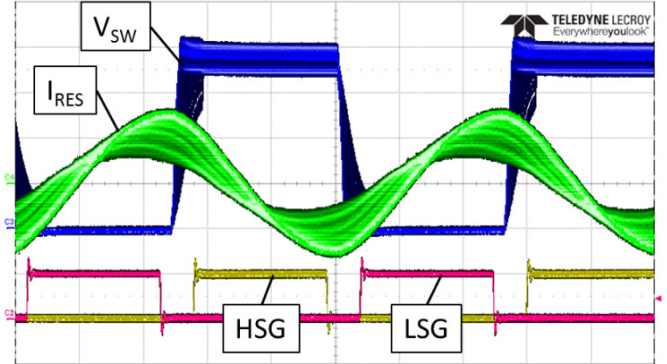


Fig. 10. Scope image for the resonant tank waveforms (V_{SW} 100 V/div, I_{RES} 1 A/div, HSG/LSG 5 V/div with 200 ns/div).

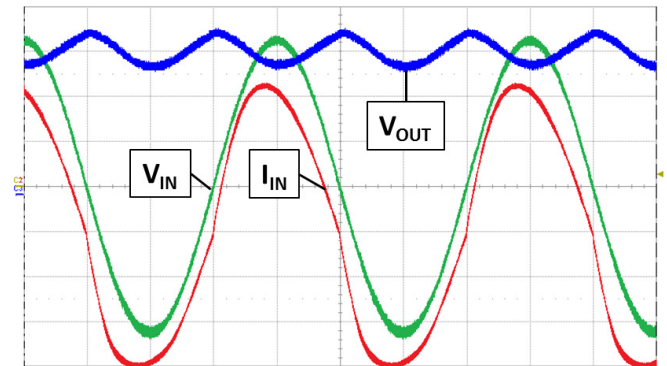


Fig. 11. Scope image for the input voltage, current, and output voltage. (V_{IN} 100 V/div, I_{IN} 100 mA/div, V_{OUT} 100 V/div with 5 ms/div).

An AC 100 Hz ripple of 40 V is measured on the output voltage, which is about 13.3 % of the average output voltage and can be reduced through the incorporation of a larger DC energy storage capacitor, depending on the specification of the following DC-DC converter stage.

Fig. 12 shows the input current harmonics distribution at full-load operation, where a THD of 8.6 % is measured. Since one of the potential applications for the proposed converter is the rectifier stage in LED drivers, the figure compares the harmonic magnitudes against the IEC 61000-3-2 standard class-C device limits [6][7], where it is shown that the measured harmonics magnitudes are substantially lower than the limits set by the standard.

Fig. 13 shows a thermal photograph for the prototype under full-load operation, where the inductor windings are the hottest element in the circuit, with a maximum temperature of 84.5 °C (with airflow). That is due to the charge pump circuit operation, which requires the resonant tank to store both the energy from the input line as well as the energy to the load every switching cycle, resulting in additional current stress on the resonant inductor.

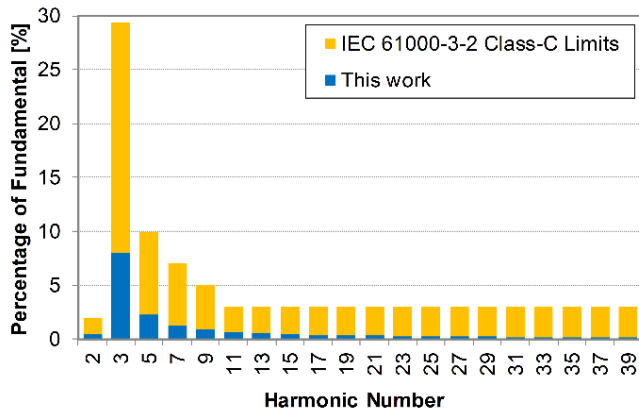


Fig. 12. Input current harmonics distribution against the IEC 61000-3-2 standard.

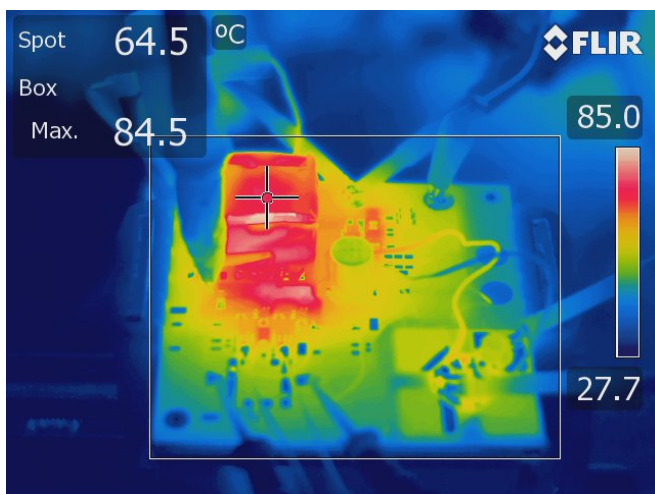


Fig. 13. Thermal image for converter at full-load.

V. CONCLUSION

A PFC rectifier for the AC-DC stage in single-phase offline converters is presented. With the addition of a charge-pump circuit comprised of a capacitor and a diode to the class-DE series-resonant converter, PFC functionality is achieved inherently, while operation is based on soft-switching, allowing for high frequency design. A 1 MHz 50 W prototype employing WBG devices is designed and implemented, achieving a power factor of 0.99 and THD of 8.6 % at an efficiency of 84 %, with input current harmonic magnitudes substantially lower than the IEC 61000-3-2 standard limit.

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