A Novel Error Rate Estimation Approach for UltraScale+ SRAM-based FPGAs

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***Abstract*—SRAM-based FPGA devices manufactured in FinFET technologies provide performances and characteristics suitable for avionics and aerospace applications. The estimation of error rate sensitivity to harsh environments is a major concern for enabling their usage on such application fields. In this paper, we propose a new estimation approach able to consider the radiation effects on the configuration memory and logic layer of FPGAs, providing a comprehensive Application Error Rate probability estimation. Experimental results provide a comparison between radiation test campaigns, which demonstrates the feasibility of the proposed solution.**

Keywords—SRAM-based FPGA, Soft-Error Rate, Single-Event Effect, Single-Event Upset, Single-Event Transient

I. INTRODUCTION

In the last decade, SRAM-based Field Programmable Gate Arrays (FPGAs) within space or avionics applications become increasingly attractive due to their reduced non-recurring engineering (NRE) costs, better performances with respect to general purpose processors, and reconfiguration capabilities. Nowadays, the novel FPGA generations, such as Xilinx UltraScale+ Family, are even more compelling, thanks to their higher density and enhanced performances.

Anyway, FPGA utilization in safety or mission critical applications is still limited due to the dependability issues related to radiation sensitivity. In fact, even if recent studies indicate that the new FinFET technology has a lower Single-Event Effect sensitivity than previous generation bulk processes [1]–[3], the technology scaling on the other side, increases the device density and consequently the probability that incident particles hit more nodes [4]. In fact, the continuous size shrinking of FPGA's transistors on one hand improves the device density, power consumption and performances and on the other hand, increases the sensitivity regarding radiation-induced errors such as Single-Event Upsets (SEUs) and Single-Event Transients (SETs). SEUs produced by high-energy particles hitting the sensitive silicon areas are one of the most probable transient faults, causing single transient bit flips in memory elements of the FPGA. SEUs in the configuration memory lead to modification in the programmable logic and routing resources, while SEUs in the application memory elements lead to modifications in the user variables and in the state of the system producing erroneous results and functionality [5].

Additionally, radiation particles crossing the device can deposit charge and create a voltage glitch in the circuit producing a SET pulse. If the induced SET pulse has a sufficient width and amplitude, it can propagate until the memory element and be sampled by memory elements, causing spurious effects in the application.

Consequently, it is fundamental to investigate and characterize the susceptibility of a device to these effects. Thus, in the last decades researchers put a lot of effort in estimating devices and applications sensibility with respect to SEUs and SETs [6]–[10].

Considering the new generation of UltraScale+ devices, due to the reduced technology size, higher sensibility is expected. However, since these devices have been released recently, not many studies have been dedicated to them.

Thus, in this paper we propose an analytical computation-based strategy, based on software tools to produce an estimation of the design susceptibility to radiation effects on Xilinx UltraScale+ devices. The main contribution of our approach is to provide an accurate SEU and SET estimation, massively reducing the amount of time required by fault-injection campaigns and the high cost involved in accelerated radiation tests.

To confirm the validity of our approach, we apply our framework to a benchmark design implemented on a Xilinx UltraScale+ XCZU3EG FPGA (16 nm FinFET technology), to estimate the application susceptibility to SEUs and SETs. Therefore, the results obtained with our approach have been compared with the one obtained with the accelerated radiation ground testing. The comparison confirmed that our error rate prediction and analysis is compliant with the results provided by radiation tests.

The rest of the paper is structured as follows: in Section II background of Single Event Upset and Single Event Transient has been elaborated. Our analysis method is presented and discussed in Section III, while experimental results and conclusions and future activities are described in Section IV and V.

II. BACKGROUND

Xilinx's new UltraScale+ FPGAs are 16nm FinFET based technologies providing more density and scalability to the device. Furthermore, Xilinx implemented a variety of features in their UltraScale architecture, in order to face the main bottlenecks of their last generation of 7 series FPGAs. In UltraScale devices the data flow and routing are improved

with the implementation of “Fast Tracks”. In comparison to family 7 devices the basic tile has a different architecture, as shown in Fig. 1 and processing and bandwidth capabilities are improved. Furthermore, other new features, such as ASIC-like clocking ASIC-like Clocking, Power Management, Multi-level Security, Reconfiguration and Co-optimization, are implemented [11].

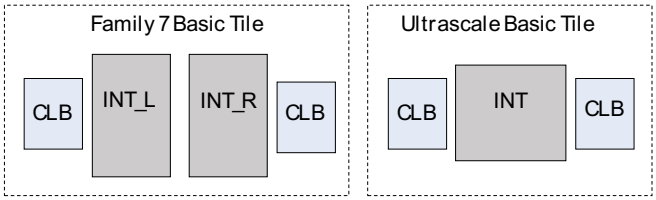

Fig. 1. Comparison between the Family 7 Basic Tile and UltraScale Basic Tile.

In most cases, when radiation strikes through the FPGA silicon, Single-Event Effects (SEEs) occur (Fig. 2). When the particle hit a sensitive node in a semi-conductor device, the ionization by the particle might produce a current pulse, which can cause permanent or transient errors in logic or in memory elements. While in the past this concern was more significant in radiation harsh environments, such as the space environment, recent technologies may suffer from SEEs even in terrestrial applications [4]. For instance, SEEs may occur even at high altitude in avionic applications, close to nuclear reactors or just due to the natural decay radiation in the device material itself.

SEEs may cause both transient faults and permanent faults depending on the amount of energy transferred by the charges particles. Transient faults cause no permanent damage and can be recovered by reconfiguring the device and according to Xilinx Radiation Reports are the most common [12]. Thus, in this section the focus is mainly on them, and above all on SEU and SET. As mentioned, SEUs are critical in electronic devices since they interact with the memory elements by changing their logic state

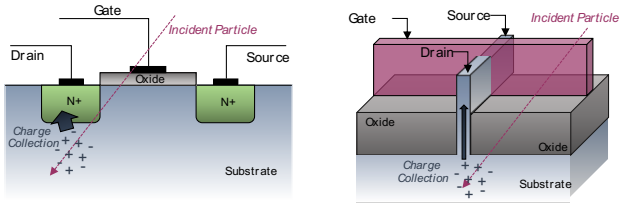

Fig. 2. Comparison between the Family 7 Basic Tile and UltraScale Basic Tile.

In FPGAs, their impact is even more dramatic since the functionality of a given application is determined by the bit values stored in the configuration memory. Thus, the effects of SEUs may drastically change the operative functionality of the FPGA causing unexpected behaviors. For instance, SEUs may alter the content of Look-Up Tables (LUTs) in Configurable Logic Blocks (CLBs), or the routing configuration inside switch matrices.

Besides the configuration memory, SEUs can also affect the user memory, and registers inside the embedded cores. SEUs in the user memory, both internal block memories (BRAMs) and user programable flip-flops, can change the variables and state of the system, while SEUs in the embedded hard IP cores, which typically contain registers, could cause changes in their operation and behavior. The error produced by SEUs in an FPGA can be quite complex and their effects often are not observable until they show themselves in the output throughout the system. Further, programmed circuits can logically mask some of these faults [8], [13].

SETs instead create a voltage glitch in the circuit known as transient faults, which last for a short period of time (ranging between picoseconds and nanoseconds) depending on the pulse width and amplitude. The shape of this glitch is related to specific type of particle hitting the device and to the device technology. In fact, the SET shape depends on the Linear Energy Transfer (LET) of the particle, on the impact angle, on the materials itself and the electric fields present at the impact moment. SET pulses become critical when they are propagating through the logic and routing of the circuit and eventually sampled by a memory element, thus corrupting the data stored inside and producing errors that may lead to application malfunctioning. SET effects in SRAM-based FPGA have not been studied in depth but recently, scientific researchers have acknowledged SET effects as a forthcoming issue for two main reasons. First, technology node scaling and increasing working frequency. In fact, the technology shrinking and the consequently increase of the density of the interconnect fabric result in increased nodes capacitance. This increases the probability of SET pulses due to low energy particles which are wide enough to be propagate and sampled. Furthermore, the probability of a SET glitch to be sampled by flip-flops increases proportionally with the working frequency of the circuit [9], [10].

To analyze the effects of SEUs and SETs in FPGAs three main approaches are possible: accelerated radiation ground testing, fault-injection and analytical computation.

In the first one, the physical device implementation of the application under test is exposed to a radiation beam, originated by particle accelerators or radioactive sources. Such radiation tests represent an accurate and effective solution to correctly estimate the sensitivity of a device to radiation effects. On the other side, this approach implies a huge cost related to several aspects. First of all, in some cases the device under test can be permanently damaged by the radiation beams. Furthermore, the cost, both in terms of money and time, related to the experimental setup and required facility are prohibitive. Additionally, the technology shrinking make every day more difficult to manage enough precision to produce single effects.

The fault-injection alternative is a valid solution to evaluate device sensitivity. It consists in injecting different kinds of faults with different kinds of technique to simulate radiation effects and to observe how the system behaves. First of all, with this technique, devices do not need to be irradiated and so it is almost impossible to damage them permanently. Furthermore, this approach most of the times, provide higher controllability to where the effect is simulated with respect to physical radiation tests allowing to better characterize resources sensitivity. Unfortunately, fault injection campaigns, especially the exhaustive ones, require an amount of time which is still to huge [14].

For all these reasons, the analytical computation-based technique is an optimal alternative to lower the execution time required for fault injection and to avoid the high costs related to of radiation test. It is based on synthesis tools and

software programs, which are already integrated or can run in cooperation with FPGA vendor's development tools.

III. Proposed Analysis Method

The aim of this work is to propose an effective methodology to estimate Error Rate of the implemented circuit due to Single-Event Upsets and Single-Event Transients. In order to due this, we developed two engines which provide the estimation of Error Rate due to SEU and SET.

A. SEU Estimation

The VERIPlace Tool is a software tool developed in house by Politecnico di Torino, which is capable of 1) performing design application error rate prediction for SRAM-based FPGA w.r.t. SEUs in the configuration memory induced by radiation effects; 2) improving design reliability without introducing hardware resource overhead. It has been used in previous radiation test for error rate prediction and the effectiveness of its hardening strategy has also been verified [17].

The application error rate is calculated as the probability of application generating an error at the output w.r.t. certain number of SEU accumulated in the configuration memory. For the purpose of this work we modified the VERIPlace algorithm in order to include the estimation of the SET probability and the correlation with the radiation particle energy used during the radiation campaigns.

B. SET Estimation

In space, several kinds of radiation particles can interact with electronic devices, deposit charge and creates a voltage glitch in the circuit known as Single Event Transient (SET). The characteristics of the generated SET pulse is a function of the energy of the particle, incident angle and the material encountered. The generated pulse can be critical if the generated pulse propagates through the circuit and reach to the storage element and be sampled by the storage element. Therefore, it creates an error in the overall functionality of the circuit.

There are several methodologies to mitigate the generated SET and following SEU. One of the most used techniques is Triple Modular Redundancy (TMR). Considering Fig. 3 as a typical case of TMR in which the logic and the voters have been triplicated, if the particles interact with device at point (A), it may generate SET pulse at this point. The generated SET will propagate through the routing segment and reach each single voter. In ideal condition, the generated pulse affects one out of three signals reaching to the voter. Supposing that the other two signals reaching to the voter are not suffering from the SET fault, the voter is filtering SET pulse and vote for the majority fault free signal. However, in real case, the SET pulse is affecting the output of the voter. To elaborate more, each FFs is connected to the voter though different routing segments. Therefore, signals from FFs will reach to the voter with a specific delay which is equal due to the difference between the delay of used routing segments. This difference between delays is opening a time window in which the voter is sensitive to SET pulses.

Considering SET pulses generated at point (A) and propagated through path 1 to voter (1). As showed in Figure 3 (b), the difference between the delay of path 1,2 and 3 is opening a time window in which the SET pulse is captured by the voter and creates a voltage glitch at the output of the voter. This pulse is going to be captured by the FF and propagate to the next stage TMR module.

Considering that the mentioned time window happening due to difference of routing delay also exists in the following TMR module, the propagated pulse is going to be captures by the next stage voter and propagate until the output of the implemented design.

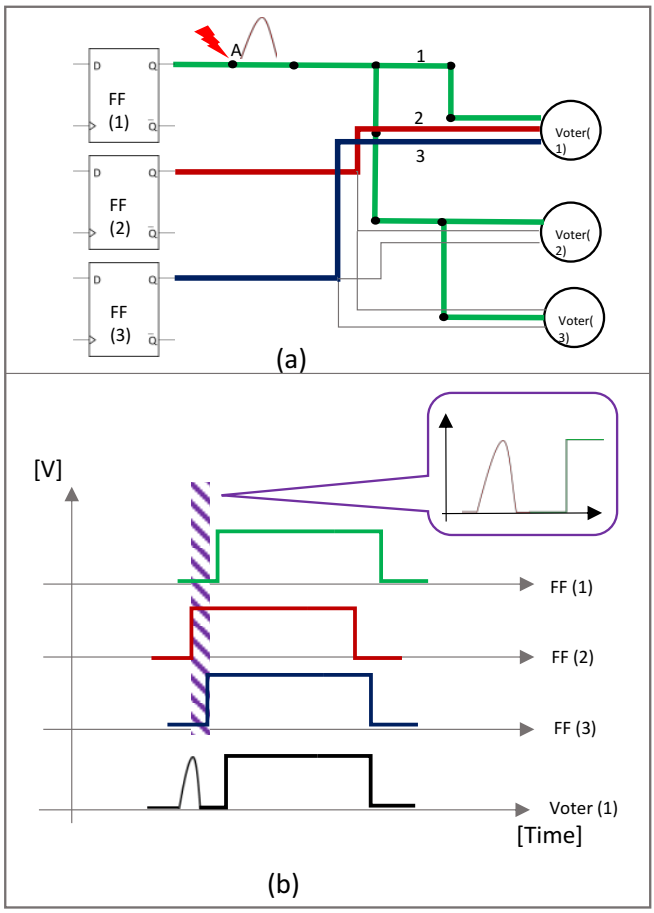

Fig. 3. Applied TMR methodology to a Single FF.

In order to analyze the sensitivity of the implemented circuit regarding the scenario of SET on TMR, we developed an engine which takes into account the netlist of the circuit, as illustrated in Figure 4. To elaborate more, the developed tool starts with the typical design tool chain. A commercial tool is used to generate synthesized netlist from the Hardware Description, HDL source file of the implemented circuit, going through mapping and place and route.

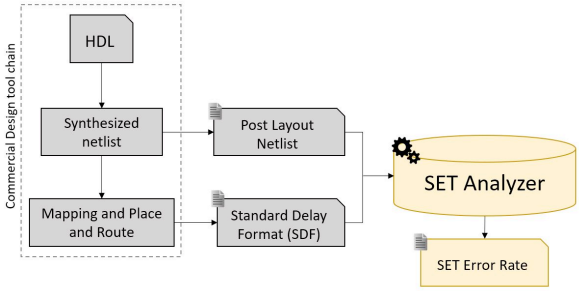

Fig. 4. Overall view of the developed flow for analyzing SET phenomena.

From the typical design tool chain, the SET analyzer algorithm starts by loading the circuit Verilog netlist and

standard delay format (SDF) of the implemented. After *Initialization Phase*, the algorithm starts with each single node of the netlist and extract all the FFs of the implemented design which has been triplicated. As a next phase, starting from each single extracted node, the algorithm extracts all the paths connecting the node to the output of the circuits and classifies the propagated path based on the module of the TMR they belong to. To elaborate more, for each three paths dedicated to one single TMR module, the algorithm dedicates the *module_ID* to the paths. The algorithm continues with connecting netlist of the design to the timing information reported in SDF file. It means that starting from the extracted path, the algorithms calculates the delay regarding each path based on used segments in the routing for the same *module_ID* and creates the database including TMR nodes with their delay information.

The last phase of the algorithm is dedicated to evaluate the sensitivity of the implemented design regarding SET phenomena in TMR. Therefore, this phase takes into account the source SET duration which has been defined by the user, the frequency of the implemented design and the databased generated by the tool in terms of the extracted paths. Based on this data, the algorithm calculates if the considered SET at the extracted node generates the error in the outputs or not. In a case of error in the output, the TMR node is reported as to be used for future mitigation solution. Fig. 5 is dedicated to the pseudo-code of the explained algorithm.

```
// Initialization Phase
    Netlist_orig= Verilog_load();
    Timing_orig= SDF_load();
    TMR_node= {0};
    extracted_path= {0,0,0};
    SET_Pulse= SET_Source_load();
    Frequency_orig= Frequency_load();
// TMR Extraction Phase
    ∀ Node n ∈ Netlist_orig
    if n is a TMR_module_component ⟶ TMR_node= n
// Propagation Phase
    module_ID=0
    ∀ Node m ∈ TMR_node
    extracted_path{path_from_node_m, module_ID};
    Module_ID++;
// Timing Phase
    ∀ Node n ∈ extracted_path
    delta_delay= SDF_load (n+1,n);
    extracted_path= {:,:,delta_delay};
// Sensitivity Evaluation
    ∀ path j ∈ extracted_path
    while (SET_Pulse, Frequency_orig)
    {
        if SET_Pulse is error
        report TMR_node
    }
```

Fig. 5. The pseudo-code for evaluating the sensitivity of the implemented design regarding SET

IV. Experimental Results

In order to evaluate the proposed method a radiation test campaign on a Xilinx UltraScale+ device has been performed. The device was tested under heavy ions. This section describes the test setup, the considered test circuit and eventually, presents the results of the radiation test. The results are used to compare the estimated error rates with the, in the previous sections proposed approach.

A. Characteristics of the Device Under Test

The Xilinx UltraScale+ devices are available in different device families. For the radiation test campaign, a device from the Zynq family was used. This device embeds a high-performance processing system (PS), based on ARM processors, and the latest generation of FPGA architecture. Within the Zynq family there are different devices available which differ in the embedded PS (number of CPU cores, maximum operating frequency, availability of a video codec IP, etc.) and the FPGA resources (number of logic slices, size and type of user memory, I/O pin count).

For the radiation test the XCZU3EGSFVA625-1-E was selected. This device embeds a Processing System with 4 ARM A53 APU cores and 2 ARM R5 RPU cores. The main characteristics and number of programmable logic resources are summarized in Table I.

TABLE I. XCZU3EG-SFVA625-1-E DEVICE CHARACTERISTICS

Resource	ZU3EG
	Processing System
APU	4 x ARM Cortex A53 - 1.5 GHz
RPU	2 x ARM Cortex R5 - 0.6 GHz
GPU	ARM MALI-400 MP2
On-Chip Memory	256 KB, ECC Protected
	Programmable Logc (FPGA)
System Logic Cells	154,000
CLB Flip-Flops	141,000
CLB LUTs	71,000
Distributed RAM	1.8 Mbit
Total Block RAM	7.6 Mbit

B. Test Board, Test Setup and Test Approach

A custom test board, shown in Fig. 6, has been designed to fulfill the requirements of the radiation test. The test board is able to monitor the device current and implements a reset management circuit which is used to reboot the device under test in the case of a fatal error (e.g. Single Event Latch-ups or uncorrectable FPGA Configuration RAM error). A QSPI flash memory is used to store the software running on the PS and the configuration bitstream of the FPGA.

During the radiation experiments, an external tester is used to monitor and check the status of the device. This tester communicates with a PC in order to log and report errors. Further, some radiation tests require that the device is in a vacuum chamber of the facility. Fig. 7 illustrates the test setup with the DUT test board and the external tester inside of the vacuum chamber.

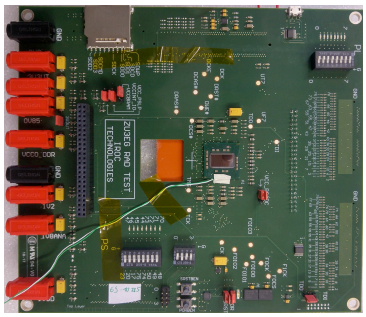

Fig. 6. Radiation Test Board designed for the XCZU3EG Device, with one de-lided device.

The FPGA Configuration RAM (CRAM) defines the behavior of the configurable logic of the FPGA. Since the DUT is an SRAM based FPGA, the CRAM needs to be loaded every time after the power-up. Under irradiation, upsets in this memory may alter the logical behavior of the implemented circuit and can induce short or open circuits in the interconnection fabric. In order to mitigate this effect, Xilinx provides the Soft-Error-Mitigation IP (SEM-IP) which continuously scrubs the CRAM during the device operation. It uses error detection and correction codes (ECC and CRC) to detect and correct errors in the CRAM.

Additionally, the SEM-IP provides an interface to report CRAM errors to the user.

The Configuration Memory is organized as an array of frames, whereas each frame is protected by ECC and the entire array of frames is protected by CRC. The CRC is mainly used for the error detection, while ECC is used for error location. When the error detection circuits signal an error, the SEM controller evaluates the situation and attempts to correct it. The ECC syndrome is used to identify the exact location of the error in a frame. If the location can be identified, the SEM controller corrects the soft error, by using active partial reconfiguration (read the frame, invert the relevant bit and write the frame back) and signals it as a correctable error. For errors which cannot be located, due to multiple bit errors, the controller signals that an uncorrectable error has occurred (Detectable Uncorrectable Error, DUE) [15].

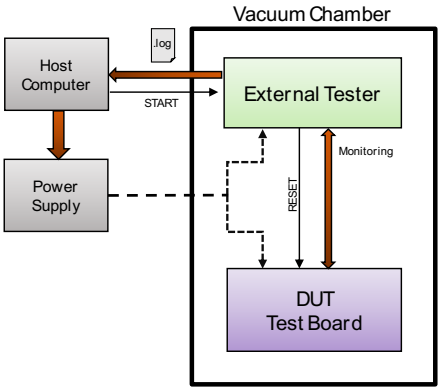

Fig. 7. Test setup with external tester in vacuum chamber.

During the radiation tests, the SEM-IP's reporting interface is used to count errors occurring in the CRAM. Therefore, the status interface and corresponding UART interface is used, which indicates a correct operation and further, provides additional details about the CRAM errors, such as frame address and erroneous bits. In case a CRAM SEU alters the behavior of the SEM-IP itself or a multi-bit Upset occurs which cannot be corrected, the IP changes into the fatal error state and the external tester will be notified. This triggers the tester to read-back the entire CRAM and resets the device.

The continuous scrubbing by using the SEM-IP has some advantages in comparison to static tests where the configuration memory is readback regularly [5]. First, it is more representative of the real usage of an SRAM based FPGA. Second, a correct behavior of the implemented circuit is maintained during the irradiation.

C. Test Circuit

The implemented test circuit considered during the radiation test consists of two parallel flip-flop chains. The first chain implements a plain shift register chain and connects the output of one flip-flop directly to the input of the following one [16], bypassing the slice look-up tables (see FF Chain in Fig. 8). The second flip-flop chain uses Triple Modular Redundancy. The TMR is implemented using three independent voting circuits at each stage of the shift register, feeding into the three redundant flip-flops of the next stage [16], as shown in Fig. 8 (TMR Chain).

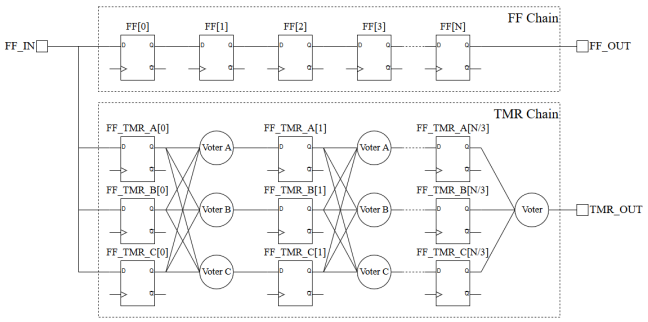

Fig. 8. Implemented Test Circuit: Standard Flip-Flop Chain and TMR Flip-Flop Chain

Each voter is implemented using one look-up table of the device. To avoid MCU effects the three redundant flip-flops and LUTs of each stage are manually placed in three different logic slices of the device. Both chains using the same input source and the separated output is monitored by the external tester. The circuit operates at a frequency of 20 Mhz. In order to use nearly all the resources of the DUT the standard flip-flop chain has a length of 49920 and the length of the TMR chain is a third of this size. The number of resources used by the test circuit is listed in Table II.

TABLE II. CIRCUIT RESOURCES UTILIZATION

	CLB Register	***CLB LUTs***
FF Chain	49,920	0
TMR Chain	49,923	49,922
SEM-IP	474	364
Temperature Report	44	32
RAM Test	40	15,699

D. Test Results

During the radiation test the SEM-IP was running at 200 MHz and checking 29,192,364 bits of the CRAM with a scrubbing cycle of 9 ms. The average SEU in the CRAM per scrub cycle is shown for the different LETs and the used average flux in Table III. Additionally, the average number of Detectable Uncorrectable Errors (DUE) per scrub cycle are listed which are about two to three orders of magnitude lower than the detectable and correctable errors.

The two flip-flop chains were tested with a dynamic pattern of "11001100". While monitoring the output of the two flip-flip chains, two types of events were observed during the radiation test. The first type of event is a single bit flip in the pattern at the output, which is caused by an SEU in one of the flip-flops. The second type of event is a continuous error at the output (burst) due to logical inversion of the pattern or a stuck at 0/1 at the output. The second type of events are probably mainly caused by an SEU in the CRAM, which alters the logic behavior or more probably the configuration memory bits controlling the FPGA interconnects. These two events were counted separately and the second events were not considered for calculating the SEU cross-section. In Table VI the SEU cross-section per bit is shown for the CRAM, the plain flip-flop chain and the TMR flip-flop chain. As it can be seen, the SEU cross-section for the CRAM and the FF Chain are mainly in the same order of magnitude, whereas no SEUs were observed for the TMR Chain.

TABLE III. SEU AND NOT CORRECTABLE ERRORS IN THE CRAM

Ion	*LET [Mev.cm2/mg]*	*Average Flux [hi/s/cm2]*	*CRAM SEU*	*CRAM DUE*
C	1.54	1.52×10^{4}	8.85×10^{-4}	0
Ne	4	8.83×10^{3}	9.58×10^{-2}	1.37×10^{-4}
Al	7.86	2.04×10^{3}	6.14×10^{-2}	6.78×10^{-5}
Ar	12.8	5.12×10^{2}	3.00×10^{-2}	9.07×10^{-5}
Xe	17.2	5.26×10^{2}	1.85×10^{-2}	2.10×10^{-5}
Ni	30.4	1.81×10^{2}	2.57×10^{-2}	4.69×10^{-5}

TABLE IV. SEU CROSS-SECTION OF THE CRAM, THE PLAIN FLIP-FLOP CHAIN AND THE TMR FLIP-FLOP CHAIN

Ion	*LET [Mev.cm2/mg]*	*XS CRAM SEU*	*XS FF Chain*	*XS TMR Chain*
C	1.54	2.21×10^{-13}	0	0
Ne	4	4.14×10^{-11}	2.10×10^{-12}	0
Al	7.86	1.14×10^{-10}	2.83×10^{-10}	0
Ar	12.8	2.23×10^{-10}	8.87×10^{-10}	0
Xe	17.2	2.84×10^{-10}	8.49×10^{-10}	0
Ni	30.4	5.52×10^{-10}	1.67×10^{-09}	0

The two observed and discussed types of events, the SEU and burst, are considered in Table V. The table lists the average number of event per CRAM Event (SEU and DUE). While for the plain FF Chain both effects were observed, the TMR Chain shows only burst events, due to the masking effect. Further, due to the masking, the observed burst events are about one magnitude lower for the TMR Chain.

TABLE V. AVAREGE NUMBER OF EVENTS PER CRAM EVENT

Ion	*LET*	*FF Chain*		*TMR Chain*	
		SEU	*Burst*	*SEU*	*BURST*
C	1.54	0	0	0	0
Ne	4	8.66×10^{-5}	2.73×10^{-3}	0	8.66×10^{-5}
Al	7.86	4.23×10^{-3}	1.84×10^{-3}	0	0
Ar	12.8	6.78×10^{-3}	3.51×10^{-3}	0	2.51×10^{-4}
Xe	17.2	5.10×10^{-3}	4.34×10^{-3}	0	1.89×10^{-4}
Ni	30.4	5.16×10^{-3}	5.47×10^{-3}	0	6.08×10^{-4}

E. Error Rate Prediction and Comparison

In order to evaluate the possibility to predict the application error rate (AEP), that means when the implemented circuit on the FPGA will have at least one erroneous data output, we performed the analysis of the implemented circuit using the VERIPlace tool. The results provided by the tool are illustrated in Fig. 9. Please note that since the circuit under test has been designed without effectively applying a TMR approach, we compute the AEP without considering any mitigation techniques applied to the mapped circuit.

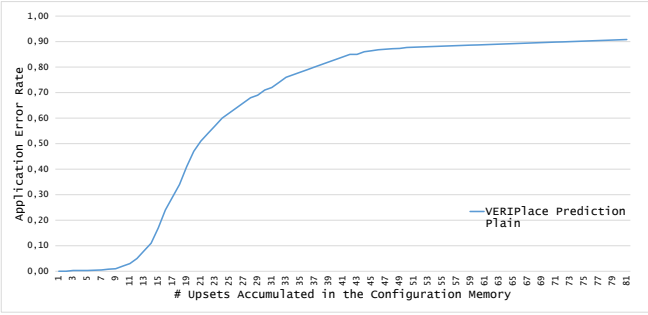

Fig. 9. Application Error Rate plot provided by the VERI-Place tool.

In order to make a feasible comparison we needed to modify the calculation of both the experimental and the VERIPlace tool analyses. In details, we extract from the radiation test data the number of scrub cycles and the relative CRAM events provoking an error on the output of the FF Chains, these events were classified during the radiation experiments as burst errors. Besides, we cumulate the number of configuration memory bit upsets events observed for each scrub cycle and we divided them by the total number of scrub cycles per run. Thanks to this calculation, it is possible to obtain the application error rate of the circuit induced by different number of SEU events on the CRAM, as illustrated in Table VI. Please note that we excluded the C ion from the computation since no burst events were observed during the radiation experiments.

TABLE VI. APPLICATION ERROR RATE PROBABILITY PER SCRUB CYCLE FROM RADIATION EXPERIMENTS

Ion	*LET [Mev.cm2/mg]*	*1 SEU AEP*	*2 SEUs AEP*	*3 SEUs AEP*	*4 SEUs AEP*
Ne	4	3.17×10^{-6}	2.9×10^{-7}	4.35×10^{-7}	2.9×10^{-7}
Al	7.86	1.50×10^{-4}	0	0	0
Ar	12.8	5.98×10^{-4}	1.51×10^{-4}	0	0
Xe	17.2	3.09×10^{-5}	0	0	0
Ni	30.4	1.54×10^{-4}	1.17×10^{-2}	0	0

On the other hand, the VERIPlace tool Application Error Rate probability method has been modified the CRAM cross-section per Ion coefficient, this allows to consider the different LET per experiment also during the analytical evaluation. The obtained results are described in Table VII, while a comparison between the AEP induced by only one SEU from the radiation experiments and the VERIPlace tool is illustrated in Figure 10. As it is possible to notice the two results are strictly similar. On the other hand, due to the lack of experimental data, we do not have the possibility to provide reliable results for the AEP induced by two or more SEUs.

TABLE VII. APPLICATION ERROR RATE PROBABILITY PER SCRUB CYCLE FROM VERIPLACE ANALYSIS

Ion	*LET [Mev.cm2/mg]*	*1 SEU AEP*	*2 SEUs AEP*	*3 SEUs AEP*	*4 SEUs AEP*
Ne	4	3.24×10^{-6}	5.42×10^{-6}	6.56×10^{-6}	7.43×10^{-6}
Al	7.86	2.02×10^{-4}	6.92×10^{-4}	1.26×10^{-3}	2.45×10^{-3}
Ar	12.8	7.03×10^{-4}	1.09×10^{-3}	5.85×10^{-3}	9.94×10^{-3}
Xe	17.2	3.21×10^{-5}	5.65×10^{-5}	2.43×10^{-4}	6.52×10^{-4}
Ni	30.4	1.68×10^{-4}	1.23×10^{-2}	6.45×10^{-2}	1.04×10^{-1}

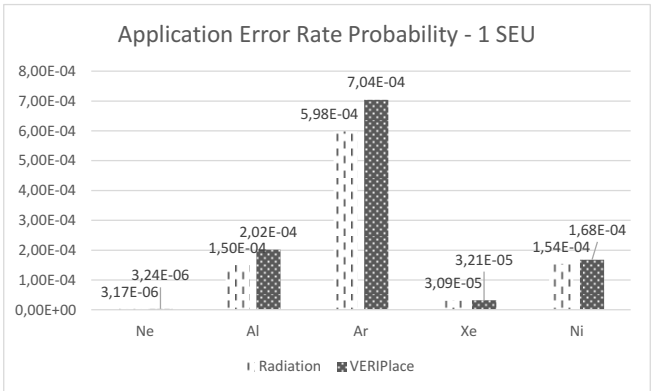

Fig. 10. A comparison of the Application Error Rate probability calculated from Radiation Experiments data and the VERI-Place tool.

V. Conclusions and Future Works

In this paper, a new method to estimate the error rate probability of circuits on SRAM-based FPGAs is proposed. A preliminary radiation test campaign analysis on a simple benchmark circuit has been used as fundamental results with respect to the analytical analysis algorithm VERIPlace. The key concept of the tool is to predict the error rate on the circuit output due to radiation particle strikes on the FPGA configuration memory and user logic. The preliminary analysis performed; demonstrate a realistic value for single SEUs into the FPGA configuration memory while more accurate and extended radiation experiments are necessary to evaluate the calculation with more upsets. On the other hand, the VERIPlace tool requires an extension of the configuration memory analysis for the modern generation of SRAM-based FPGAs in order to improve the calculation due to different technology layers.

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