Single-Event Characterization of Xilinx UltraScale+® MPSOC under Standard and Ultra-High Energy Heavy-Ion Irradiation

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***Abstract*—Heavy-Ion irradiation of a Xilinx Ultrascale+ MPSOC was performed to measure Single-Event-Latch-up and Single-Event-Upset Cross-Sections. Additionally, irradiation with a ultra high energy xenon beam shows similar upset sensitivity.**

***Index Terms*—Single-Event-Effect, Radiation Testing, FPGA, Single-Event-Upset, Single-Event-Latchup**

I. Introduction

As technology scales, configurable devices such as Xilinx FPGAs and MPSOCs can be configured to implement increasingly complex applications. Additionally, new technologies, such as FDSOI and FinFETs, shows much lower single event effect sensitivity, than older bulk processes. Given their resiliency and their affordable cost, new generation FPGAs compare very favorably to Application Specific Integrated Circuits (ASICs).

II. Test Description

A. Device Under Test Characteristics

The Xilinx Ultrascale+ devices are available in different device families. The Zynq®familiy embeds a high performance processing system (PS), based on ARM®processors, and a lastest generation FPGA, based on the Xilinx Ultrascale architecture. Many configurations of Zynq devices are available, with differences in the PS (number of CPU cores, maximum operating frequency, presence of a video codec IP, ...) and the FPGA (number of logic slices, size and type of user memory, I/O pin count). The part selected for this test is the XCZU3EG-SFVA625-1-E. This component is a small device of the EG category of the Zynq family, meaning that its PS embeds 4 ARM A53 APU cores and 2 ARM R5 RPU cores. However, the size of the FPGA is relatively small and advanced features suck as high-speed transceivers, DRAM memory controller and UltraRAM are not available. It is a flip-chip device, whose main core voltage is 0.85 V and its auxiliary voltage is 1.8V. Table I lists the main characteristics of the tested device.

The device under test was prepared for the heavy-ion irradiation by removing the lid and thinning the die to approximately 70 µm by mechanical milling.

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TABLE I
Main Characteristics of the XCZU3EG-SFVA625-1-E Device

Feature	ZU3EG
Processing System	
APU	4x ARM CORTEX^{TM} A53 - 1.5 GHz
RPU	2x ARM CORTEX^{TM} R5 - 0.6 GHz
GPU	ARM MALI^{TM}-400 MP2
On-Chip Memory	256 KB, ECC Protected
Programmable Logic (FPGA)	
System Logic Cells	154,000
CLB Flip-Flops	141,000
CLB LUTs	71,000
Maximum Distributed RAM	1.8 Mbit
Total Block RAM	7.6 Mbit

B. Radiation Test Board

A custom test board, shown in figure 1, has been designed to fulfill the requirements of the radiation testing. On this board, the current consumption on each of the 19 power domains of the ZU3EG device was monitored independently, using shunt resistors. This independent current measurement allows the detection of any sudden current increase, which is the typical signature of Single-Event-Latchup Events.

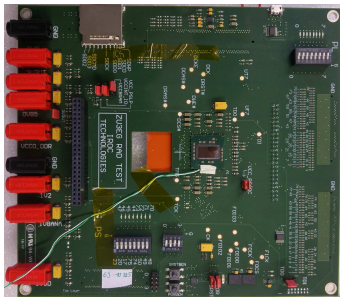

Fig. 1. Radiation Test Board designed for the XCZU3EG Device, with one de-lided device.

Additionally, the test board implements a reset management circuit which is used to reboot the device under test in the case of a fatal error (uncorrectable FPGA CRAM error, CPU crashes). It also embeds two QSPI flash memories, used to store the software running on the PS and the configuration bitstream of the FPGA. Finally, a UART-to-USB chip is used on the board to monitor and log the standard output of the PS during the radiation tests.

C. Implemented Design for Radiation Testing

The main objective of the radiation test campaign was to measure the SEL and SEU cross-section of the FPGA features (configuration and block memory, programmable logic).

In order to measure SEL cross-sections in worst case conditions, all the I/Os were operating at the highest voltage I/O standard for each type of bank (1.8 V for HPIO and 3.3 V for HDIO). Additionally, the voltage was increased to the part's maximum limit for each supply rails for SEL test conditions. SEL detection was based on the current measurements performed on each of the power domains of the ZU3EG device. Current and Voltage sampling was performed 10 times per seconds during the heavy-ion irradiations.

The goal of the SEU testing was to measure the SEU cross-section of the configuration RAM (CRAM), the Block RAM (BRAM), the Distributed RAM (DistRAM) and the user flip-flops during irradiation of the ZU3EG device. Device scrubbing, using the Xilinx SEM-IP solution, was enabled during the radiation testing to report and correct SEUs occurring in the CRAM of the device under test. This approach has several advantages compared to static irradiation during which the configuration is readback regularly [1]: First, it avoids the accumulation of interval voltage contentions, due to configuration errors, leading to a constant increase of the power consumption of the core power domain. Second, it is more representative of the real usage of an SRAM based FPGA in space applications. Third, it maintains a correct behavior of the device during the irradiation, allowing to measure SEU cross-section of user logical cells and memories. Finally, the correct operation of the Xilinx scrubbing solution and its capability to maintain the expected logical behavior of the device can be validated during radiation testing.

The BRAM, DistRAM and flip-flops were tested concurrently with to the CRAM, because the logic portion of the FPGA was sufficiently stable due to the scrubbing performed by the SEM-IP. Most of BRAM and DistRAM cells of the device were aggregated in two large memory arrays. These two arrays were tested by an external tester, using a dynamic test algorithm and standard patterns (ALL1, ALL0 and Checkerboard). The FPGA flip-flops were tested using two shift registers. The first one connects the output of one flip-flop directly to the input of the following one, by bypassing the slice look-up table. The second register can be configured either as a standard shift register or a TMR shift register, with its depth divided by three. The selection between both modes and the voting logic are implemented using one look-up table of the device. The TMR is implemented using three independent voting circuits at each stage of the shift register, feeding into the three redundant flip-flops, to maximize its robustness, as reported in [2]. Note that the three redundant logic cells of each stage were manually placed in three different logic slices of the device to avoid MCU effects. SEU cross-sections of both shift registers were measured using a dynamic test algorithm and standard logical patterns during the heavy-ion irradiations. The memory and flip-flop shifter test algorithms were designed to detect and filter burst events induced by upset occurring in the configuration RAM.

TABLE II
HEAVY-ION USED AT UCL FOR THE TEST OF ZU3EG DEVICE

Ion	Energy (MeV)	Range (μm)	LET_{SURF} (MeV.cm^2/mg)	LET_{EFF} (MeV.cm^2/mg)
C	131	269.3	1.3	1.5
Ne	238	202	3.3	4
Al	250	131.2	5.7	7.9
Ar	379	120.5	10.0	12.8
Ni	582	100.5	20.4	30.4
Xe	995	73.1	62.5	17.2

During the radiation test, an FPGA based tester was used to report and log the errors. Currents and voltages of the 19 power domains were measured and logged 10 times per seconds. SEL events was detected by the successive observation of three current samples with a value higher than a predefined threshold. In this case, the tester triggered a power cycle which lasted approximately one second. An effective heavy-ion fluence, considering the dead-times (power cycles, reset, time between successive memory read and write operations...), was calculated for each type of events and used to compute the associated cross-sections.

D. Heavy-Ion Test Facilities

1) Standard Heavy-Ions - UCL: Main heavy-ion tests were performed at UCL Heavy-Ion Irradiation Facility, at Louvain-La-Neuve, Belgium. UCL uses a cyclotron capable of accelerating heavy-ions up to an energy of $110\ Q^2/M$. Table II lists the heavy-ions used at UCL for radiation testing of the ZU3EG device, and their characteristics. For each ion, an effective LET was computed using SRIM to consider the ion energy change across the 70 um silicon substrates. Note that the range of the Xe ion is closed to the thickness of the device under test, leading to an effective LET lower than the one of the Ni ion. Additionally, some non-negligible strangling effects induce some variability of the effective LET. Due to these measurement uncertainties, the cross-sections measured with the Xe ion were not taken into account while computing the Weibull fits.

2) Ultra-High-Energy Heavy-Ions - CERN: Additionally to the standard heavy-ion tests, the ZU3EG device have been irradiated with 30 GeV/n xenon beam, at CERN, in the H8 SPS North Area beam line. The xenon beam was directly extracted from the Super Proton Synchrotron (SPS). Ions accelerated in the SPS can be extracted to the North Experimental Area (NA) with an energy range of 13-150 GeV/n. The beam is delivered as a series of spills with a duration of 4.5 to 10 seconds, depending on the configuration of the accelerator. The periodicity of the spills varied between 30 to 50 seconds during the test. The delivery of the beam in spills will generate additional complexity (when compared to constant beam experiments) during the result analysis phase, as we need to compute an effective fluence and dead time by carefully monitoring the beam flux. Particularly, the test setup should be able to handle and correctly discriminate from a temporal perspective the high number of errors that are induced during a fast spill event.

The beam intensity was measured using a scintillator, located approximately 50 meters behind the device under test.

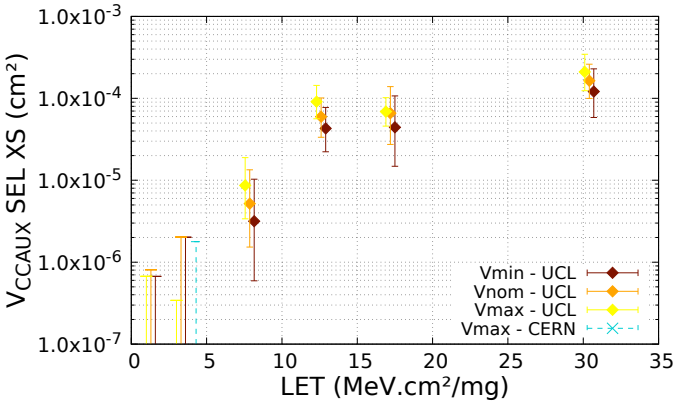

Fig. 2. V_{CCAUX} Power Domain Single-Event-Latchup Cross-Section of XCZU3EG Device (Weibull fit: XS_{SAT}=2.1e-4cm^2; LET_{TH}=6.11$MeV \cdot cm^2/mg$; W=9.0; S=1.9)

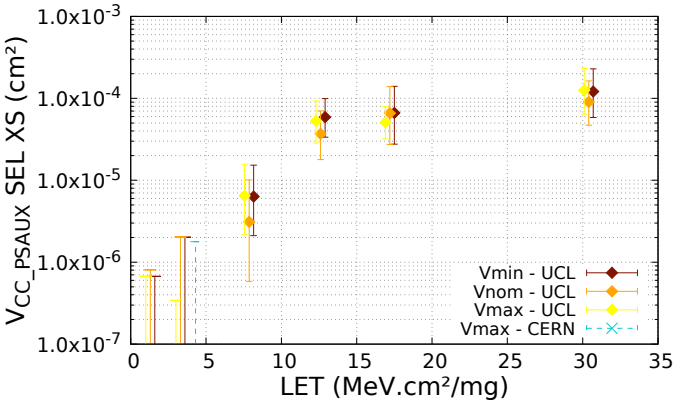

Fig. 3. V_{CC_PSAUX} Power Domain Single-Event-Latchup Cross-Section of XCZU3EG Device (Weibull fit: XS_{SAT}=1.3e-4cm^2; LET_{TH}=5.5$MeV \cdot cm^2/mg$; W=9.8; S=2.1)

Pulse height analysis techniques were used to determine the fraction of the scintillator counts corresponding to the primary xenon beam. The remaining counts correspond to minimum ionizing particle propagated with the beam and neglected for the SEE analysis due to their very low LET value. The effective LET of this 30 GeV/n Xe ions was evaluated at 3.7 $MeV \cdot cm^2/mg$ using FLUKA simulations[3] and at 4.3 $MeV \cdot cm^2/mg$ by measuring the main peak energy deposition on a diode.

An important difference between UCL and CERN test is that the device under test used at CERN was not thinned (the lid was removed). This is not an issue for high-energy heavy-ions testing as the inelastic interaction length of the beam in silicon is roughly 6 cm. However, heavy-ion can generate nuclear reactions while going through the silicon substrate, which may lead to the generation of secondaries particles, which trough calculations were shown to have similar LET distribution than that generated by high energy protons.

III. Test Results

This section presents SEL and SEU test results measured on the ZU3EG device during both test campaigns. On all the plots, error bars include to 95% statistical confidence intervals plus the dosimetry uncertainties (10% for UCL and 25% for CERN).

A. SEL Test Results

During the standard heavy-ion test campaign, SEL events were observed on V_{CCAUX}, V_{CC_PSAUX} and V_{AUXIO} power domains, for all ions with an LET above than 5.7 $MeV \cdot cm^2/mg$. V_{CCAUX}, V_{CC_PSAUX} and V_{AUXIO} correspond to the auxiliary supply voltage of the programmable logic (FPGA), the processing system and the HPIO respectively. Figures 2, 3 and 4 show the measured SEL cross-sections on these three power domains.

During the high-energy heavy-ion test performed at CERN, no SEL were observed at normal incidence, as shown in Figures 2, 3 and 4. However, the total fluence used during this test was only 2.8×10^6 hi/cm^2 due to the beam distribution as spills, which limits the average flux. This result is

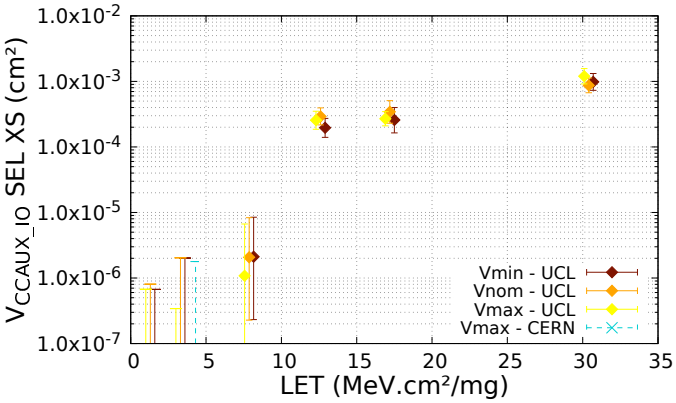

Fig. 4. V_{AUXIO} Power Domain Single-Event-Latchup Cross-Section of XCZU3EG Device (Weibull fit: XS_{SAT}=1.2e-3cm^2; LET_{TH}=7.4$MeV \cdot cm^2/mg$; W=10.0; S=2.3)

consistent with the measurement performed at UCL, at which the SEL threshold was found between LET = 3.3 and 5.7 $MeV \cdot cm^2/mg$. Tests were also performed at 30°, 60° and 90° incidence angles to emulate higher LET ions and see if the device was SEL sensitive with high-energy heavy-ions. SELs were observed only at an incidence of 90°. However, accurate measurement of their cross-section was difficult at CERN, due to multiple simultaneous events occurring at such grazing angles.

B. SEU Test Results

Figures 5, 6 and 7 show the heavy-ion SEU cross-section measured during the UCL and CERN test campaign for the CRAM, the BRAM and the DistRAM of the ZU3EG device. The CRAM upset cross-section was computed on the basis of 29,192,364 configuration bits. This number was extracted from the bitstream mask file, which is usually an effective method to evaluates the number of true configuration bits of a programmable devices. CRAM and BRAM SEU cross-sections of this Ultrascale+ device are 2-4 times lower than the one of the previous generation, denoted as Ultrascale, and reported in [1]. Measured cross-sections at CERN show that the ZU3EG device has similar SEU sensitivity with high-energy heavy-ions and standard heavy-ions. This is discussed in section IV.

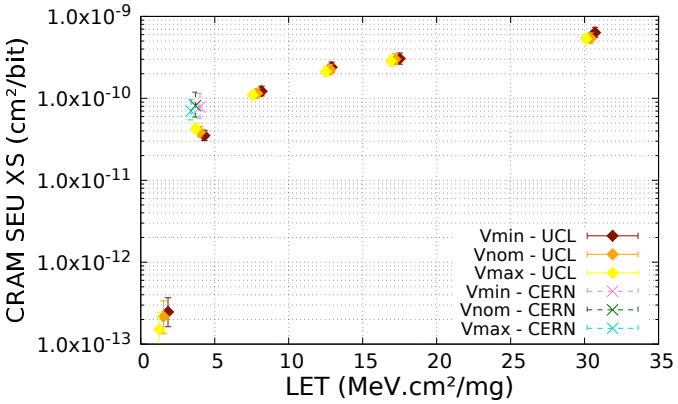

Fig. 5. Per bit CRAM Single-Event-Upset Cross-Section of XCZU3EG Device (Weibull fit: XS_{SAT}=5.4e-10cm^2; LET_{TH}=0.3$MeV \cdot cm^2/mg$; W=15.7; S=2.3)

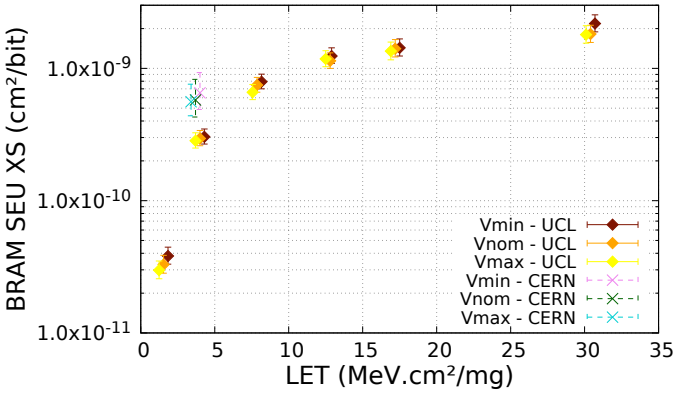

Fig. 6. Per bit BRAM Single-Event-Upset Cross-Section of XCZU3EG Device (Weibull fit: XS_{SAT}=1.8e-9cm^2; LET_{TH}=0.3$MeV \cdot cm^2/mg$; W=10.3; S=2.2)

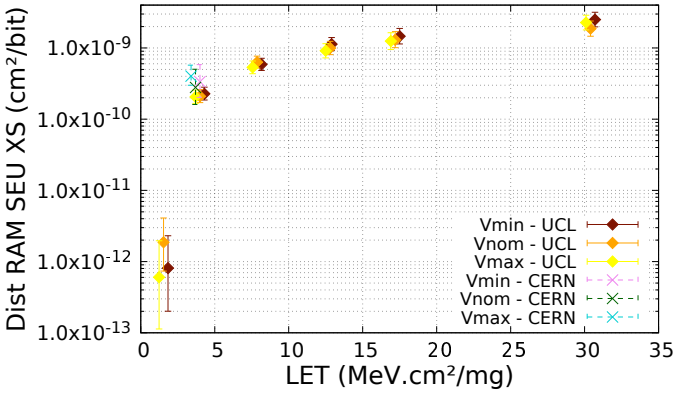

Fig. 7. Per bit Distributed RAM Single-Event-Upset Cross-Section of XCZU3EG Device (Weibull fit: XS_{SAT}=1.9e-9cm^2; LET_{TH}=1.4$MeV \cdot cm^2/mg$; W=10.5; S=1.6)

Figure 8 shows the heavy-ion SEU flip-flop cross-section of the ZU3EG device, measured at CERN and UCL. Note that no upset was observed during the CERN test campaign. The TMR shifter was also tested during both test campaigns but no SEU was observed. However, as the depth of the TMR shifter was 3 times lower than the one of the standard shifter, the measured upper limit SEU cross-section of this TMR implementation is about $5.5E^{-10}$ cm^2/bit with Xe ion (LET = 62.5 $MeV.cm^2/mg$). Burst events were also observed on both shift-registers during radiation testings. Several mechanisms such as upset in the configuration RAM or incorrect operation of the IO during SEL events may explain these bursts. Test results show that the shift registers can be ranked in term of sensitivity to burst events as follows: The TMR shift register is obviously the least sensitive. The shift register bypassing the look-up tables is approximately two time less sensitive than the standard shift register, routed through the look-up tables.

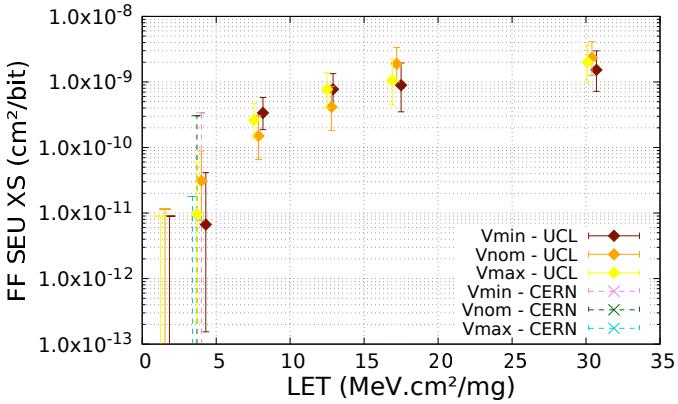

Fig. 8. Per bit FF Single-Event-Upset Cross-Section of XCZU3EG Device (Weibull fit: XS_{SAT}=2.3e-9cm^2; LET_{TH}=1.5$MeV \cdot cm^2/mg$; W=17.2; S=2.3)

IV. Discussion

Measured SEL and SEU cross-sections provided by the high-energy heavy-ion test campaign at CERN are consistent with the results obtained with standard heavy-ion tests. No SELs was observed during the ultra high energy heavy-ion test at normal incidence, confirming that the SEL LET threshold is between 3.7 $MeV \cdot cm^2/mg$ and 5.7 $MeV \cdot cm^2/mg$. SEU cross-sections measured on the three different memories are very close to the value obtained during the UCL test campaign.

This result is consistent with previous works [4]–[8] which compare SRAM SEU cross-sections against the ion energy, up to several hundred of MeV/n, at constant LET. Conclusions of these works are that the ion energy has a very low impact on the measured SEU cross-sections of SRAM memories, for LET higher than the upset threshold, as most of the events are due to direct ionization mechanisms. For LET values that are lower than the upset threshold, previous works report that the SEU cross-section can either decrease [4]–[7] or increase [8] by several orders of magnitude. These large variations are due to indirect ionization mechanisms, which are the main source of upset as the incident ions don't deposit enough energy to induce an SEU.

Xe ions used during the CERN test campaign had a higher LET than the upset threshold of the memories of the ZU3EG device. The good correlation between the measurements obtained at CERN and UCL shows that results reported in [4]–[8] are still valid for energies in the range of several tens of GeV/n and for advanced FinFETs technologies.

Ultra high energy heavy-ion testing had several advantages compared to standard energy heavy-ion test: first, it is not needed to de-lid or thin the device. It is also possible to

perform test at 90° tilt angle. Finally, the possibility to perform test in air simplifies the setup.

V. Conclusion

Standard and high energy heavy-ion test results on a lastest generation SRAM based FPGA were reported, for a large variety of the device features.

Acknowledgments

This work was supported by the European Space Agency under contract No. 4000116569.

References

[1] D. S. Lee *et al.*, "Single-Event Characterization of the 20 nm Xilinx Kintex UltraScale Field-Programmable Gate Array under Heavy Ion Irradiation," in *2015 IEEE REDW*, July 2015.

[2] A. Manuzzato *et al.*, "Effectiveness of TMR-based techniques to mitigate alpha-induced SEU accumulation in commercial SRAM-based FPGAs," in *2007 9th European Conference on Radiation and Its Effects on Components and Systems*, Sept.

[3] T. Böhlen *et al.*, "The FLUKA Code: Developments and Challenges for High Energy and Medical Applications," *Nuclear Data Sheets*, 2014. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0090375214005018

[4] S. K. Hoeffgen *et al.*, "Investigations of Single Event Effects With Heavy Ions of Energies up to 1.5 GeV/n," *IEEE TNS*, Aug 2012.

[5] J. A. Pellish *et al.*, "Heavy ion testing at the galactic cosmic ray energy peak," in *2009 European Conference on Radiation and Its Effects on Components and Systems*, Sept 2009.

[6] N. A. Dodds *et al.*, "Charge Generation by Secondary Particles From Nuclear Reactions in BEOL Materials," *IEEE TNS*, Dec 2009.

[7] R. G. Alía *et al.*, "Sub-LET Threshold SEE Cross Section Dependency With Ion Energy," *IEEE TNS*, Dec 2015.

[8] R. A. Reed *et al.*, "Impact of Ion Energy and Species on Single Event Effects Analysis," *IEEE TNS*, Dec 2007.