MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

MPSoC'13
July 15-19, 2013
Otsu, Japan

Multi-Gigabit Channel Decoders

"Ten Years After"

Norbert Wehn
wehn@eit.uni-kl.de

MPSoC 2003

Parallel SMAP Units N_D Parallel I/O N_{IO}	1 1	4 1	6 1	6 2	6 con. I/O	8 1	8 2
Total Area [mm²]	3.9	9.2	13.3	13.0	18.0	15.9	17.3
Fraction of Memory	85%	69%	69%	68%	77%	61%	64%
Energy per Block [mJ]	48.7	51.7	55.2	50.9	55.2	57.6	55.2
Throughput [MBit/s]	11.7	39.0	50.6	59.6	72.6	59.7	72.7
Efficiency (norm.)	1.00	1.32	1.12	1.47	1.19	1.05	1.24

TECHNISCHE UNIVERSITÄT KAISERSLAUTERN

MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

Channel Coding for Tb/s Communications

(in this talk main focus on Polar Codes)

Norbert Wehn

DFG Deutsche Forschungsgemeinschaft

EPIC

EPIC Grant Agreement No. 760150

TECHNISCHE UNIVERSITÄT KAISERSLAUTERN

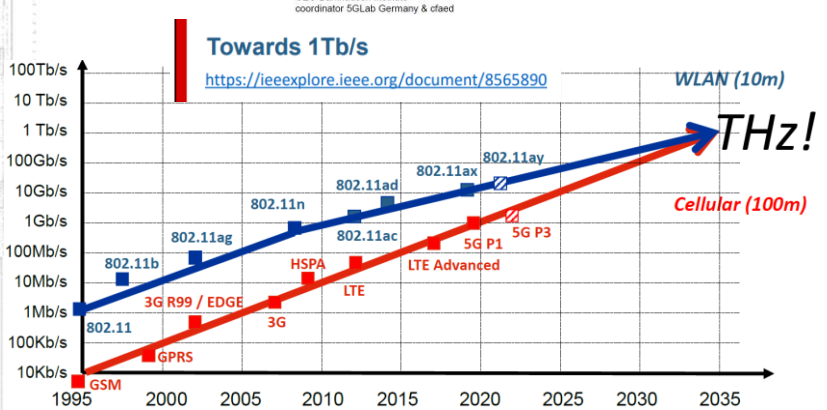
MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

TECHNISCHE UNIVERSITÄT DRESDEN

5G LAB GERMANY

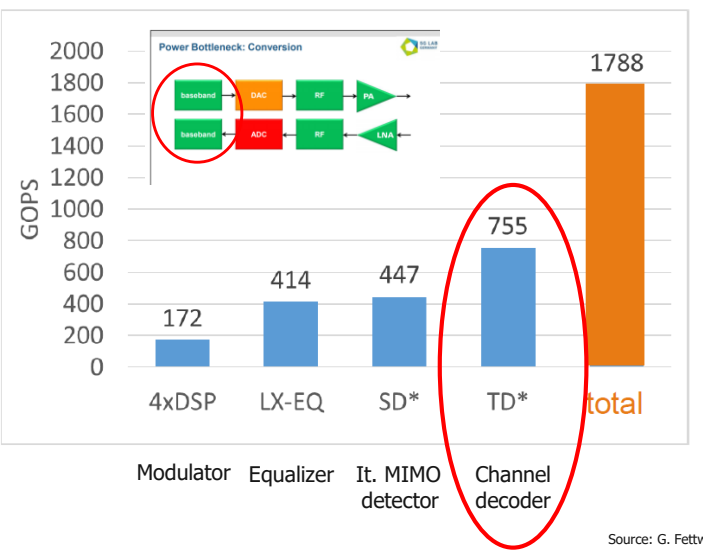
A First Step To Building A 6G HW/SW Platform

Gerhard P. Fettweis Vodafone Chair Professor/TU Dresden
CEO Barkhausen Institute
coordinator 5GLab Germany & cfaed



MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

5G Terminal Baseband Computation Requirements



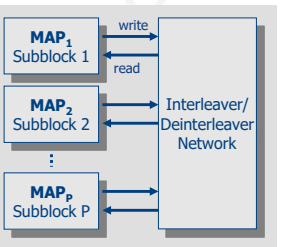
Source: G. Fettweis, MPSoC 2018

MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

Microelectronic Contribution to Channel Coding

2 Turbo-Code decoders in different technologies

- Both decoders designed with the same methodology
- Similar basic architecture: exploit spatial parallelism, sub-blocks on several MAP decoders in parallel



Decoder 1 (2004)

- UMTS compliant decoder in **180nm** technology
- Max frequency **166 MHz**
- **16** MAP decoders in parallel
- Throughput **80 Mbit/s** @ 6 iterations
- **30 mm²**

Journal of VLSI Signal Processing 39, 63–77, 2005

A Scalable System Architecture for High-Throughput Turbo-Decoders

MICHAEL J. THUL, FRANK GILBERT, TIMO VOGT, GERD KREISELMAIER AND NORBERT WEHN
Microelectronic System Design Research Group, University of Kaiserslautern, Erwin-Schroedinger-Strasse, 67663 Kaiserslautern, Germany

MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

Microelectronic Contribution to Channel Coding

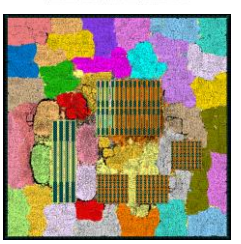
Decoder 2 (2012)

- LTE compliant decoder, **65nm** technology
- Max frequency **450 MHz**
- **32** parallel MAP decoders
- Throughput **2.15Gbit/s** @ 6 iteration
- **7.7 mm²**

2012 7th International Symposium on Turbo Codes and Iterative Information Processing (ISTC)

A 2.15*GBit/s* Turbo Code Decoder for LTE Advanced Base Station Applications

Thomas Ilsseher, Frank Kienle, Christian Weis, Norbert Wehn
Microelectronic Systems Design Research Group, University of Kaiserslautern
67663 Kaiserslautern, Germany
{ilsseher, kienle, weis, wehn}@eit.uni-kl.de



Comparison

- **180nm**, 130nm, 90nm, **65nm**
- Throughput increase **27x**, but frequency increase only **3x**
- Improvement in area efficiency (throughput/area) **100x**

⇒ Progress due to microelectronic mainly in area efficiency

⇒ Throughput increase mainly due to code, algorithm, architecture: e.g. conflict free interleaver, NII, radix-4, re-computation, advanced normalization, larger parallelism…

25 Years of Turbo Codes: From Mb/s to beyond 100 Gb/s

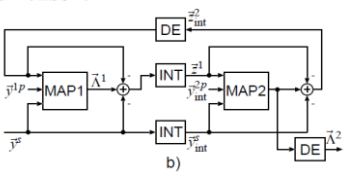
Stefan Weithoffer*, Charbel Abdel Nour†, Norbert Wehn*, Catherine Douillard†, Claude Berrou†
*Department of Electrical and Computer Engineering, Technische Universität Kaiserslautern
Email: *{weithoffer, wehn}@eit.uni-kl.de, †{charbel.abdelnour, catherine.douillard, claude.berrou}@imt-atlantique.fr
†IMT Atlantique, Department of Electronics, Lab-STICC - UMR 6285

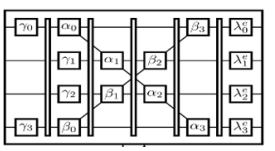
	This Work		[2]	[3]	[4]	[5]	[6]	[7]	[8]
Architecture	UXMAP	FPMAP	PMAP				FPMAP	XMAP	
K	128		6144	6144	6144	6144	6144	6144	6144
Parallelism	128		64	32	64	6144	6144	64	32
n_{IT}	4	40	5.5	5.5	6	6	39	5.5	7
Technology	28 nm		90 nm‡	65 nm†‡	65 nm†‡	65 nm†‡	65 nm†‡	45 nm♣♠	28 nm
Freq. $[MHz]$									625
Throughput $[Gb/s]$									1.13
Area $[mm^2]$									0.49
Area Eff. $[Gb/s/mm^2]$									2.32

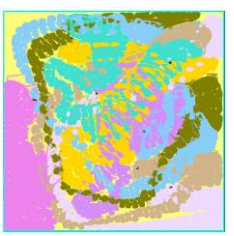
Table I: Comparison
Frequency scaling to 28

2003: 70 Mbit/s @180 nm technology MPSoC 2003
2011: 2.15Gbit/s @65nm technology MPSoC 2013
2018: 102 Gbit/s @28nm techology MPSoC 2019

28nm FDSOI, worst case PVT, LTE turbo code K=128







MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

Towards 1Tb/s FEC Decoders

Power envelope **1 Watt@10mm²,** throughput **1Tb/s@1GHz**

⇒ **~1pJ/bit, ~100mW/mm², ~1000 bits in 1ns**

EPIC
EPIC Grant Agreement No. 760150

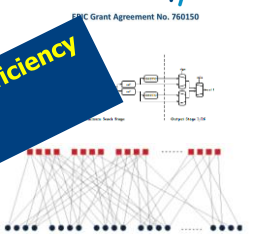
Energy efficient high throughput architectures

- Large locality and regularity, large parallelis

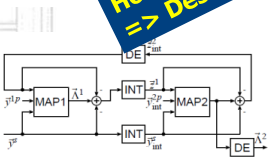
Information theory

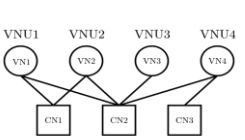
- Irregularity, Iterative/sequenti ithms

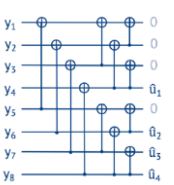
Trade-Off comm. performance vs implementation efficiency
How do different codes compare to each other?
=> Design Space Exploration



Code	Decoding algorith	Locality	Compute kernels	Transfers vs. compute
Turbo code	ative	low (interleaver)	Add-Compare-select	compute dominated
LDPC code	arallel/iterative	low (Tanner graph)	Min-Sum/add	transfer dominated
Polar code	serial	high	Min-Sum/add/sorting	balanced





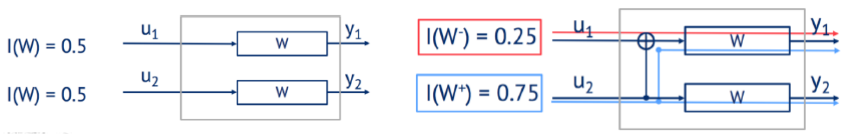


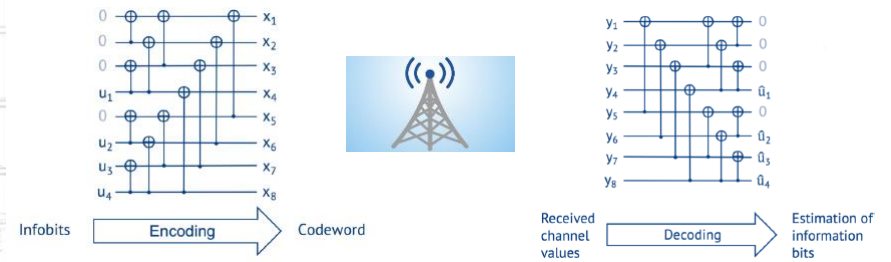
MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

Polar Codes

HUAWEI 5G

- Erdal Arikan (2009), Norbert Stolte (2002)
- Proven to achieve channel capacity for Binary Symmetric Memoryless Channels
- Channel polarization: transformation of independent copies of a channel W into a new set of N channel that can be separated in noiseless and noisy channels



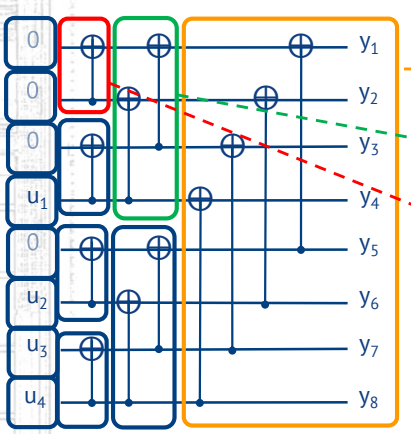


MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

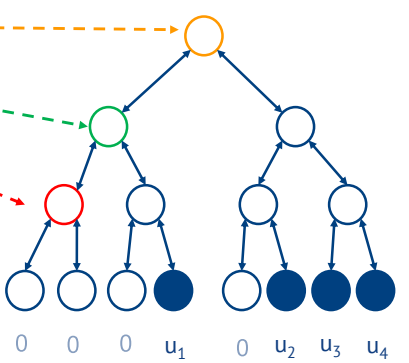
Polar Code Decoding

HUAWEI 5G

Polar Factor Graph (K=8, N=4)



Polar Factor Tree



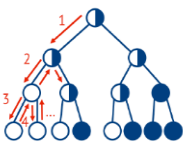
MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

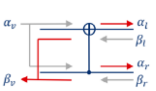
Polar Code Decoding

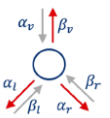
5G

Many different decoding algorithms SC, SCL, SCAN, BP….

- Depth-first or breadth-first traversal on polar factor tree
- Different node operations







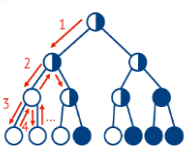
α_{l_i}	**Sucessive Cancelation**	**Successive Cancelation List**	**Soft Cancelation**
α_{r_i}	$f(\alpha_{v_i}, \alpha_{v_{i+N/2}})$	$L * f(\alpha_{v_i}, \alpha_{v_{i+N/2}})$	$f(\alpha_{v_i}, \alpha_{v_{i+N/2}})$
β_{v_i} $\beta_{v_{i+N/2}}$	$f(\alpha_{v_i}, \beta_{l_i} \oplus \alpha_{v_{i+N/2}})$	$L * f(\alpha_{v_i}, \beta_{l_i} \oplus \alpha_{v_{i+N/2}})$	$f(\alpha_{v_i}, \beta_{l_i} + \alpha_{v_{i+N/2}})$
	$\beta_{l_i} \oplus \beta_{r_i}$ β_{r_i}	$L * \beta_{l_i} \oplus \beta_{r_i}$ $L * \beta_{r_i}$ (Sort and Prune List)	$f(\beta_{l_i}, \beta_{r_i} + \alpha_{v_{i+N/2}})$ $f(\beta_{l_i}, \alpha_{v_{i+N/2}}) + \beta_{r_i}$

$$f = sign(a) \times sign(b) \times \min(|a|, |b|)$$

MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

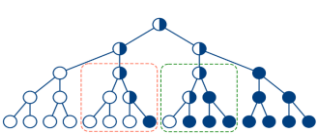
Towards 1Tb/s Polar Code Decoding

Highest throughput: “unrolling” of tree traversal on polar factor tree

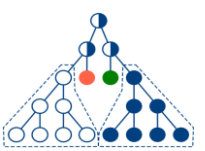


2*(2N-2)+1 stages

- Reduction of tree size by different optimizations e.g.
  - Replace repetition codes and parity check code by one single nodes
  - Merge rate-0 codes and rate-1 nodes into parent nodes



Original Tree

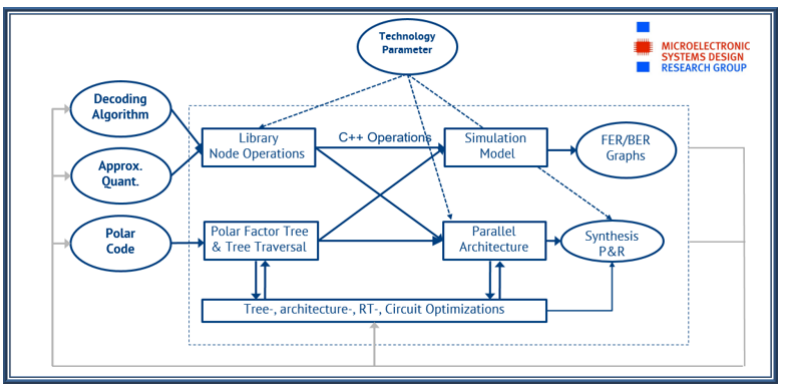


Replaced subtrees

Optimized tree

Polar Decoder Generator Framework

- C++ framework embedded in simulation chain
- Fully automated VHDL and test bench generation, correct-by-construction
- Supports different decoding algorithms: SC, SCLx, SC-MJL, BP
- Optimization engine: tree optimization, retiming, clock gating, latch-based design…

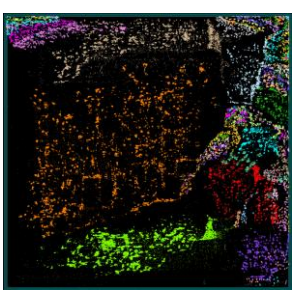


Towards 1Tb/s SC Polar Decoding

1024/512 Code, fast SC decoding algorithms

- Worst case PVT timing 28nm technology, optimized factor tree
- Logic stages 385, retimed pipeline stages 105 (f ~ 600MHz)

Place&Route	Register	Latches
Area [mm^2]	3.14	2.79
- Combinat.	0.96	0.91
- Buf/Inv	0.65	0.27
- Noncomb	1.55	1.12
Area Eff. [Gbps/mm^2]	205	231
Utilization	78%	72%
Frequency [MHz]	621	629
Throughput [Gbps]	636	644
Power [W]	5.7	2.7
- Clock	47%	19%
- Registers	24%	13%
- Combinat.	29%	68%
Energy Eff. [pJ/bit]	8.8	4.2



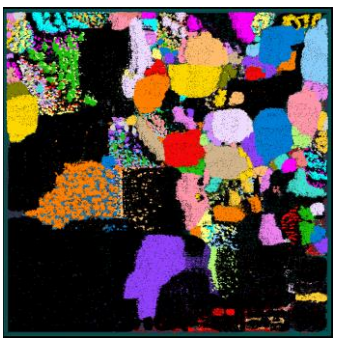
Each colour represents a stage (105)
black color is memory

Towards 1Tb/s SCL Polar Decoding

256/128 Polar Code

- Worst case PVT timing 28nm, optimized tree, retiming, latch based design
- SC vs SCL2, SCL4 @ 125Gbit/s

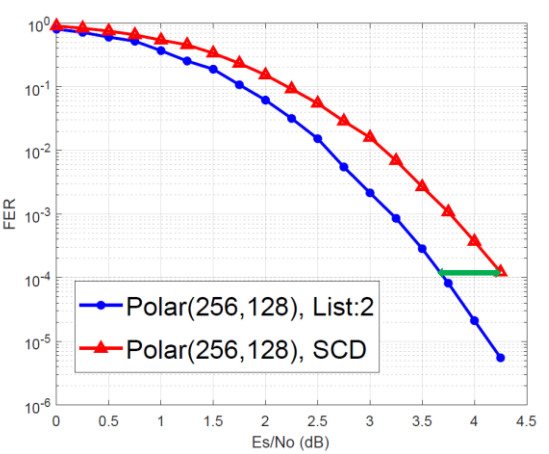
Place & Route	SC	SCL L2	SCL L4
Frequency (MHz)	493	485	481
Throughput (Gbps)	126.1	124.3	123.1
Core Area (mm2)	0.2270	0.5899	1.3754
Area Efficiency (Gbps/mm2)	556	211	89
Utilization %	69	71	74
Power Total (W)	0.200	0.634	1.587
Energy Efficiency (pJ/bit)	1.59	5.11	12.89
Power Density (W/mm2)	0.88	1.08	1.15



SCL4, each colour represents a logic stage, black color is memory

Towards 1Tb/s SCL Polar Decoding

FER 10^{-4}@125 Gbit/s
SCD versus SCList2
1 dB gain
+0.35mm^2, +0.4W

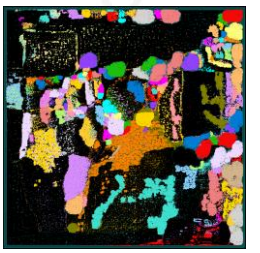


MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

Towards 1Tb/s SCL Polar Decoding

512/427 Polar Code SCL [1]
- Worst case PVT timing 28nm technology
- Normalized to same frequency as [1]

[1] 28nm technology (WC PVT?), SCL2
- Better energy than [1] @ 17x higher throughput



SCL4, each colour represents a logic stage, black color is memory

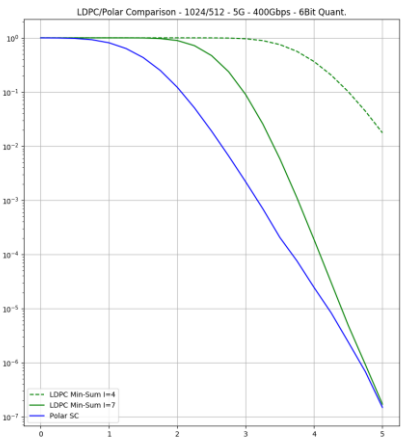
Place & Route	SC	SCL L2	SCL L4	[1]
Frequency (MHz)	493	397	400	468
Throughput (Gbps)	252.2	203.2	204.8	12.0
Core Area (mm2)	0.4235	1.4872	3.2581	0.8700
Area Efficiency (Gbps/mm2)	596	137	63	14
Power Total (W)	0.535	1.266	2.615	0.087
Energy Efficiency (pJ/bit)	2.12	6.23	12.77	7.25
Power Density (W/mm2)	1.26	0.85	0.80	0.10

[1] P. Giard, A. Balatsoukas-Stimming, T. C. Müller, A. Burg, C. Thibeault and W. J. Gross, "A multi-Gbps unrolled hardware list decoder for a systematic polar code," 2016 50th Asilomar Conference on Signals, Systems and Computers, Pacific Grove, CA, 2016.

MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

5G Polar Codes versus LDPC Codes, R=0.5

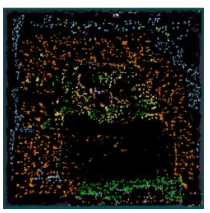
1024/512 5G Polar/LDPC Codes
- 6 bit quantization, SC, Min-Sum (4 & 7 iterations)



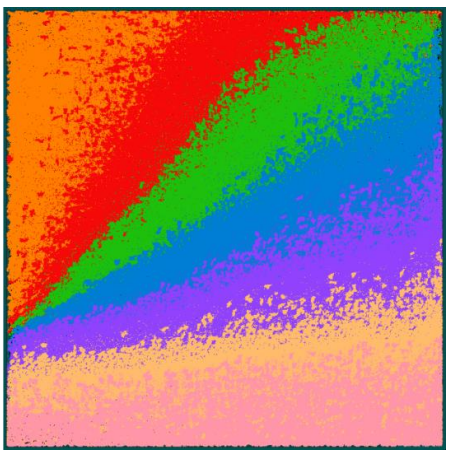
FER 10^{-7}@400 Gbit/s

MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

5G Polar Codes versus LDPC Codes, R=0.5



Polar decoder
1,4 mm^2 @1,2 W
Latency 105ns



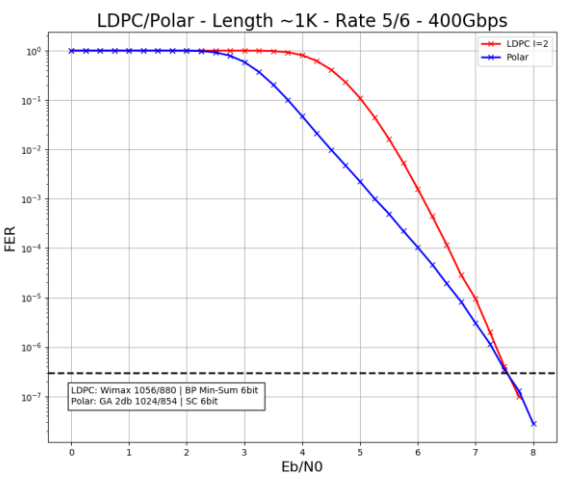
LDPC decoder
6,9 mm^2 @8 Watt
Latency 53ns

MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

Polar Codes versus LDPC Codes, R=5/6

1024 Polar Code/ 1056 LDPC Codes, code rate 5/6

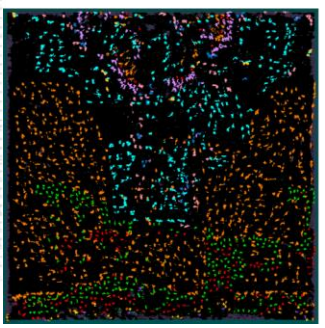
- 6 bit quantization, SC, Min-Sum (2 iterations)



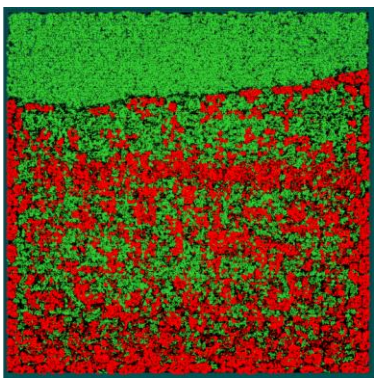
FER ~10^{-7}@400 Gbit/s

MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

Polar Code versus LDPC Codes, R=5/6



Polar decoder
1,2 mm^2 @0,9 W
Latency 67ns



LDPC decoder
1,7 mm^2 @2,0 Watt
Latency 15ns

MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

Summary

- Applications require ever higher throughput, lower latency, better communication performance, higher energy efficiency and low power
- Throughput towards 1 Tb/s are feasible for TC, LDPC, PC in advanced technology
- But
  - Limited to smaller block sizes, low iterations (TC, LDPC) ➔ comm. performance
  - Flexibility challenge
  - Heavy pipelining increases latency, power in clock tree is a major challenge
  - Power (density) one of the biggest challenge

EPIC
EPIC Grant Agreement No. 760150

Thank you for attention!

For more information please visit

http://ems.eit.uni-kl.de